Low Power Technology (LPT) 3.3V Logic, LCX, and FCT3 Logic

Introduction

Pericom manufactures LPT, FCT3, and LCX logic families. The Low Power Technology (LPT) Logic product line is comprised of both 8-bit octals and 16-bit double density products. The LPT series is a faster version of the LCX logic family. LPT/LCX offers a balanced drive +/- 24mA output. The output impedance is ~20Ω for both pull-up and pull-down. Basically, the edges are slow (3ns - 4ns) which results in minimal overshoot and undershoot. In other words, the LPT/LCX families are quiet-low noise. This brief will describe bus contention, live insertion, I/O tolerance, and give a comparison of LPT, FCT3, LCX , ALVC, and ALVT.

LPT vs LVT

ALVT is a BiCMOS logic family that has a bipolar output stage which is generally considered more robust. Even though LPT does not have bipolar technology it does have a very robust output stage during bus contention as shown in Figure 1.

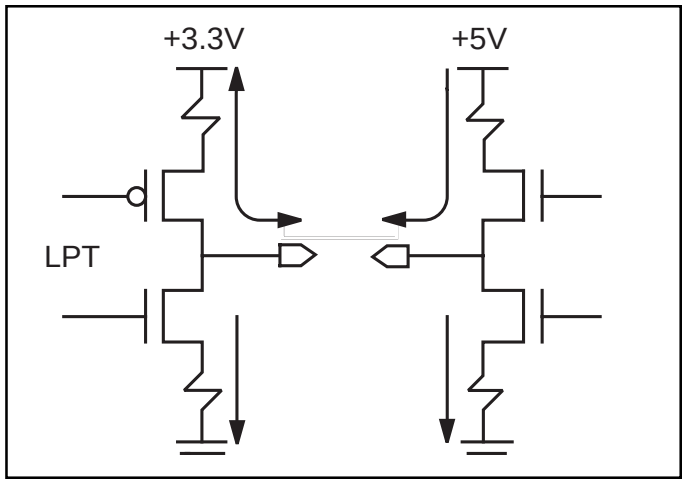

Figure 1. LPT/LCX Bus Contention

When LPT drives the bus, a specification called Output High Current (I_{ODH}) allows the instantaneous or transition current to go as high as 110mA. Also, when LPT goes low the sink current, which is called I_{ODL} or Output Low Current, can sink up to 200mA of transition current (I_{ODH} and I_{ODL} are not generally specified in other type logic). Outputs can withstand a 1 second duration when grounded or at +5V. A worst-case condition exists when both devices on the bus try to drive at the same time-this is referred to as *bus contention.* If LPT is connected to a 5V bus (no problem because LPT is I/O tolerant) as in Figure 1, the 5V logic device will try to push current into the active high LPT device. Generally this current is about 50mA and is not a problem.

Live Insertion

When inserting a logic device in a live circuit the most important rule is power sequencing. For instance; ground, disable, and power should be connected in this sequence through a staggered edge PCB. Another hint is to make sure the disable RC time is about 10 times less than the power RC time as shown in Figure 2. This insures that the part will be disabled and won't disrupt bus data during insertion. Actually all logic families should follow these hints. Also see Figure 4.

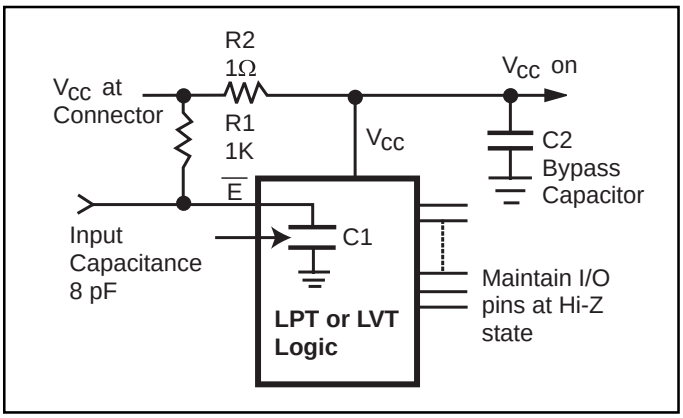

Figure 2. Live Insertion

What Does I/O Tolerance Mean?

A special advantage was designed into LPT products-5V I/O tolerance. This means that all input and output pins can be connected to 5V logic or bus even when power to the LPT device is 3.3V (no damage to the LPT device will occur, see Figure 4). FCT3 has input tolerance but not output tolerance.

Competition

Table 1 exhibits the advantages of LPT/FCT3. It should be noted that all technologies shown are CMOS except for LVT which is BiCMOS.

Table 1. Competitive Comparisons

Comparison	LPT	FCT3	LCX	ALVT	ALVCH
I/O Tolerance	X		X	X	
Propagation Delay	4ns		7.1ns	2.5ns	3ns
Low Noise	X		X	X	X
Robust Outputs	X		X	X	X
Low Power	X		X		X
2.5V Low Voltage Operation	X		X		

LPT/LCX Output Stage Description

Pericom has developed a proprietary design that guarantees the normal PMOS inherent diode from source-to-drain (see Figure 3) will never forward bias causing current flow during a shut down mode (V_{CC} = 0V) or in live insertion mode.

Figure 4 shows this proprietary controller that senses the output voltage. When the buffer is driving a 5V bus the inherent diode would normally forward bias, but as seen in Figure 4 the diode is connected to the 5V tolerant controller. This controller disconnects the diode with a muxing action, thus allowing no current flow when the LPT/LCX device is shut down or in live insertion.

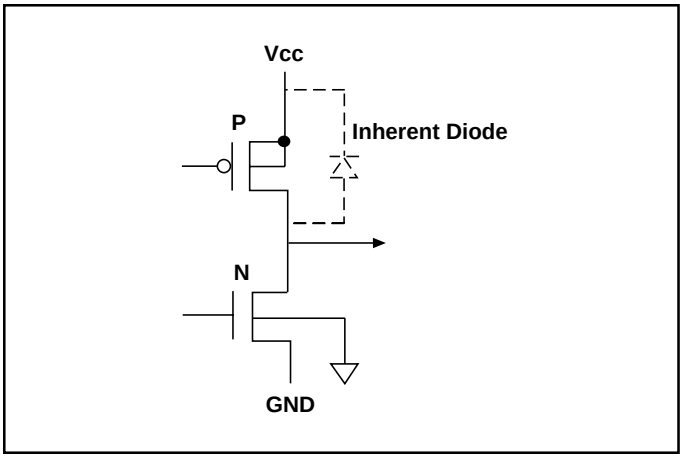

Figure 3. Typical Logic Output Stage

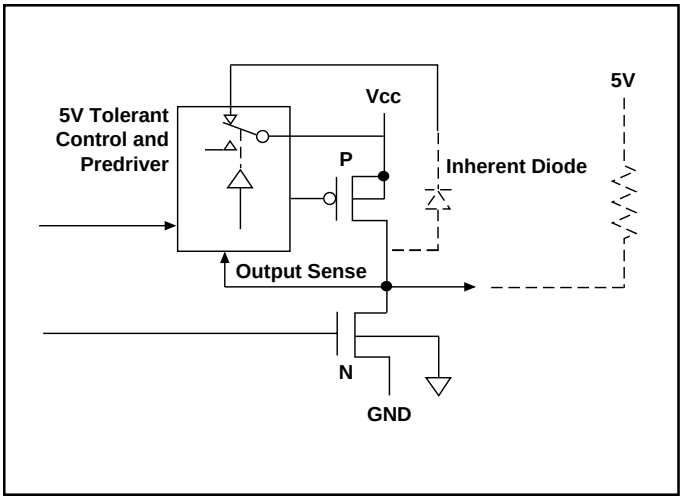

Figure 4. LPT/LCX Output Stage