PC100 Registered SDRAM Module Design

by Michael Yen

A conventional way to boost PC performance has been to raise the internal clock frequency of a microprocessor while the microprocessor's external bus remains the same at 66 MHz. As the Pentium II microprocessor internal bus reaches 350 MHz or higher, memories and core-logic must keep up with microprocessor performance. The microprocessor's external bus on the motherboard must run at a clock rate higher than 66 MHz. EDO DRAM has reached its performance limit at 66 MHz. The best possible performance of EDO DRAM is only equal to the performance of the 66 MHz SDRAM module. To keep up with new generation platform performance, attention has been focused on the increased clock rate of SDRAM.

Since SDRAM performance is proportional to its clock frequency, a SDRAM module running at 100 MHz on the motherboard bus has a 50 percent performance increase over the 66 MHz SDRAM module and the best EDO DRAM module.

The cost difference of memories is small and DRAM prices keep dropping, the 100 MHz SDRAM module is the best choice because of performance, cost and availability. EDO DRAM has almost disappeared in new PC platform designs.

Clock Signals of SDRAM DIMM Modules

The most popular SDRAM module, the 168-pin DIMM, has up to 36 or more SDRAM chips. Each SDRAM chip needs a clock input as shown in Figures 1(a) and 1(b). Providing clocks to 36 SDRAM chips, the clock distribution circuit is critical in DIMM module design. At 100 MHz, a clock period is only 10 ns, making the timing delay along the trace very significant. The timing skew among such a large number of clock signals for SDRAM chips is critical. Clock rise time is also important. To maintain clock signal integrity, the JEDEC specification requires a motherboard to provide ***four*** identical clock signals to each DIMM module at module pins 42, 79, 125, and 163 (see Figure 2. These four clock signals are identical and are driven by four separate clock drivers. If a motherboard has 3 DIMM sockets, then that motherboard must provide twelve identical clock signals driven by twelve clock drivers.

To minimize timing skew among the clock signals, the DIMM board layout design assures that the trace length of all clock signals on a module must be nearly equal.

An Unbuffered SDRAM DIMM module uses memory chips without buffer chips for clock/address/control signals. Each clock signal from the motherboard typically directly drives only 2 or 3 SDRAM chips on a module. JEDEC specifies that each clock signal from the motherboard can drive 4 chips maximum. Since there are only four clock signals from the motherboard, an Unbuffered SDRAM DIMM module can have a maximum of 16 SDRAM chips.

Registered SDRAM DIMM

Server/workstation/high-end PC platforms require very large DRAM memory size, typically more than 4 DIMM modules and more than 16 SDRAM chips per module as indicated in Table 1. Because of overloading of the address/control/clock signals, Unbuffered SDRAM DIMM modules cannot support such applications. Therefore, Buffered SDRAM DIMM module products are required. A clock signal needs a PLL driver as a buffer to generate clock outputs identical to the clock input with zero propagation delay. Since registered buffer drivers are used to buffer address/control signals, a buffered SDRAM DIMM is called a ***Registered*** SDRAM DIMM. Figure 3 shows the Registered SDRAM DIMM.

Table 1. Registered SDRAM DIMM Module Configurations

Config #	DIMM Capacity	DIMM Organization	SDRAM Chip Organization	#SDRAM Chips	#Rows of SDRAM Chips
1	32 MB	4Mx72	4Mx4	18	1
2	64 MB	8Mx72	8Mx8	9	1
3	128 MB	16Mx72	16Mx4	18	1
4	256 MB	32Mx72	16Mx4	36	2
5	512 MB	64Mx72	32Mx4	36	2

2509A/2510A PLL Drivers

The PLL buffer needs only one clock signal, CK0, from the motherboard, to generate 9 or 10 clock signals on a module. The motherboard provides one clock signal per DIMM module whose design greatly reduces the number of clock signals generated by motherboard and minimizes EMI problems.

As indicated in Figure 4, CK0, from the motherboard, is the Input Clock to the 2509A. Nine copies of CK0 are generated at outputs of the 2509A. Each clock output typically drives the SDRAM chips directly without any external damping series resistor.

The feedback output FBOUT pin is directly connected to the feedback input FBIN pin. Figures 5(a) and 5(b) show the output clocks lead and lag the input clock, respectively. The C1 capacitor is designed to adjust the relative timing between the input clock and the output clocks, if needed. C1 is typically not connected. As the C1 value increases, the timing of the output clocks will advance in time relative to the input clock.

To run at 100 MHz, a clock output driver must be high-drive and quiet. The output drivers of Pericom's PI6C2509A have been carefully designed to provide sufficient heavy pull-up and pull-down drive currents such that the clock signals at SDRAM chips meet the rise/fall time requirements. The output drivers are also designed for minimum undershoot and overshoot

When a designer selects a PLL driver chip for his PC100 SDRAM DIMM module design, the following AC parameters are critical:

Phase Error is the propagation-time between the Clock Input pin and the clock feedback input FBIN pin. Since it is ideal to have the clock outputs exactly identical to the clock input, phase error should be very small. A phase error of 150ps leading or lagging is fine in 100 MHz and 66 MHz clock distribution circuits. A DIMM is typically required to run at both 100 MHz and 66 MHz. It could be a problem for a DIMM module if the phase error of a PLL clock driver meets the spec at 100 MHz, but not at 66 MHz. The Pericom 2509A part is designed to meet the phase error spec for both 100 MHz and 66 MHz clock operations.

Cycle-to-Cycle Jitter is the difference of period-time between one clock cycle to the adjacent clock cycle. If the clock input has no spread spectrum modulation, PC100 allows ±100ps cycle-to-cycle jitter at clock outputs. A critical jitter issue is clock input with spread spectrum. Many PLL circuits will greatly increase jitter and fail to meet jitter specs when the motherboard clock generator enables spread spectrum modulation. Pericom's 2509A/2510A parts are designed to meet the jitter spec when spread spectrum is disabled as well as when it is enabled, applying also for 100 MHz and 66 MHz.

Output Skew is the "time skew" among all clock outputs. The output drivers of Pericom's 2509A/2510A parts are carefully designed to meet the 200ps spec at 100 MHz as well as 66 MHz.

Routing of Clock Outputs

Since the skew among all clock outputs is critical, every clock output from 2509A/2510A must have the same trace length and the same loading. Each clock output must drive the same number of SDRAM chips. Per JEDEC spec, each clock can drive no more than four SDRAM chips.

Table 2. PLL Drivers Required by Each DIMM Configuration

Config # of Table 1	DIMM Capacity	Number of SDRAM chips	2509A or 2910A is used	Number of Clock Outputs Used	Number of Unused Clock Outputs
1	32 MB	18	2509A	Use 6 clocks to drive the 18 SDRAM chips Use 1 clock to drive 2 registered drivers	2
2	64 MB	9	2509A	Use 3 clocks to drive the 9 SDRAM chips. Use 1 clock to drive the 2 registered drivers	5 (One Bank of 2509A is unused)
3	128 MB	18	2509A	Use 6 clocks to drive the 18 SDRAM chips. Use 1 clock to drive the 2 registered drivers	2
4	256 MB	36	2510A	Use 9 clocks to drive the 36 SDRAM chips Use 1 clock to drive the 3 registered drivers	0
5	512 MB	36	2510A	Use 9 clocks to drive the 36 SDRAM chips Use 1 clock to drive the 3 registered drivers	0

ALVC16334/162835/16836 Registered Drivers

An SDRAM chip needs address and control signals, in addition to clock and data signals (see Figures 1(a) and 1(b). For Unbuffered SDRAM DIMM, each and every address/control signal from the motherboard has to drive all SDRAM chips on the module. The address/control driver on motherboard will be over-loaded if there are many DIMM modules (there are 18 or more SDRAM chips on each module).

The ALVC16835/162835 18-bit Registered Universal Bus Drivers are used to buffer the address/control signals from the motherboard. When a DIMM module is selected by the motherboard, the registered drivers on the DIMM module are operated at rising-edge clock mode. When a DIMM module is not selected by the motherboard, the registered drivers are operated at transparent mode for input signals to flow through.

The output drivers of **ALVC16835** have no embedded series termination resistor on chip, for use in a DIMM module with heavily loaded memory chips. The output drivers of **ALVC162835** have an embedded series termination resistor on chip for signal damping in light-loaded DIMM module applications. Because bus hold introduced an unwanted latency on the memory bus that could slow the system, Pericom has removed the standard bus hold feature.

Pericom offers five functions to support the address/control buffer of PC100 100 MHz SDRAM DIMM modules:

Part Number	Package and Pin Count	Number of Bits
PI74ALVC16334/162334	48-pin 240 mil wide plastic TSSOP (A48) 48-pin 173 mil wide plastic TVSOP (K48) 48-pin 300 mil wide plastic SSOP (V48)	16
PI74ALVC16835/162835	56-pin 240 mil wide plastic TSSOP (A56) 56-pin 173 mil wide plastic TVSOP (K56) 56-pin 300 mil wide plastic SSOP (V56)	18
PI74ALVC162836	56-pin 240 mil wide plastic TSSOP (A56) 56-pin 173 mil wide plastic TVSOP (K56) 56-pin 300 mil wide plastic SSOP (V56)	20

In addition to **ALVC16835/162835**, there are other registered drivers to give module designers flexibility to reduce manufacturing cost, i.e., an 18-bit PI74ALVC16835/162835 could be replaced by a 20-bit PI74ALVC162836 for two additional clock outputs and a cost savings of one logic-inverter part. ALVC16334/162334 are 16-bit registered driver parts for module applications that only need 16-bit drivers, resulting in a smaller 48-pin package and a cost savings of one logic-inverter part. To save the logic inverter see Figures 6(a) and 6(b), the LE pin is now complemented.

Number of Signals Required to be Buffered by Registered Driver

Configuration Number 2 has the smallest number of SDRAM chips on a module. The 64 MB DIMM requires 28 signals to be buffered by a registered driver (see Figure 7). Two 16-bit registered drivers, ALVC162334, can provide buffers for 32 signals. Therefore, there are four unused buffers. Since each signal drives only eight SDRAM chips, the ALVC162334 part is recommended because it provides an on-chip damping series resistor at each driver output to avoid undershoot/overshoot noises.

Other configurations have 18 or more SDRAM chips. No on-chip damping series resistors are needed.

Configurations 4 and 5 have 36 SDRAM chips. Each address/control signal, except DQMBx and Sx#, requires two registered drivers, since each registered driver can only drive a load of up to 18 SDRAM chips.

An unused input should be held at a valid high or low voltage by a pull-up or pull-down resistor.

As mentioned above, ALVC16334/162334 has 16-bit drivers. ALVC16835/162835 has 18-bit drivers. And ALVC162836 has 20-bit drivers. Each bit provides a buffer for one address/control signal to drive up to 18 SDRAM chips. To avoid too many unused bits, the following registered drivers are recommended to each DIMM configuration.

It is possible to use the 18-bit ALVC16835/162835 as registered driver parts in each DIMM configuration, although the number of unused bits in each registered driver part may increase.

Table 3. Number of Signals Required to be Buffered by Registered Driver

Config. Number	DIMM Capacity	DIMM Organization	SDRAM Chip Organization	#SDRAM Chips	Number of Signals buffered by Registered Drivers
1	32 MB	4Mx72	4Mx4	18	29
2	64 MB	8Mx72	8Mx8	9	28
3	128MB	16Mx72	16Mx4	18	29
4	256MB	32Mx72	16Mx4	36	50
5	512MB	64Mx72	32Mx4	36	50

Table 4. Registered Driver Recommended for Each DIMM Configuration

Config #	DIMM Capacity	DIMM Organization	No. of Signals Buffered by Registered Drivers	Recommended Registered Drivers	Alternate Registered Drivers
1	32 MB	4Mx72	29	(2) PI74ALVC16334	(2) PI74ALVC16835
2	64 MB	8Mx72	28	(2) PI74ALVC162334	(2) PI74ALVC162835
3	128 MB	16Mx72	29	(2) PI74ALVC16334	(2) PI74ALVC16835
4	256 MB	32Mx72	50	(2) PI74ALVC16334 (1) PI74ALVC162836	(3) PI74ALVC16835
5	512 MB	64Mx72	50	(2) PI74ALVC16334 (1) PI74ALVC162836	(3) PI74ALVC16835

List of PLL Drivers and Registered Drivers Used

Each DIMM configuration uses a PLL Driver as shown in Table 2, and Registered Drivers as indicated in Table 4. The following table summarizes the recommended drivers for each DIMM configuration.

Table 5. PLL Driver and Registered Driver Recommended for Each DIMM Configuration

Config. Number	DIMM Capacity	DIMM Organization	SDRAM Chip Organization	#SDRAM Chips	Recommended Drivers	Alternate Drivers
1	32 MB	4Mx72	4Mx4	18	(1) PI6C2509A (2) PI74ALVC16334	(1) PI6C2509A (2) PI74ALVC16835
2	64 MB	8Mx72	8Mx8	9	(1) PI6C2509A (2) PI74ALVC162334	(1) PI6C2509A (2) PI74ALVC162835
3	128 MB	16Mx72	16Mx4	18	(1) PI6C2509A (2) PI74ALVC16334	(1) PI6C2509A (2) PI74ALVC16835
4	256 MB	32Mx72	16Mx4	36	(1) PI6C2510A (2) PI74ALVC16334 (1) PI74ALVC162836	(1) PI6C2510A (3) PI74ALVC16835
5	512 MB	64Mx72	32Mx4	36	(1) PI6C2510A (2) PI74ALVC16334 (1) PI74ALVC162836	(1) PI6C2510A (3) PI74ALVC16835

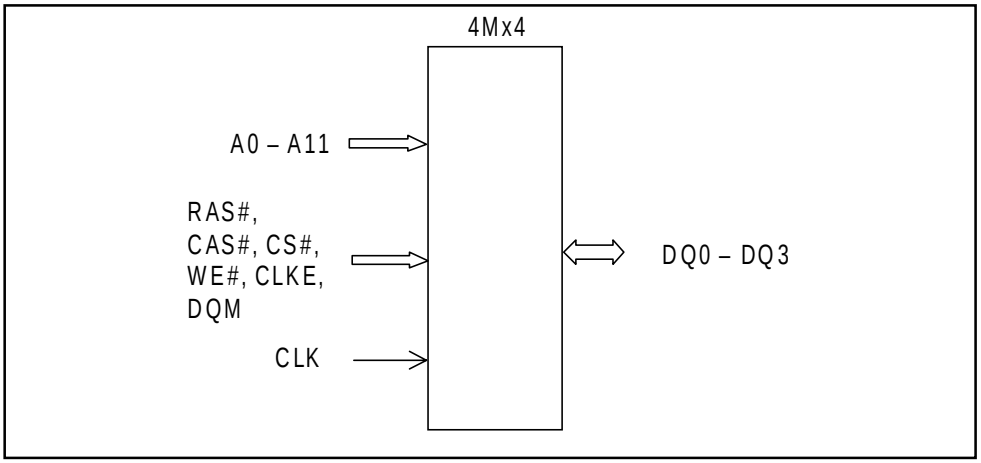

Figure 1(a). SDRAM Chip 4Mx4

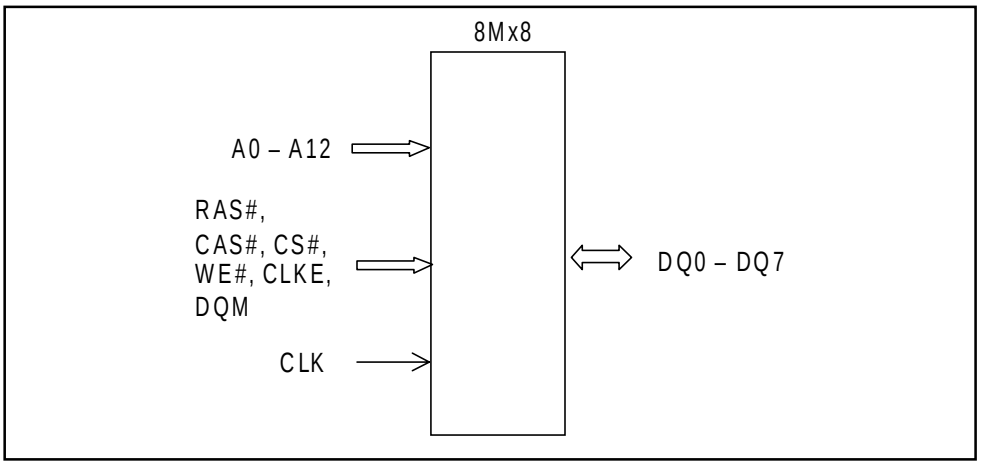

Figure 1(b). SDRAM Chip 8Mx8

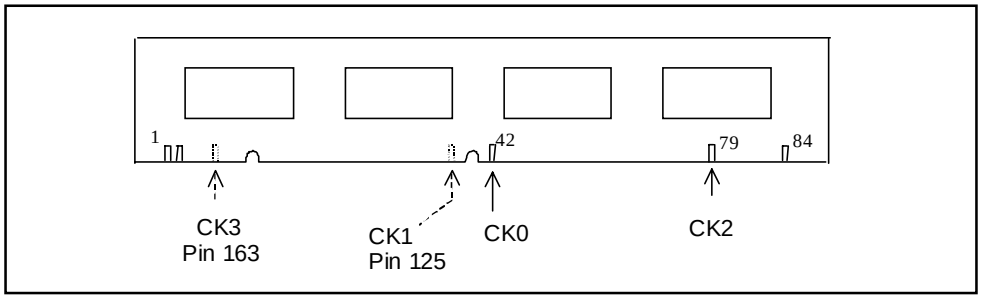

Figure 2. Unbuffered 168-pin SDRAM DIMM

CK0 and CK2 are at the front side. CK1 and CK3 are at the backside. The four clock signals from the motherboard directly drive the eight SDRAM chips – each clock signal drives two chips. There is no PLL driver or logic buffer driver.

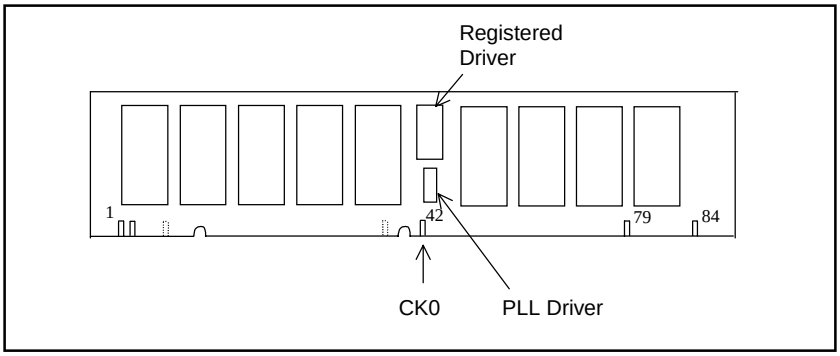

Figure 3. Registered 168-pin SDRAM DIMM

Only clock CK0 is used. The PLL driver generates 9 or 10 copies of clock CK0 on the DIMM module. A registered driver buffers the Address/control signals.

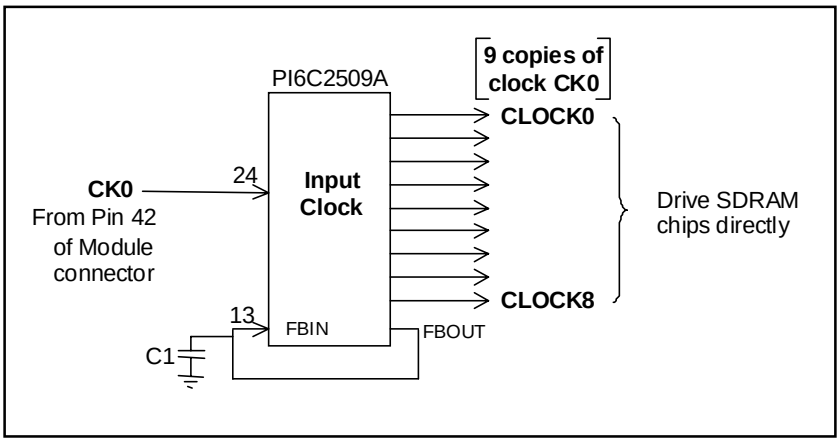

Figure 4. Block Diagram of PI6C2509A

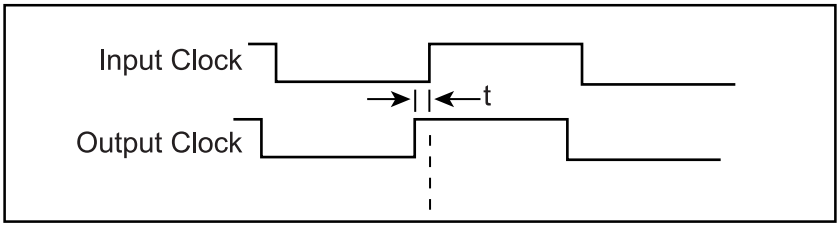

Figure 5(a). Output Clocks Lead the Input Clock

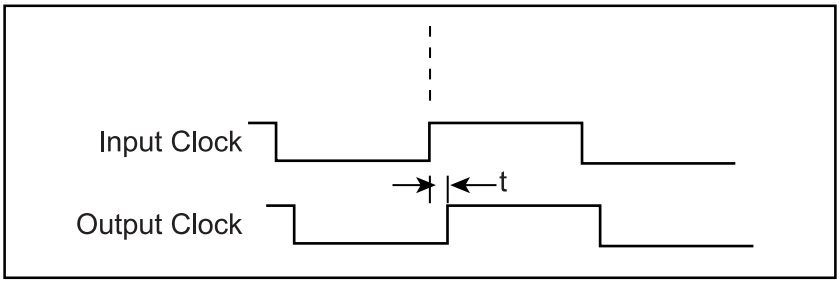

Figure 5(b). Output Clocks Lag the Input Clock

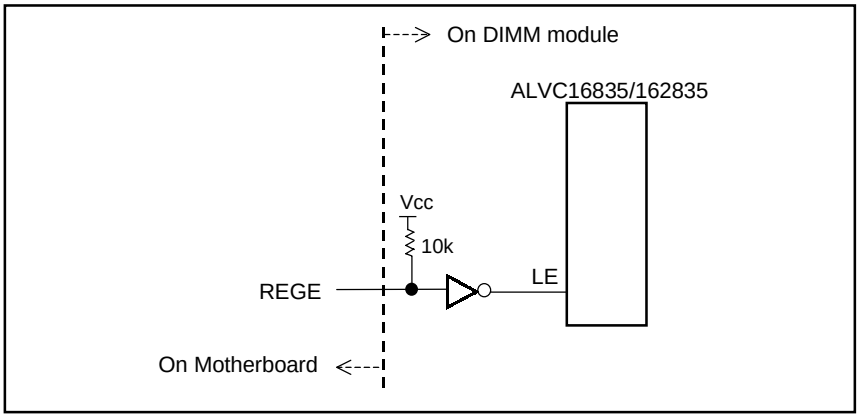

Figure 6(a). ALVC16835/162835 Registered Driver Needs a Logic Inverter

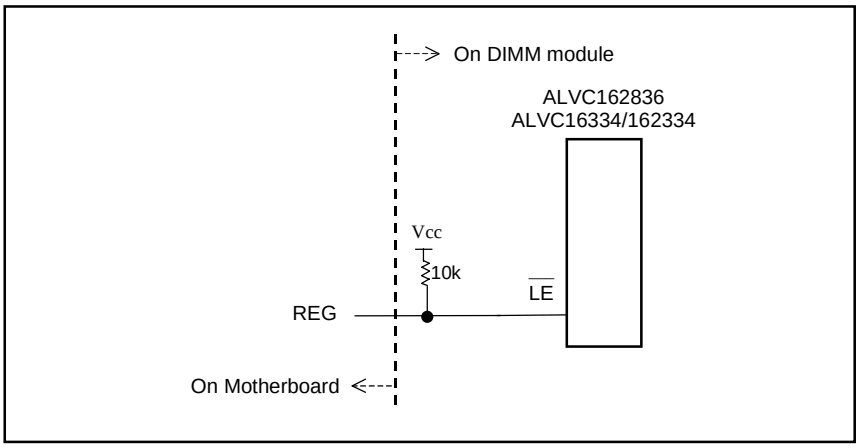

Figure 6(b). ALVC162836 and ALVC16334/162334 Registered Drivers Do Not Need a Logic Inverter

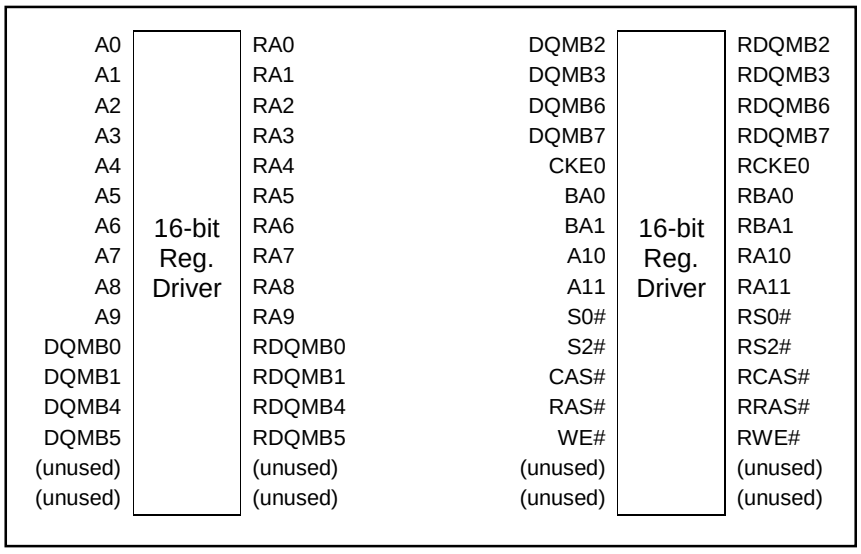

Figure 7. The 64-MB DIMM Uses Two 16-bit Registered Drivers to Provide 28 Control/Address Signals on the Module.