Design Guide Lines for Registered DDR DIMM Module Using PI74SSTV16857 Register and PI6CV857 PLL Clock Driver.

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Introduction

DDR SDRAM boosts performance by transferring data on both edges of the clock yet allows memory suppliers to employ the same packaging and test equipment used with the current generation of SDRAMs. Double Data Rate design enables memory to keep pace with the ever-increasing microprocessor speeds in servers, workstations, PCs, data communications and consumers products.

The 184-pin DDR registered DIMM offers reduced system loading by including on-board registers for additional signal drive and a zero delay PLL for clock distribution. With this added circuitry, DIMMs can be designed with higher memory density since there is now a reduction in memory signal loading. A typical 133 MHz, 64-bit wide DIMM designed with Pericom's DDR solution will deliver up to 2.1-gigabytes/sec data bandwidth. DDR memory modules require between 23 and 27 registered control and address lines, so two 14-bit PI74SSTV16857 Registers are required on each memory module. In order to synchronize signals on the individual memory chip, a PI6CV857 PLL is also required on each memory module.

The PI74SSTV16857 is a 14-bit stub-series-terminated logic (SSTL_2) registered driver with differential clock inputs to provide the DDR SDRAM with address and control signals. The PI74SSTV16857 provides fast address signaling with minimal propagation delay when driving LVTTL or SSTL_2 signals from the memory controller to the SDRAM's SSTL signal input pins. LVTTL switching levels are implemented with systems that use frequencies less than 100 MHz, while SSTL_2 is more commonly used for systems with frequencies greater than 125 MHz.

The DDR clock driver is a 2.5V driver designed to meet the new technology needs of high-speed data transfers. The concept is that data is clocked on both the rising as well as the falling edge of the clock. This results in Double Data Rate (DDR) transfers. PI6CV857 zero delay clock buffer is used to synchronize signals to each memory chip. The PI6CV857 is a 170 MHz, SSTL_2 optimized 1:10 clock buffer with impressive jitter (less than 75 Pico seconds), phase error (50 Pico seconds) and output skew (100 Pico seconds) specification. This industry leading clock buffer allows a single clock source to drive a memory module's multiple DDR SDRAM devices.
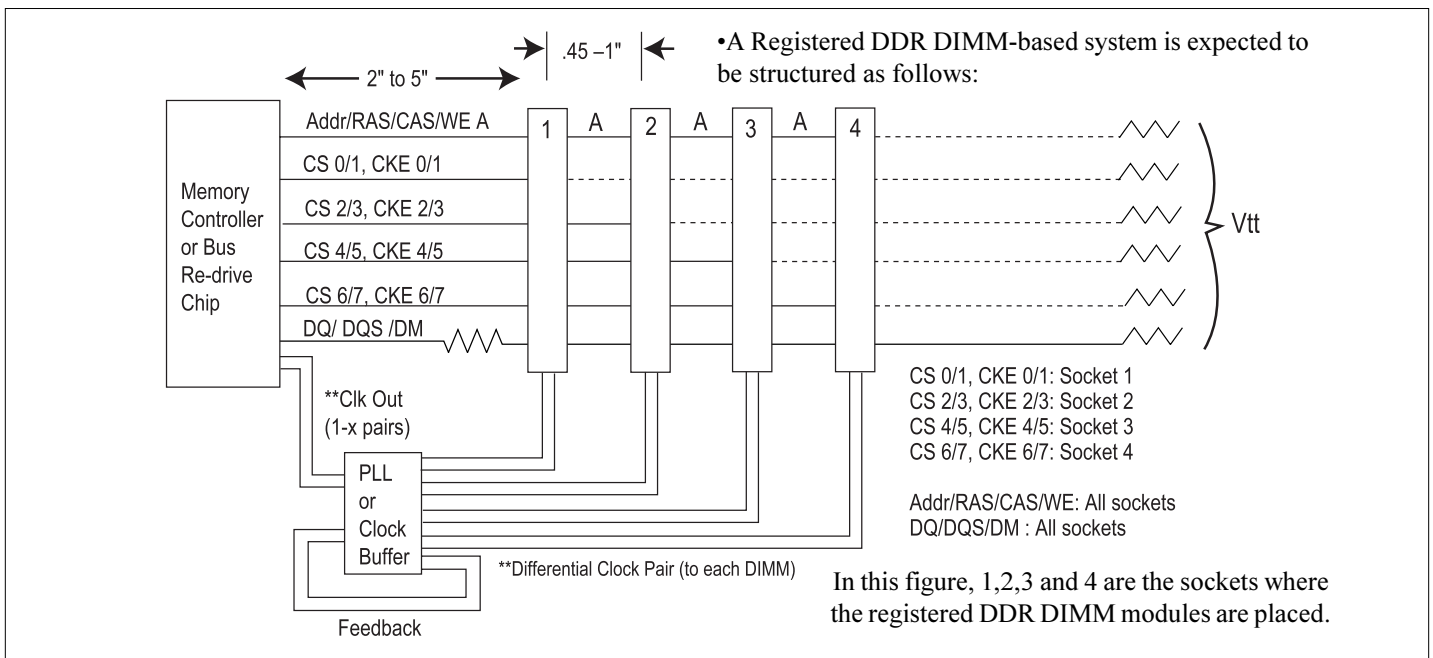
Typical PC2700 RDIMM Application Environment
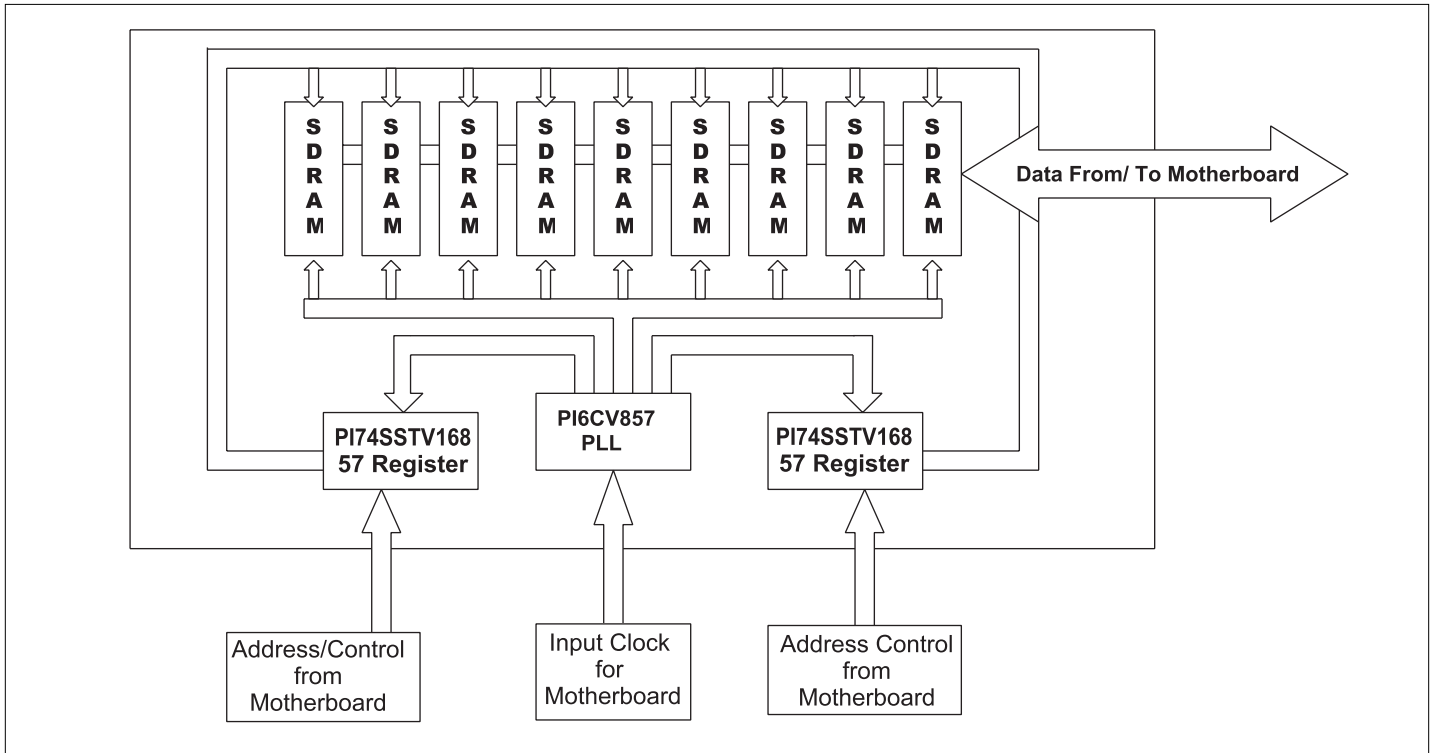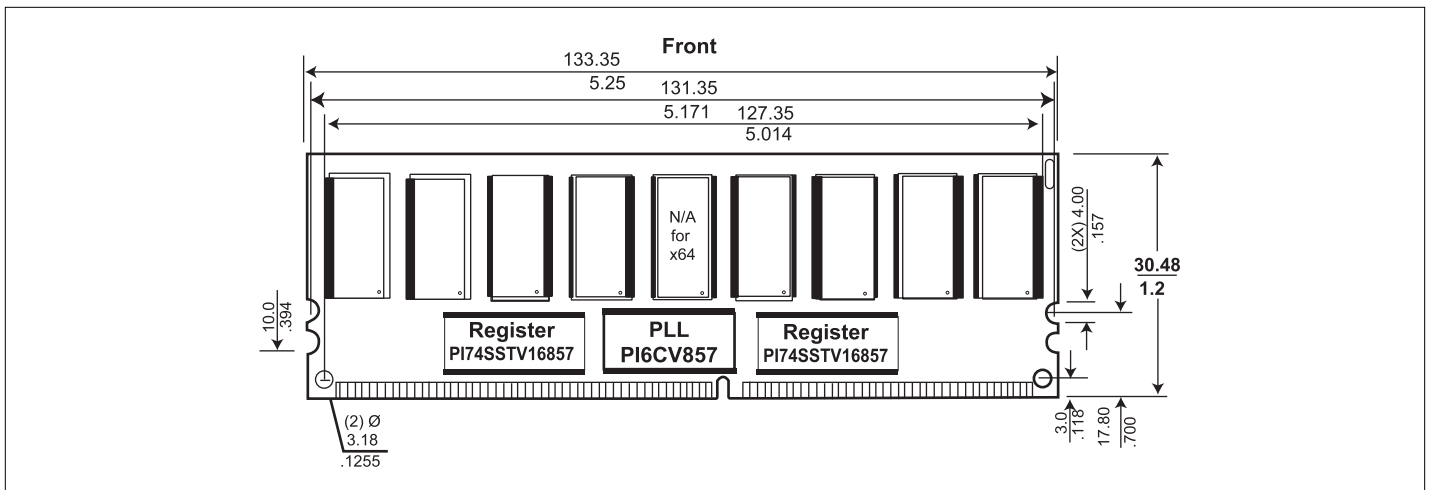
Registered DDR DIMM Block Diagram

A Registered DDR DIMM Module consists of three key parts.
1. DDR-SDRAM Memory Chips
2. DDR PLL Clock buffer.(PI6CV857)
3. Registers(x2).(PI74SSTV16857)

Component Types and Placement:

Components should be surface mounted on both sides of the PCB and positioned on the PCB to meet the minimum and maximum trace lengths required for DDR SDRAM signals. Bypass capacitors for DDR SDRAM devices must be located closer to the device power pins.

The following layout suggest placement for the Raw Card Version A. Exact spacing is not provided, but should be based on manufacturing constraints and signal routing constraints provided by this design guide.

Example Raw Card Version A (2 Physical Banks) Component Placement

Back

Side

N/A
for
x64

(Front)

3.99
.157 max

4.24
.167

1.27 ± 0.10
.050 ± .004

Note: All dimensions are typical unless otherwise stated. Millimeters
Inches

Oms (nominal)

PLL

SDRAM
Stack

OUT1

120 Ohm

P
I
6
C
V
8
5
7

SDRAM
Stack

CK0

IN
PI6CV857

CK0

120 Ohm

240 Ohm

PI74SSTTV16857
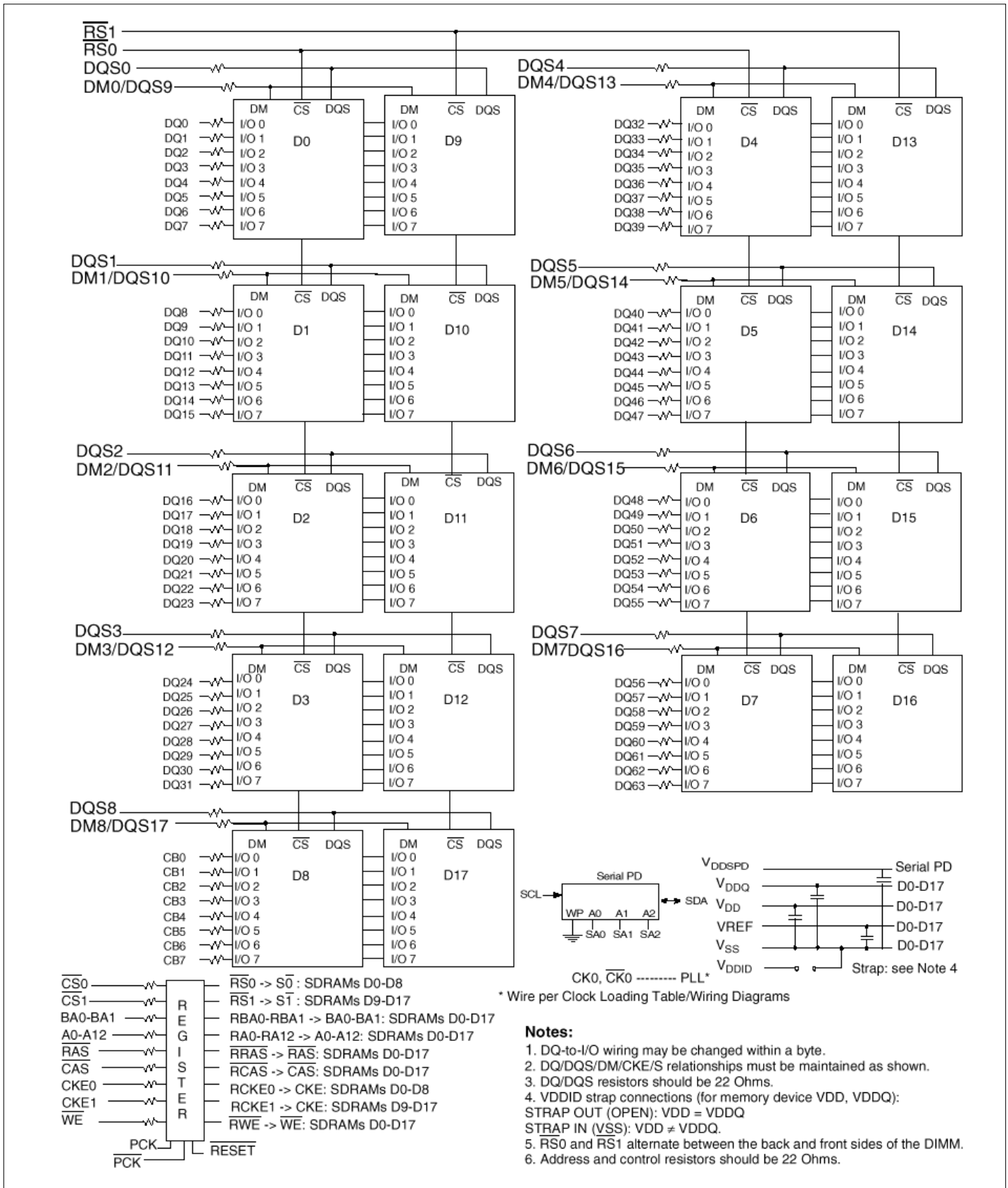
(Typically two
registers per DIMM)

120 Ohm

OUT'N'

C

Feedback

240 Ohm

PI74SSTTV16857
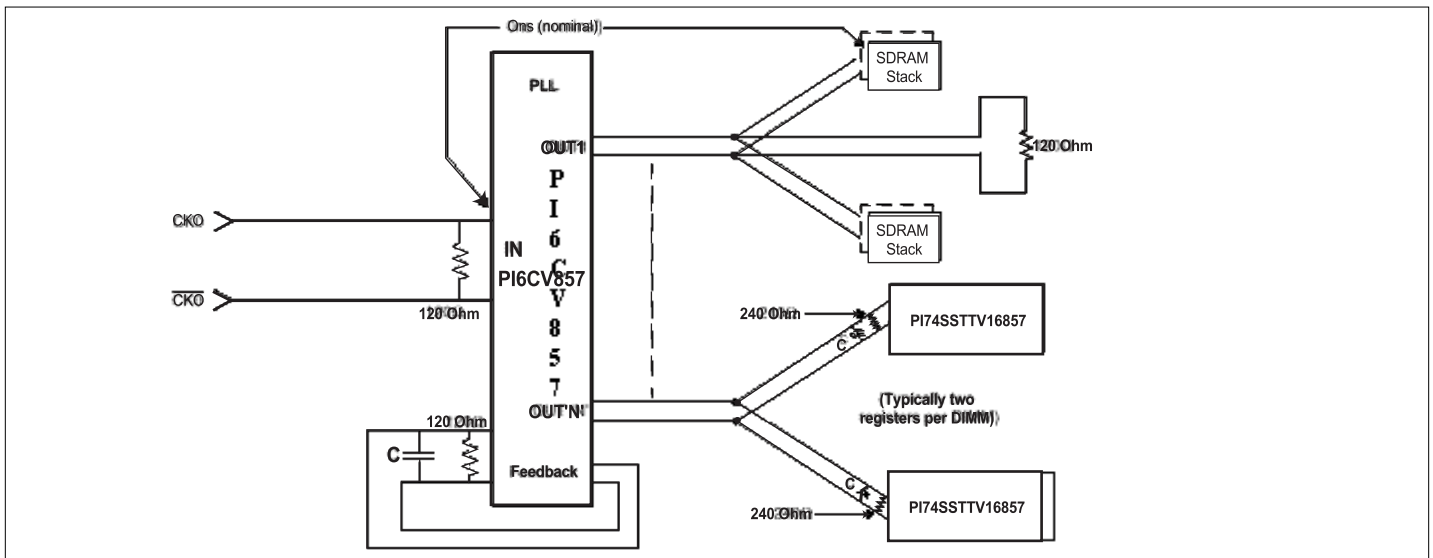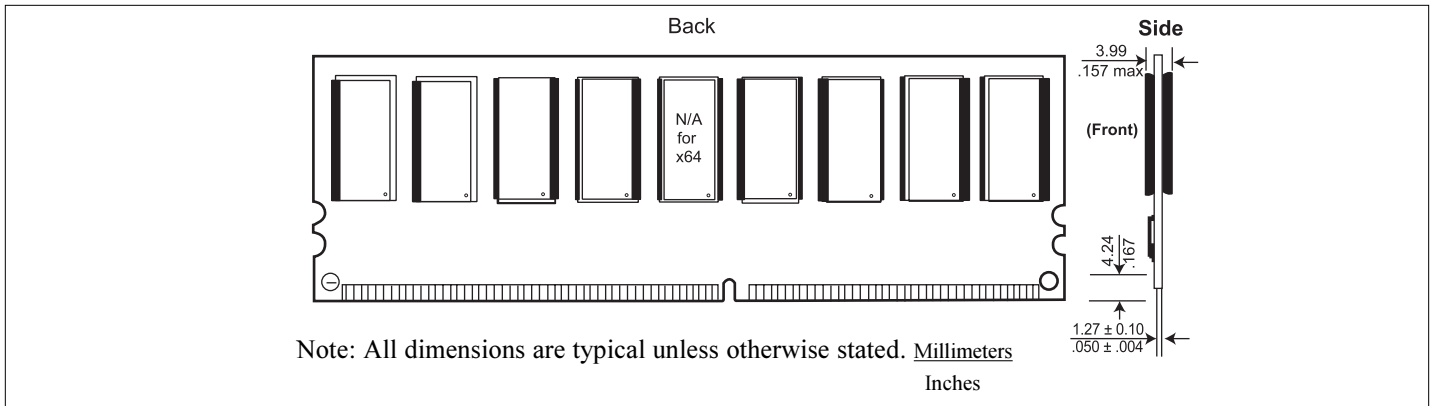
*Differential Clock Net Wiring (CK0, CK0)

1: The Clock delay from the input of the PLL Clock to the input of any SDRAM or Register will be set to O (nominal).
2: Input, output, and feedback clock lines are terminated from line to line a shown, and not from line to ground.
3: Only one PLL output is shown per output type. Any additional PLL outputs will be wired in a similar manner.
4: Termination resistors for the PLL feedback path clocks are located as close to the input pin of the PLL as possible.
5: Please check Application Note on Layout Decoupling Guidelines for PI6CV857 PLL Clock Driver for more information.

Notes:
1. DQ-to-I/O wiring may be changed within a byte.
2. DQ/DQS/DM/CKE/S relationships must be maintained as shown.
3. DQ/DQS resistors should be 22 Ohms.
4. VDDID strap connections (for memory device VDD, VDDQ):
STRAP OUT (OPEN): VDD = VDDQ
STRAP IN (VSS): VDD ≠ VDDQ.
5. RS0 and RS1 alternate between the back and front sides of the DIMM.
6. Address and control resistors should be 22 Ohms.

* Wire per Clock Loading Table/Wiring Diagrams

Registered DIMM Schematics Diagram: (x64 DIMM, populated as 2 physical banks of x8 DDR SDRAMS)

Critical Register Specifications: (JEDEC & Pericom Semiconductor Specification)

Register	Symbol	Parameter	Condition	TA = 0 - 70°C VDD = 2.5V±0.2V		Units	Notes
				Min.	Max.		
1:1 14-Bit and 1:2 13-Bit	tck	Clock Frequency		60	170	MHz	
	tpD	Clock to Output Time	30pF to GND and 50 Ohm to VTT	1.1	2.8	ns	
	tRST	Reset to Output Time		—	5	ns	
	tSL	Output Slew Rate	30pF to GND & 50Ohms to VTT/2	0.5	4	V/ns	
	tsu	Setup time, fast slew rate (Note 1 and 3)		—	0.75	ns	1,3
		Setup time, slow slew rate (Note 2 and 3)		—	0.9	ns	2,3
	th	Hold time, fast slew rate (Note 1 and 3)		—	0.75		1,3
		Hold time, slow slew rate (Note 2 and 3)		—	0.9		2,3
	$C_{IN}(ck)$	Clock input Capacitance		2.5	3.5	pF	
	C_{IN} (data)	Data Input Capacitance		2.5	3.5	pF	

Notes:
1. For data signal, input slew rate $\geq$ 1 V/ns.
2. For data signal, input slew rate $\geq$ 0.5 V/ns and < 1 V/ns.
3. For CLK and CLK signals, input slew rates are $\geq$ 1 V/ns.

Critical PLL Specifications: (JEDEC & Pericom Semiconductor Specification)

Device	Symbol	Parameter	Conditions	$T_A = 0.70°C$ $V_{DD} = 2.5V \pm 0.2V$		Units	Notes
				Min.	Max.		
1:10, 2.5Volt	I_{CK}	Operating Clock Frequency		60	170	MHz	
	F_{CK}	Application Clock Frequency		95	170	MHz	
	I_{SPE}	Static Phase Error	Application load	-50	50	ps	
	t_{SK}	Output Clock Skew	Application load	—	100	ps	
	t_{SL}	Output Slew Rate		1	3	V/ns	1,3
	$?_{S(per)}$	Period		-75	75	ps	2,3
	?	Cycle-to-Cycle					1,3
	?	Half Period		-100	-100		2,3
	t_{STAB}	PLL Stabilization Time			100	pF	
	C_{IN}	Input Capacitance		2.5	3.5	pF	

1. The PLL used on the registered DIMM needs to support SSC synthesizers with a Modulation Freq. of 30 to 50 KHz and a Clock Freq. Deviation of –0.5%. PLL designs should target the following values: *Greater than 1.2 MHz PLL loop bandwidth
*Less than –0.031 degrees of phase angle

2. The application load is defined in Differential Clock Net Structure.

3. Period jitter defines the largest variation in clock period, around a nominal clock period.

4. Period jitter and half-period jitter are independent from each other.

PI6CV857 AC Specifications

Switching characteristics over recommended Operating free-air temp. range(unless otherwise stated)

Parameters	Description	Avcc, V_{DDQ} = 2.5V ± 0.2V			Units
		Min.	Nom.	Max.	
tjit (cc)	Cycle-to-cycle jitter	-75		75	Ps
t(θ)	Static phase error (1)	-50	0	50	
tsk(0)	Output clock skew			100	
tjit(per)	Period jitter	-75		75	
tjit(hper)	Half period jitter	-100		100	
tsl(i)	Input clock slew rate(2)	1.0		2.0	V/ns
tsl(o)	Output clock slew rate(2)	1.0		2.0	
The PLL on the PI9CV857 is capable of meeting all the above parameters while Supporting SSC synthesizers (3) with the following parameters.					
SSC modulation frequency		30.00		50.00	KHz
SSC clock input frequency deviation		0.00		-0.50	%
PLL loop bandwidth			2		MHz
Phase Angle				-0.031	degrees

Notes:
1. Static phase Error does not include Jitter.
2. The slew rate is determined from the IBIS model and not from the test load.
3. The SSC requirements meet the Intel PC100 SDRAM Registered DIMM specification.

Conclusion:

In this Application Note we have described how to use the PI6CV857 PLL and the PI74SSTV16857 Register to design a Registered DDR DIMM module. We also described that Pericom PLL and Registers meet all JEDEC SPECIFICATION and have been qualified by leading Memory and DIMM vendors.

References:

1. DDR SDRAM Registered DIMM. Design Specification Rev 1.0 July 2000 by IBM, Micron Technology, and ServerWorks.
2. JEDEC STANDARD. JESD82 JULY 2000
3. PC2700 DDR Registered DIMM Status JEDEC Task Group Presentation March 2001.