User Guide for PI7C8154 Reference Board

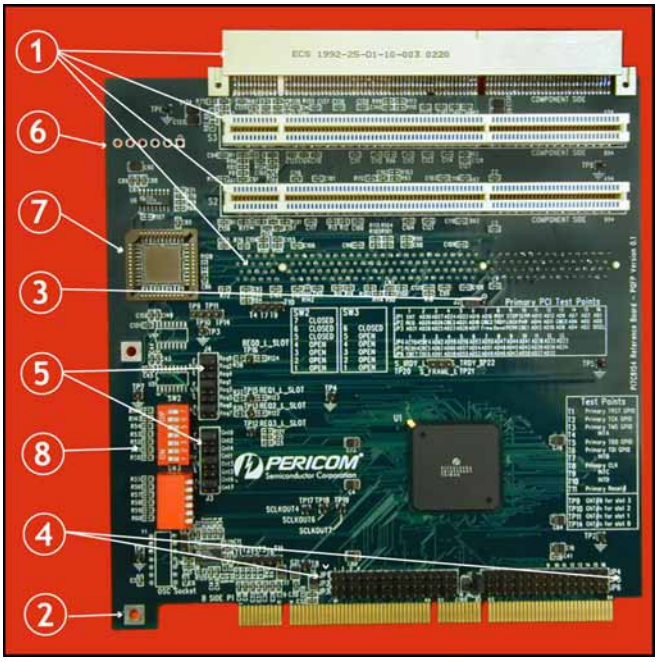
By Glenn Sanders

Introduction:

The Pericom PI7C8154 PCI to PCI bridge evaluation board demonstrates the bridge and allows testing of key features either before or during design / layout stages. The PI7C8154 PCI Bridge complies with PCI Local Bus specification 2.2, as well as PCI bridge specification 1.1

Quick start: (*photo of 8154 reference board*)

The numbers on the photo correspond to the text explanation on the right:



1) 3 standard and one straddle mount PCI connectors.
2) Pin 1 on the golden PCI edge connector faces left when looking down on the component (bridge IC).
3) Secondary bus Vio select : 3.3V or 5V
4) Headers for sampling signals on the primary PCI bus
5) GNT# and REQ# selection jumpers for the first 3 slots
6) Auxiliary power connector
7) External arbiter socket
8) Switches to set bus speed, control clocks, and some miscellaneous functions

---

This board comes **already configured** to support:

a) Primary PCI voltage (p_VIO) can be either 3.3V or 5V keying.
b) Secondary PCI voltage is set to 3.3V at J2
c) 66 or 33 MHz primary (i.e. M66EN is high)
d) 66 MHz secondary if all cards on the secondary bus are 66 MHz capable (i.e. secondary bus M66EN is high)
e) internal arbiter and internal clock source are enabled
f) no need to connect external power in most applications; the host PCI bus generally can power all 4 secondary bus slots.

Default and (*) important switch settings at a glance:

SW1: *there is no SW1*

SW2	Signal	Default	(Off=High, On=Low)
1	bpcce	Off	"off" Enables bus/power clock control function (**BPCCE is high**)
* 2	cfg66	**Off**	"**Off**" selects **Bridge is 66 MHz capable.**
3	p_M66en	Off	Reference board can be used in ***either*** 66 or 33 MHz motherboard slot. (**P_M66EN high**)
4	s_M66en	Off	"**Off**" sets Secondary bus is 66 MHz capable (**S_M66EN is high**)
* 5	reserved	On	Reserved, this switch is **not** used on the **8154.**
* 6	arbctrl	**On**	"On" Internal arbiter is selected
7	Not used	**Off**	No effect in either position (used for optional clock buffer)

SW3: **not used**. (This switch is used when locations U2 and U4 are stuffed).

Pericom Semiconductor ▪ 2380 Bering Drive ▪ San Jose, CA 95131
PH: 800-435-2336 FX: 408-435-1100
www.pericom.com

Defaults for Jumpers:

J1	Not connected	Normally, the reference board draws all power from the motherboard
J2	jumper **2-3**	**3.3 V** secondary bus **VIO**
J3	jump **2-10, 4-12, 7-15**	Assigns REQ#6 to slot 2, REQ#3 to slot 1, REQ#2 to slot 0
J4	jump **2-10, 4-12, 7-15**	Assigns GNT#6 to slot 2, GNT#3 to slot 1, GNT#2 to slot 0
J5	Not connected	
J6	Not connected	
J7	jumper **1-2**	edge connector on primary bus supplies p_VIO

BEFORE POWERING THE BOARD:

a) Speed selection:

Using the switch **SW2**, **choose the speed setting for the secondary bus** based upon the input primary bus speed:

SW2	33/33	66/33 secondary	66/66	Default
2-**2** CONFIG66	On	Off	Off	**Off**
2-**3** M66EN **pri**	On	Off	Off	**Off**
2-**4** M66EN **sec**	On	On	Off	**Off**

(Note: When primary bus M66EN is ***low*** (33 MHz), regardless of how the bridge reference board is configured the bridge will be dynamically set to 33 MHz primary and 33 MHz secondary, with S_M66EN driven low by the bridge.)

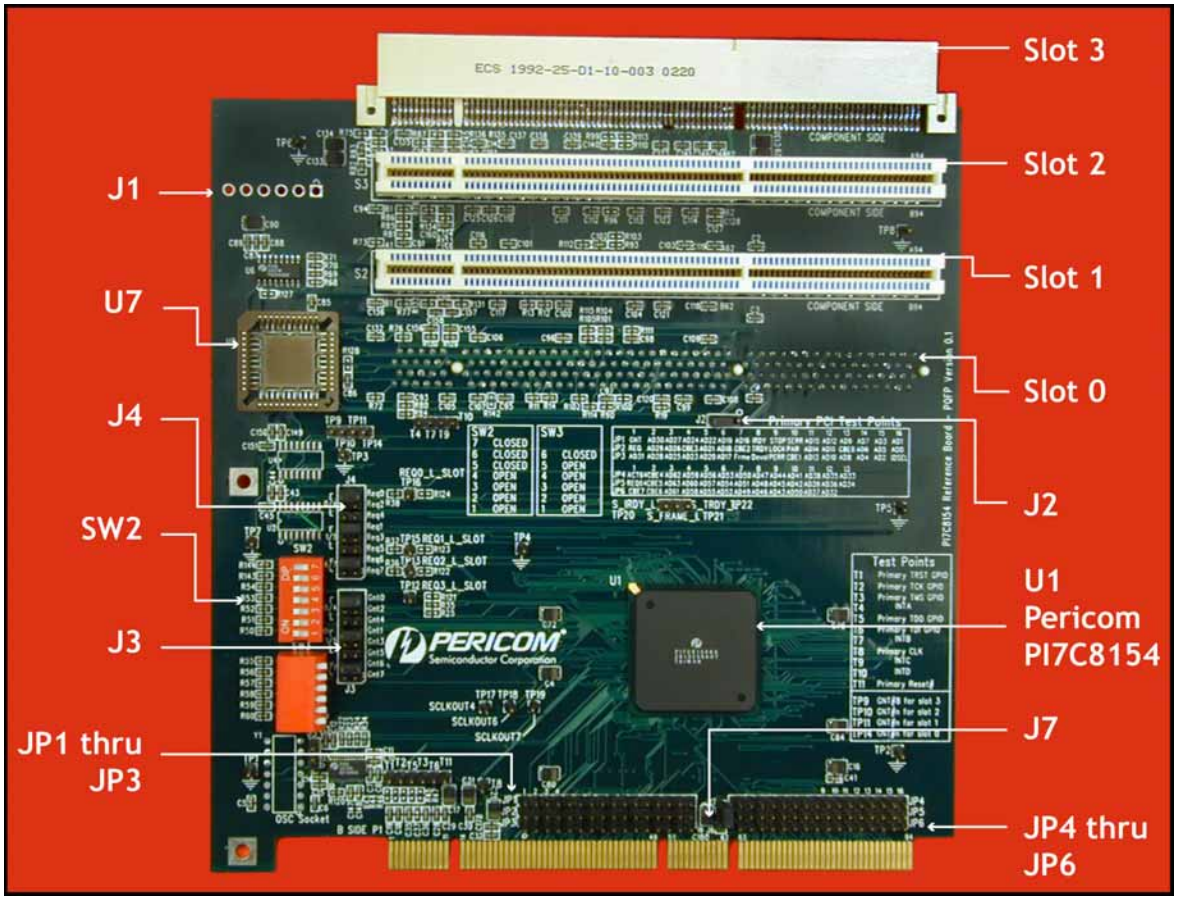
b) **Seat the board into a PCI slot on the main system board**. Looking from the front of the motherboard, the small lip on our reference board points to the back of the motherboard, and the component side with the PI7C8154 bridge chip is on the left hand side. Normally you won't need to connect power to the reference board through header J1. Otherwise the motherboard PCI connector is adequate to powering the board with a few add-in cards.

c) **Connect any PCI cards desired on the secondary PCI bus**. For all PCI connectors on our reference board, when looking down onto the bridge IC, pin 1 is on the left side of the board. Notice that the external arbiter socket on the front and the auxiliary power connector on the back are closest to PCI connector pin 1. This also applies to the top mounted "straddle" connector. Putting in any cards backwards will short 5V to ground through the PCI connector. Also each PCI connector has "A1", "B1", "A62", "B62" at the 4 corners of each slot, as a reminder where pin 1 is on each connector.

At this point, the Pericom PI7C8154 reference board is ready for you to use.

Pericom Semiconductor ▪ 2380 Bering Drive ▪ San Jose, CA 95131
PH: 800-435-2336 FX: 408-435-1100
www.pericom.com

Components and Jumper Reference:



U1 Pericom 8154 Bridge
U2 Not stuffed
U3 PI6C2410 Clock Buffer
U4 Not stuffed
U6 PI3B3257-W Mux/Demux bus switch
U7 Socket for optional external arbiter

SW2 Speed, options selection
SW3 Secondary clock control
J1 Auxiliary power
J2 Secondary bus Vio select
J3 Grant# selection for slots 1..3
J4 Req# selection for slots 1..3
J5 Not used
J6 Forces 3.3V ***detect*** for primary Vio
J7 Primary Vio follows motherboard

TABLES:

a) Tables on the front remind shipping defaults for SW2, SW3.
b) The right side of the board has a silk-screened table of test points T1..T11 and TP9..11, TP14.
c) Right side of board has JP1 to JP6 list

PH: 800-435-2336 FX: 408-435-1100
Pericom Semiconductor • 2380 Bering Drive • San Jose, CA 95131
www.pericom.com

Switch Listing

SW1: does not exist

SW2	Signal	Default	Full Description
1	**bpcce**	Off	"off" Enables bus/power clock control function (**BPCCE is high**) "on" puts a low at this signal. (This influences turning off PCI clocks under ACPI power management.)
2	**cfg66**	**Off**	"**Off**" selects **Bridge is 66 MHz capable.** When "On", the bridge is set to 33 MHz on **both** primary and secondary buses.
3	**p_M66en**	Off	"**Off**" sets **P_M66EN high**. Reference board can be used in either 66 or 33 MHz motherboard slot. "On" sets P_M66EN to low (and thus 33 MHz only mode).
4	**s_M66en**	Off	"**Off**" sets Secondary bus is 66 MHz capable (**S_M66EN is high**) "On" forces 33 MHz secondary bus even if primary bus is 66 MHz. (S_M66EN low)
5	**reserved**	**On**	Reserved, this switch is **not** used on the 8154.
6	**arbctrl**	**On**	"On" Internal arbiter is selected; "off" selects external arbiter but other changes needed also to activate external arbiter. See page 5.
7	**Not used**	Off	Off sets external clock buffer to 1:1 mode; On sets output of U3 to 2x Clock-in. (But external clock buffer is not used unless the board is modified.)

SW3 (only valid when **U2** and **U4** are **stuffed**)

1	Off	Turns off sclock**4**; "on" requests the clock to be turned on even if no device uses it
2	Off	Turns off sclock**5**; "on" requests the clock to be turned on even if no device uses it
3	Off	Turns off sclock**6**; "on" requests the clock to be turned on even if no device uses it
4	Off	Turns off sclock**7**; "on" requests the clock to be turned on even if no device uses it
5	Off	Turns off sclock**8**; "on" requests the clock to be turned on even if no device uses it
6	**On**	**Feedback clock is enabled.** *Turning this switch off hangs the secondary bus.*

(Normally, at power on, the 2 components U2 and U4 report which secondary PCI connectors have the PRSNTx_1 and PRSNTx_2 pins pulled low, implying there is a device at that location and it's power requirements. Switching 1 through 5 on simply forces the unused clocks on. The Feedback clock MUST be turned on, if our bridge is generating the secondary bus clock outputs.) However as shipped, Mask_In is low and thus ***all clocks are enabled***.

Jumper Block Listing

J1 **external power** connector. From pin 1 on the innermost pin of this location,
[+5V, +3.3V, +3.3V, ground, ground, ground]
This does NOT need to be connected in order to use the bridge.

J2 **Vio select** 3-2 **3.3V** (left) 1-2 **5V** (right)
This sets Vio for the **secondary** bus. The PCI bridge will drive control signals to this voltage on the secondary bus. This should already be configured for you.

J3 **Grant assignments** to secondary PCI bus connector slots 1, 2, and 3.
The 3 ordinary PCI connectors have GNT# (and REQ#) assigned by jumpers.
Notice that to the left of these are stenciled brackets; you may select only ONE of the possible jumper positions within a pair of brackets [ ]
Thus, on our reference board, for the slot closest to the bridge, (which is mounted on the ***back*** of the board)
{***Gnt0*** OR ***Gnt2*** OR ***Gnt4*** } *jump one only of these 3 choices*
we can monitor the grant signal for this slot at TP14.

For the next slot up {***Gnt1*** OR ***Gnt3*** OR ***Gnt5***} *jump only 1 of the 3 choices*
Monitor at TP 11

For the third slot up {***Gnt6*** OR ***Gnt7***} *jump only 1 of the two choices*
Monitor at TP10

Top slot is fixed at ***Gnt8***. Monitor at TP9

J4 Req assignments
These must match the positions chosen in J3.!
From bottom slot to top,
{***Req0*** or ***Req2*** or ***Req4***} monitor at TP16
{***Req1*** or ***Req3*** or ***Req5***} monitor at TP15
{***Req6*** or ***Req7***} monitor at TP13
fixed at ***Req8*** top slot monitor at TP12

J5 Not used.

J6 3.3V pin
J6 allows a method to **force** the bridge to use 3.3V signaling for communicating with a 66 MHz motherboard without disturbing the motherboard's Vio, which is only useful when an older motherboard has a 66 MHz PCI bus keyed for 5V. (*This signal is NOT bused into the motherboard Vio.)*

J7 P_Vio select
The topmost pin at **J7** is **P_Vio** from the motherboard; the center pin goes to our bridge.

Pericom Semiconductor ▪ 2380 Bering Drive ▪ San Jose, CA 95131
PH: 800-435-2336 FX: 408-435-1100
www.pericom.com

Primary bus test points **JP1, JP2, JP3**:
These allow a logic analyzer or oscilloscope to monitor signals on the path between the 8154 and primary bus.
There are 3 rows of 16 header pins each, labeled JP1, next JP2, next JP3: (and likewise JP4 through JP6)

	1	2	3	4	5	6	7	8
JP1	GNT	AD30	AD27	AD24	AD22	AD19	AD16	IRDY
JP2	REQ	AD29	AD26	CBE3	AD21	AD18	CBE2	TRDY
JP3	AD31	AD28	AD25	AD23	AD20	AD17	Frame	Devsel
JP4	ACK64	CBE4	AD62	AD59	AD56	AD53	AD50	AD47
JP5	REQ64	CBE5	AD63	AD60	AD57	AD54	AD51	AD48
JP6	CBE7	CBE6	AD61	AD58	AD55	AD52	AD49	AD46
	9	**10**	**11**	**12**	**13**	**14**	**15**	**16**
JP1	STOP	SERR	AD15	AD12	AD9	AD7	AD3	AD1
JP2	LOCK	PAR	AD14	AD11	CBE0	AD6	AD5	AD0
JP3	PERR	CBE1	AD13	AD10	AD8	AD4	AD2	Idsel
JP4	AD44	AD41	AD38	AD35	AD33	.	.	.
JP5	AD45	AD42	AD39	AD36	AD34	.	.	.
JP6	AD43	AD50	AD37	AD32	.	.	.	.

(A copy of this table is present on the right hand side of the component side of the reference board.)
Header locations marked with a "." are empty and are "no connect".

Test Points Description:

These allow convenient sampling of signals by logic analyzer or oscilloscope:

T1 Primary TRST# GPIO
T2 Primary TCK GPIO
T3 Primary TMS GPIO
T4 INTA#
T5 Primary TDO GPIO
T6 Primary TDI GPIO
T7 INTB#
T8 Primary bus **clock**
T9 INTC#
T10 INTD#
T11 Primary bus Reset#

TP1 ground
TP2 ground
TP3 ground
TP4 ground
TP5 ground
TP6 ground
TP7 ground
TP8 ground
TP9 Gnt to top (4th) slot
TP10 Gnt to 3rd slot

TP11 Gnt to 2nd slot
TP12 Req to 4th (top) slot
TP13 Req to 3rd slot
TP14 Gnt to 1st (bottom) slot
TP15 Req to 2nd slot
TP16 Req to 1st (bottom) slot

OPTIONAL External Arbiter:

For **internal** arbiter, **SW2 -6** is **ON** (closed)**.** This is the **default.**

For **external** arbiter, a number of changes are made to the board:

Remove the 0-Ohm resistors at R35, R36, R37, R38
Stuff 0-Ohm resistors into R121, R122, R123, R124, R127, R128
Verify that **J4 -8** (*assigning REQ#0 to secondary bus slot 0*) is **open.**
Instead, put the jumper at J4 -7.
Verify that **J3 -8** (*assigning GNT#0 to secondary bus slot 0)* is **open.**
Instead, put the jumper at J3 -7.
Finally, stuff socket **U7** with an appropriately programmed **Xylinx XC9572 CPLD**
(availability of code TBD)

Where to find more information:

Schematics, bill of materials, gerber files, and technical assistance are available at our website www.pericom.com