

Designing a high-speed differential signal interface using the PI2EQX Re-Driver family

By Paul Li

Introduction

The PI2EQX family was developed using Pericom's cutting-edge technology to boost the high-speed differential signals traveling in traces or cables in high-performance system interface protocols such as PCI Express, Fibre Channel, Rapid I/O at 2.5Gbps (using PI2EQX4401 and PI2EQX4402), XAUI, InfiniBand, SATA, SATA-II, SAS applications from 3.0Gbps to 3.2Gbps (using PI2EQX3201 and PI2EQX3302),

and many other high speed differential signals in the bandwidth ranging from 1.5Gbps to 3.5Gbps.

The PI2EQX family has flexible and programmable settings for its equalization, de-emphasis and switch to fit various lengths of trace and cable. It has programmable equalization from 0db, 1.5db, 2.5db, 3.5db, 4.5db, 5.5db, 6.5db to 7.5db; programmable signal-swing from 0.8x, 1.0x, 1.2x to 1.4x and programmable de-emphasis at 0db, -2.5db, -3.5db and -4.5db.

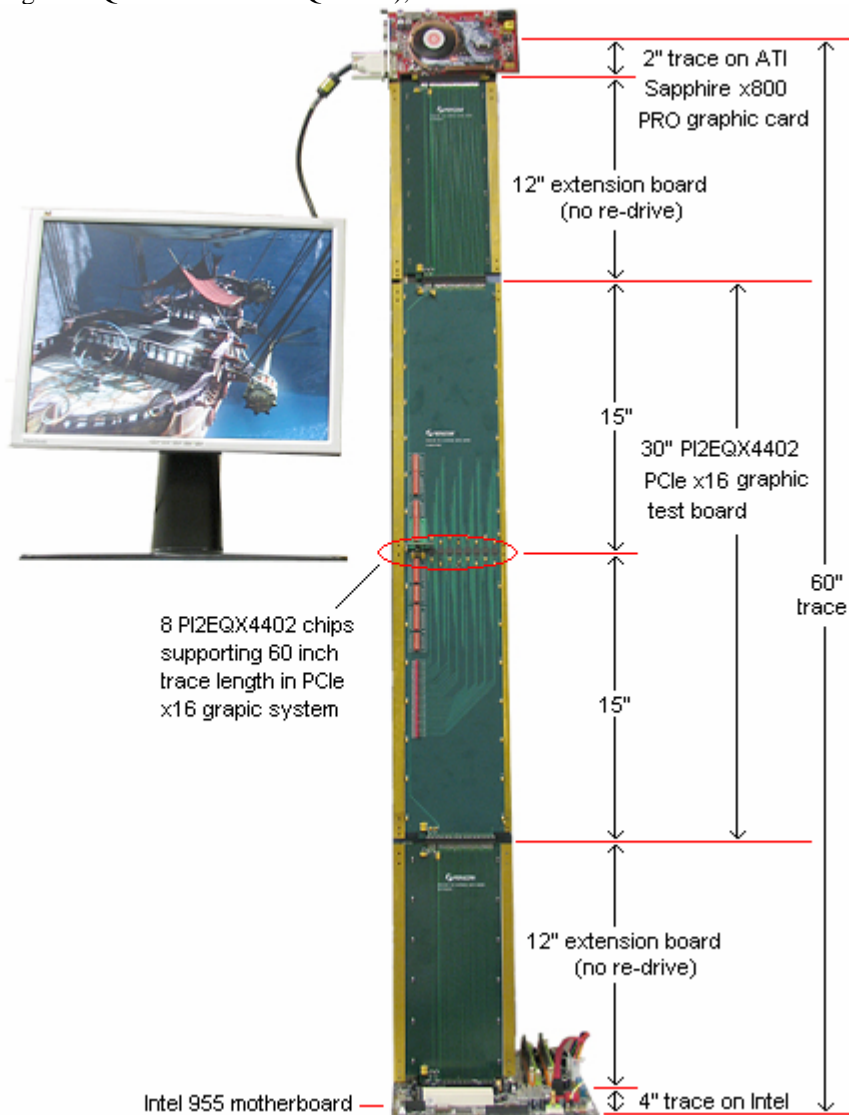


Figure 1: PI2EQX4402 system test board for PCI Express x16 graphic application supporting 60" trace length

Beating the distance challenge

High-speed differential signal interfaces dominate today's high-performance system architectures because of their ultra-high data rate throughput, low power consumption, facilitation of PCB layout, and PCB cost reduction. The challenge is that at the bandwidth of 2.5Gbps to 3.2Gbps, the differential signals are tremendously attenuated and distorted when traveling through a long trace or cable. Pericom Semiconductor has developed a Re-Driver device with programmable de-emphasis and equalization that will boost the signal over long distances, and will recover the distorted signal received from a long trace or cable. The example in Figure 1 uses 8 pieces of Pericom PI2EQX4402 Re-Driver chips for the PCI Express x16 graphic system supporting a total of 60 inches of trace length.

Figure 2 is the compliance test results using the SigTest 2.0 software and the CLB (Compliance-test Load Board) test fixture from PCI-SIG, which is developed by Intel. The Rx eyes measured at the upper graphic card connector shown on page 1 in Figure 1 are wide opening with fairly low jitter after 60" trace and 4 connectors and meet the PCI Express compliance test specification.

Different approaches to extend a trace or cable include using a PCI Express Bridge or a Packet Switch, or by using the PI2EQX Re-Driver family. PI2EQX is an optimized cost-to-function solution for trace and cable extension applications.

A PCI Express Bridge or a PCI Express Packet Switch will cost much more than using the PI2EQX family, and the extended functions in the PCI Express Bridge or Packet Switch may not be fully used if the application is only for trace and cable extension.

The design cycle and design effort of using a PCI Express Bridge or a PCI Express Packet switch is also a great deal longer than using a PI2EQX re-driver, if the application is only for trace and cable extension.

Most PCI Express Bridge and Packet Switches have fixed de-emphasis at 3.5db with no equalization, while the PI2EQX Re-Driver family has flexible programmable signal swing, de-emphasis, and equalization to fit any lengths of trace or cable within the spec and guaranteed passing of the PCI Express compliance test.

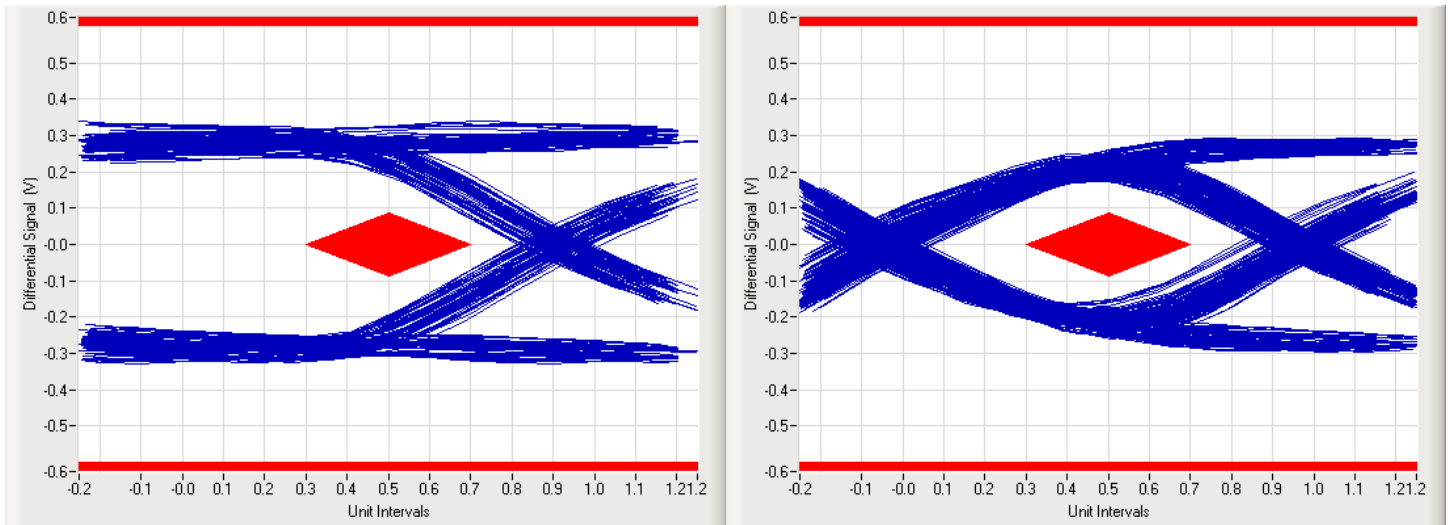


Figure 2: The non-transition (left) and transition (right) eyes measured at the end of the 60" trace in the system test setup shown in Figure 1

The excellent equalization of the PI2EQX family

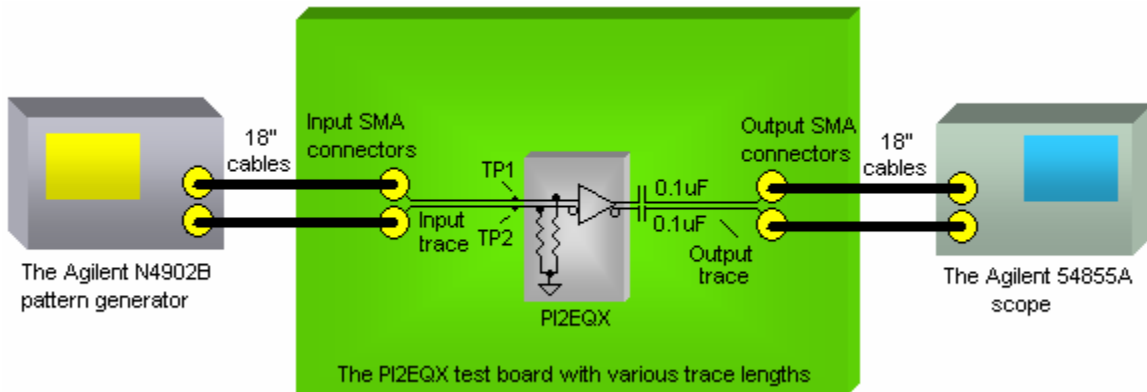


Figure 3: The Pericom PI2EQX4402 and PI2EQX3202 test board

The eyes in Figure 4 are the results of 35" input trace and 1.9" output trace tested using the PI2EQX4402 test board in Figure 3, which has variety trace lengths from 1.9" to 40" at input and output for the signal integrity test.

Figure 4 shows that the messy input eyes measured at TP1 and TP2 are very well recovered at the output of the PI2EQX4402

because of the 7.5db equalization in the input of PI2EQX4402. These eyes were measured using the SigTest 2.0 software downloaded from PCI-SIG web site and it passed the PCI Express Tx compliance test spec, after the 2.5Gbps K28.5 pattern signal from the Agilent pattern generator traveling through 35" traces.

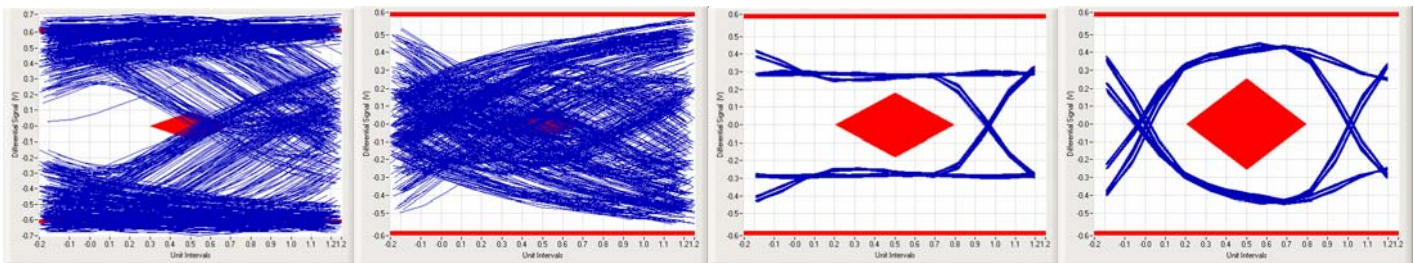


Figure 4: The left non-transition and transition eyes were measured at the TP1 and TP2 with 35" input trace, the right two eyes were measured at the output SMA connectors with 1.9" trace as in Figure 3. Test settings: equalization = 7.5db, de-emphasis = -3.5, swing = 1x.

The eyes in Figure 5 were measured in the same trace length and using the same test board as for the eyes in Figure 4, but with different equalization settings to demonstrate the linearity and efficiency of the equalization of the PI2EQX4402. By comparing the results difference versus the equalization settings from 7.5db (in Figure 4), 5.5db, 3.5db 1.5db and 0db

(Figure 5), we can see that the jitters are increasing from lowest to highest in a linear degree. This test proves the efficiency of the equalization of PI2EQX4402, and thus provides us a basis to set the equalization against different trace and cable lengths in different applications using various trace and cable lengths.

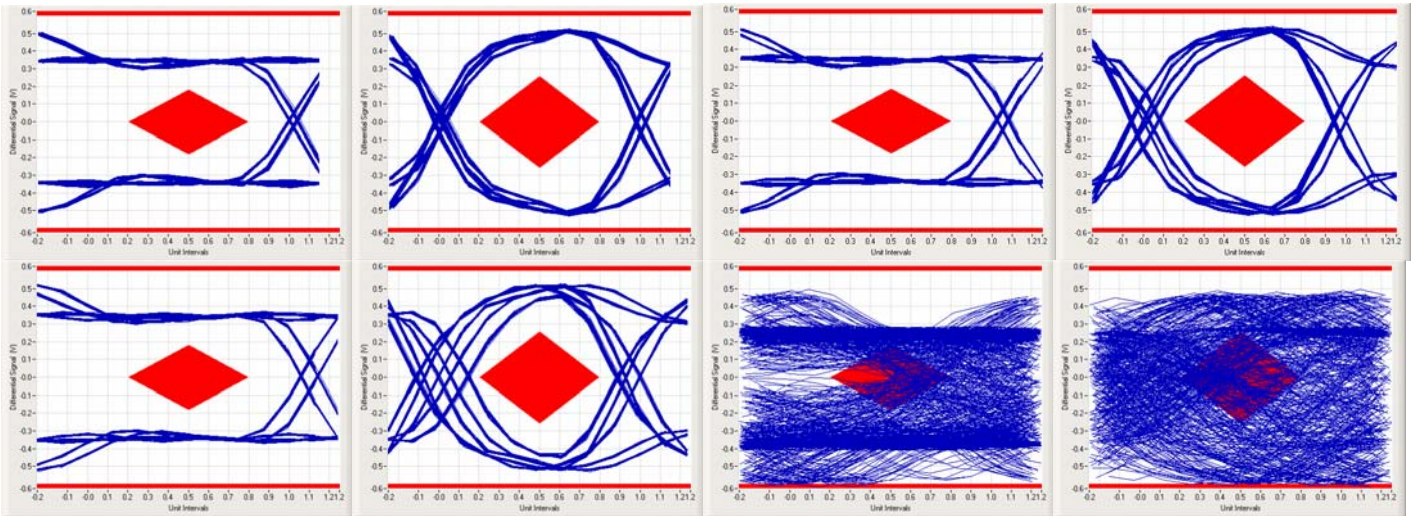


Figure 5: The eyes for the equalization settings of 5.5db, 3.5db 1.5db and 0db, from left to right and top to bottom. All measured at the output SMA connectors of the PI2EQX4402 with 35" input and 1.9" output trace as in Figure 3 De-emphasis = -3.5, swing = 1x

Applications using PI2EQX family

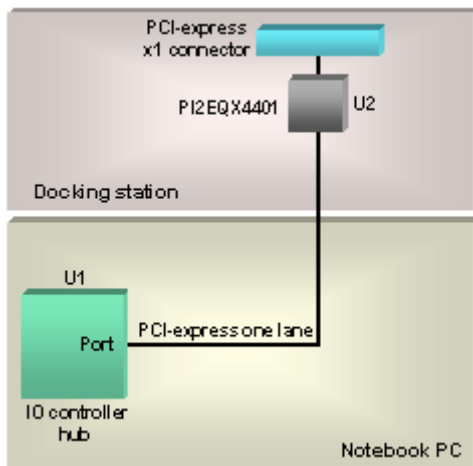


Figure 6: Using PI2EQX4401 for signal re-conditioning in the notebook and docking station

Before using the PI2EQX4401 U2 as in Figure 6, the PCI Express signal at the PCI Express x1 connector in the docking station will become weak and fail the compliance test after the signal traveling the long trace between U1 and the PCI Express x1 connector. The PI2EQX4401 in the docking station re-conditions the signal from U1 to meet the PCI Express compliance test on the PCI Express x1 connector.

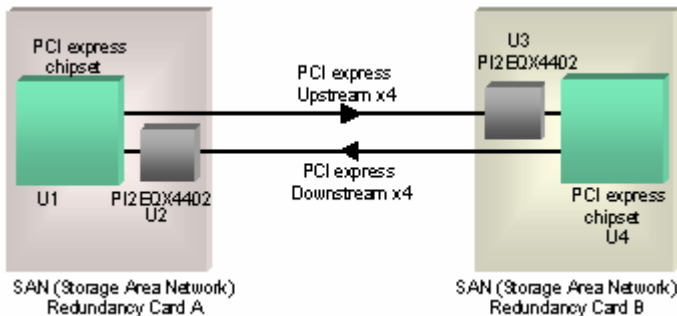


Figure 7: Using the PI2EQX4402 for the SAN (Storage Area Network) redundancy application

In Figure 7, the two SAN redundancy cards with 4 lanes PCI Express interface are 35” away from each other and the two PI2EQX4402 chips U2 and U3 are deployed at the input of PCI Express chipsets U1 and U4. Thus, the equalization in the input of the PI2EQX4402 will correct the re-conditioning of the messy deterministic jitters at the input of the PI2EQX4402 and the output of the PI2EQX4402 will become clear and pass the PCI Express compliance test.

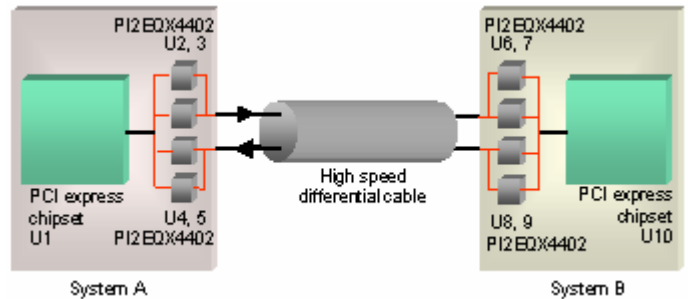


Figure 8: Using PIEQX4402 for high-speed differential cable between two systems A and B

In Figure 8, the systems A and B are using a high-speed differential cable, 3 meter to 7 meter, for PCI Express interface. The PI2EQX4402 chips U2, U3, U6 and U7 will guarantee that the signals at the input of the U1 and U10 will pass the PCI Express compliance test.

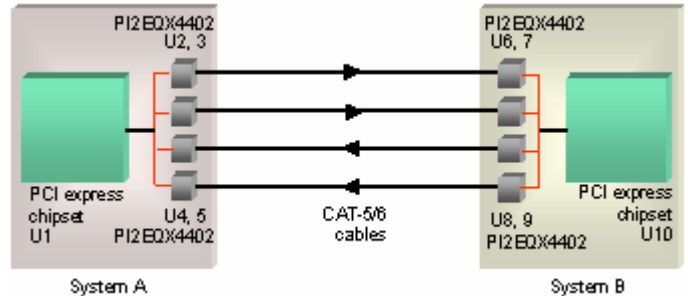


Figure 9: Using PIEQX4402 for CAT-5 cables between two systems A and B

In Figure 9, the PCI Express x8 systems A and B are using CAT-5 (or CAT-6) cables, 2 meter to 5 meter depending on the quality of the cables, while guarantee passing the PCI Express compliance test at the input of the U1 and U10. This combining of PI2EQX4402 and CAT-5 cable will provide an optimized cost reduction solution for cable applications. For instance, a dedicated high-speed differential cable with 16 pairs for the PCI Express x8 application in Figure 8 will easily cost above \$250, which is almost impossible for PC or other commodity markets. But using CAT-5 cables at \$3 each plus 8 chips of PI2EQX4402 as in Figure 9 will only cost \$40 or less, which is affordable for any kind of application, including consumer markets.

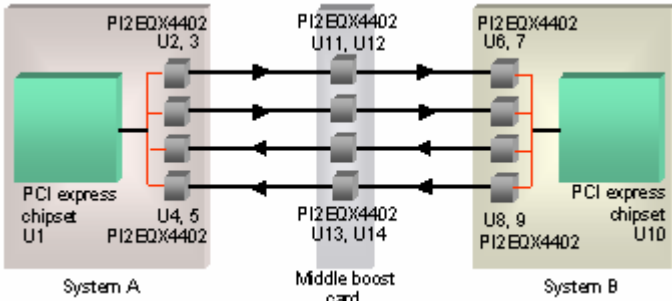


Figure 10: A middle card with PI2EQX4402 for the cable extension

If further trace and cable extension is needed, a middle card with PI2EQX4402 can be used as in Figure 10 to further extend the cable length.

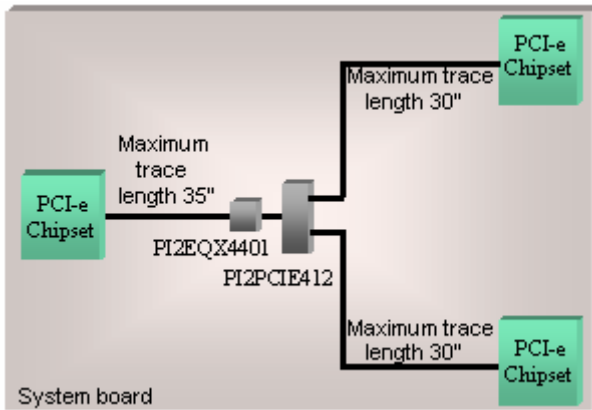


Figure 11: Using PI2PCIE412 with PI2EQX4402 for Mux applications

Figure 11 shows the application using PI2EQX4402 combined with Pericom 2:1 Mux PCI Express switch PI2PCIE412. PI2PCIE412 is designed using Pericom revolutionary

technology and is the first PCI Express switch in the market with the highest performance in industry. The PI2PCIE412 switch can pass the Rx PCI Express compliance test with total 16" trace as specified in the PCI Express specification. But for applications with trace longer than 16", a PI2EQX4402 can be used as in Figure 11 to guarantee that the Rx eyes at the inputs of the PCI Express chipsets will pass the PCI Express compliance test.

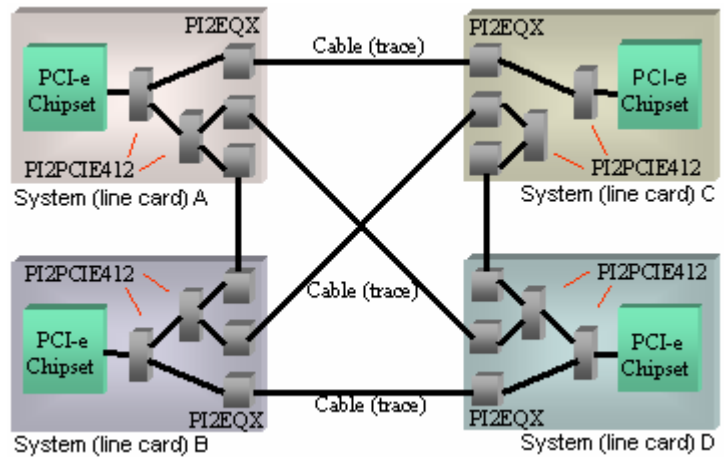


Figure 12: Using PI2EQX4402 for the cross-point system application

The application in Figure 12 is a conceptual block diagram to bring up a brainstorm of how to use the PI2EQX4402 combined with the PI2PCIE412 for complex system designs. The real applications may vary with different combinations of using the PI2EQX4402 and PI2PCIE412, but using the similar concept as in Figure 12.

The recommended settings of the PI2EQX Re-Driver family

1. The settings of PI2EQX4401 and PI2EQX4402 for various input trace lengths

Input trace lengths (all output traces are 1.9" or less)	For PI2EQX44XX, PCI Express 2.5Gbps			Non transition and transition eyes test results
	Swing	De-emphasis	Equalization	
1.3"	1x	-3.5db	0db	Figure 13, top-left
13"	1x	-3.5db	1.5db	Figure 13, top-middle
19"	1x	-3.5db	2.5db	Figure 13, top-right
24"	1x	-3.5db	3.5db	Figure 13, middle-left
30"	1x	-3.5db	5.5db	Figure 13, middle-middle
35"	1x	-3.5db	7.5db	Figure 13, middle-right
40"	1x	-4.5db	7.5db	Figure 13, bottom

Table 1: The settings for PI2EQX44XX family versus various input trace lengths. For cable applications, use the same settings in Table 1 and multiply the trace length by 2.5 to 5, depending on the cable type.

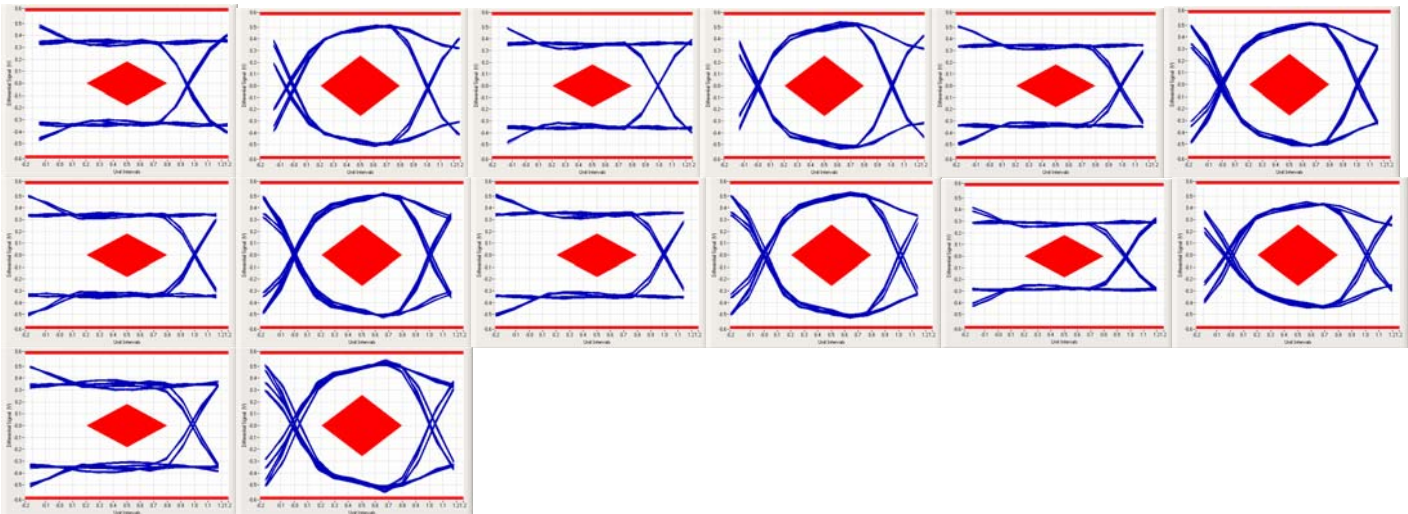


Figure 13: The Tx eye compliance test results of the PI2EQX44XX settings in Table 1 against various input trace lengths, measured using the PI2EQX4402 test board in Figure 3.

Figure 13 shows the eyes test results using the settings recommended in Table 1. Please refer to Table 1 for the settings of each eye patterns. We can see that all the eyes in Figure 13 passed the PCI Express compliance test.

2. The settings of PI2EQX44XX for various output trace lengths

Output trace lengths (all the input traces are 1.3" or less)	For PI2EQX44XX, PCI Express 2.5Gbps			Non transition and transition eye pair test results
	Swing	De-emphasis	Equalization	
16"	1x	-3.5db	0db	Figure 14, left
24"	1x	-3.5db	0db	Figure 14, middle
32"	1x	-4.5db	0db	Figure 14, right

Table 2: The settings for PI2EQX44XX versus various output trace lengths. For cable applications, use the same settings in Table 2 and multiply the trace length by 2.5 to 5, depending on the cable type.

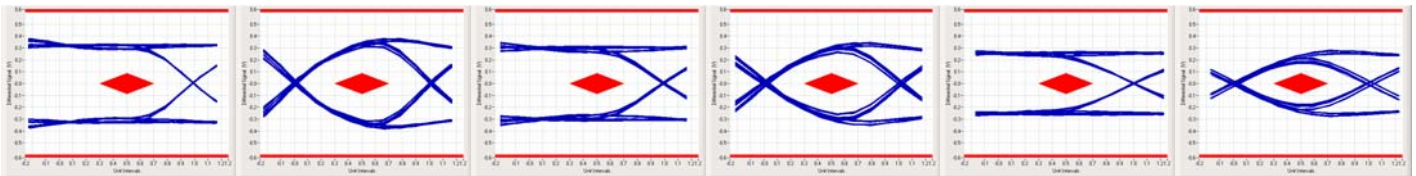


Figure 14: The Rx eye compliance test results of the PI2EQX44XX settings in Table 2 against various output trace lengths, measured using the PI2EQX4402 test board in Figure 3

Figure 14 shows the eyes test results using the settings recommended in Table 2. Please refer to Table 2 for the settings of each eye patterns. We can see that all the eyes in Figure 14 passed the PCI Express compliance test.

3. The settings of PI2EQX44XX for various input and output trace length combinations

Input and output trace lengths	For PI2EQX44XX, PCI Express 2.5Gbps			Non transition and transition eye pair test results
	Swing	De-emphasis	Equalization	
16" - 16"	1x	-3.5db	3.5db	Figure 15, left
24" - 24"	1x	-4.5db	4.5db	Figure 15, middle
31" - 29"	1x	-4.5db	7.5db	Figure 15, right

Table 3, the settings for PI2EQX44XX versus various input and output trace length combinations. For cable applications, use the same settings in Table 3 and multiply the trace length by 2.5 to 5, depending on the cable type.

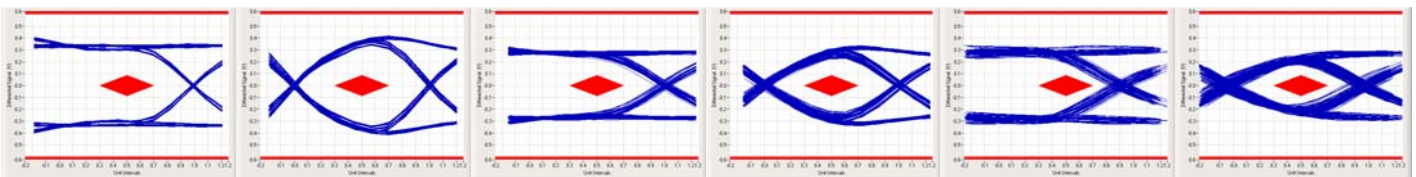


Figure 15, the Rx eye compliance test results of the settings in table-3 against various length combinations, measured using the test board in Figure 3 for the 16"-16" and 24"-24", and used the test setup in Figure 1 for the 31" - 29" traces

Figure 15 shows the eyes test results using the settings recommended in Table 3. Please refer to Table 3 for the settings of each eye patterns. We can see that all the eyes in Figure 15 passed the PCI Express compliance test.

The recommended settings of PI2EQX32XX for XAUI, InfiniBand, SATA-II, SAS, Fibre Channel, Rapid IO, Hyper transport and other applications

1. The settings for various input trace lengths

Input trace lengths (all the output traces are 1.9" or less)	For PI2EQX32XX, 3.0Gbps - 3.2Gbps (For XAUI, InfiniBand, SATA-II, SAS, Fibre Channel, Rapid IO, Hyper transport, etc)		
	Swing	De-emphasis	Equalization
1.3"	1x to 1.4x	-3.5db	0db
13"	1x to 1.4x	-3.5db	1.5db
19"	1x to 1.4x	-3.5db	2.5db
24"	1x to 1.4x	-3.5db	3.5db
30"	1x to 1.4x	-3.5db	5.5db
35"	1x to 1.4x	-3.5db	7.5db

Table 4, the settings for PI2EQX32XX versus various input trace lengths. For cable applications, use the same settings in table-4 and multiply the trace length by 2.5 to 5, depending on the cable type.

2. The settings for various output trace lengths

Output trace lengths (all the input traces are 1.3" or less)	For PI2EQX32XX, 3.0Gbps - 3.2Gbps (For XAUI, InfiniBand, SATA-II, SAS, Fibre Channel, Rapid IO, Hyper transport, etc)		
	Swing	De-emphasis	Equalization
16"	1x to 1.4x	-3.5db	0db
24"	1x to 1.4x	-3.5db	0db
32"	1x to 1.4x	-4.5db	0db

Table 5, the settings for PI2EQX32XX versus various output trace lengths. For cable applications, use the same settings in table-5 and multiply the trace length by 2.5 to 5, depending on the cable type.

3. The settings for various input and output trace length combinations

Input and output trace lengths	For PI2EQX32XX, 3.0Gbps - 3.2Gbps (For XAUI, InfiniBand, SATA-II, SAS, Fiber Channel, Rapid IO, Hyper transport, etc)		
	Swing	De-emphasis	Equalization
16" - 16"	1x to 1.4x	-3.5db	3.5db
24" - 24"	1x to 1.4x	-4.5db	4.5db
30" - 30"	1x to 1.4x	-4.5db	7.5db

Table 6, the settings for PI2EQX32XX versus various input and output trace lengths. For cable applications, use the same settings in table-6 and multiply the trace length by 2.5 to 5, depends on the cable type.

The generic topology and layout guidance for PCI Express signal PCB

1. The trace width and clearance

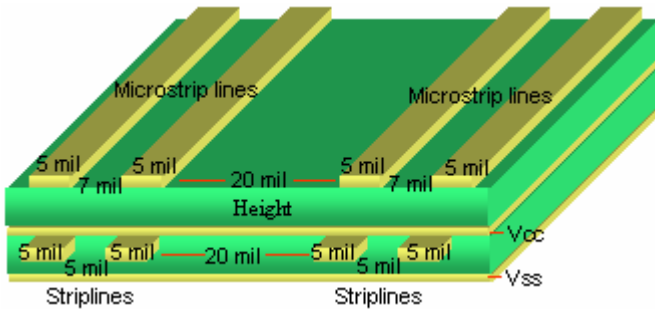


Figure 16: The trace width and clearance

- The trace length miss-matching shall be less than 5 mils for the “+” and “-” traces in the same pairs
- Match the length between the pairs less than 3 inches
- Use wider trace width, with 100-ohm differential impedance, to minimize the loss for long routes
- More pair-to-pair spacing for minimal crosstalk
- Target differential Z_0 of 100-ohm $\pm 20\%$

2. The PCB layers stack-up

- No new PCB technology required. Use FR4 is fine.
- Using standard 4 to 8 layers stack-up with 0.062 inch thick PCB.
- For micro strip lines, using 1/2 OZ Cu plated is ok.
- For strip line in 6 plus players, using 1 OZ Cu is better.

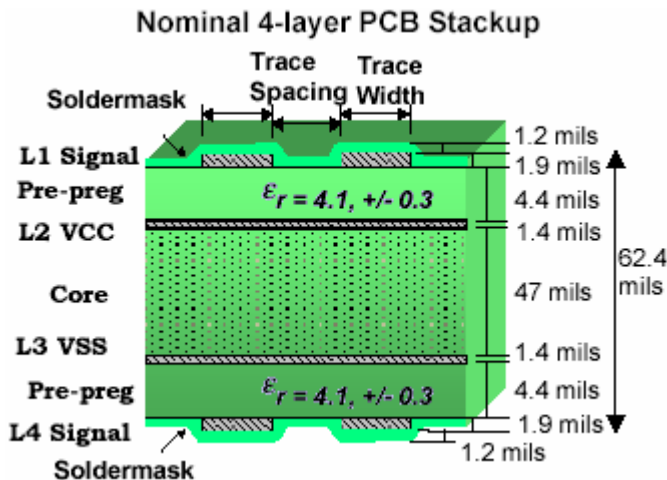


Figure 17: The PCB layers stack-up

3. The layout guidance for the trace routings

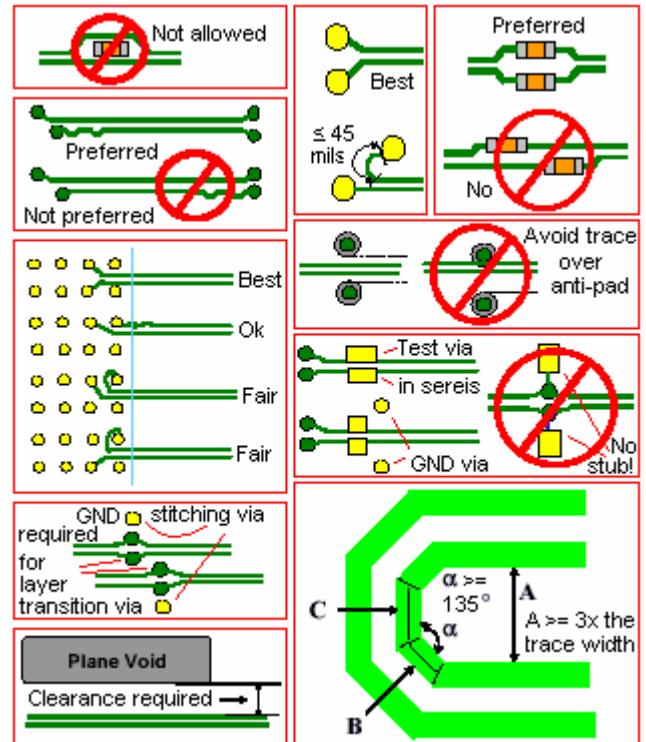


Figure 18: The layout guidance for the trace routings

4. The guidance for the layers under the edge fingers

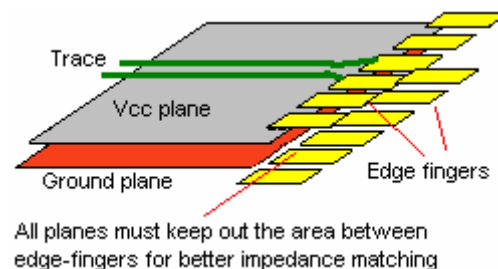


Figure 19: The layers under the edge fingers

For more detailed PCI Express PCB layout guidelines, refer to the PCI-SIG presentation of “PCI Express™ Technical Training Day PCI Express™ Technical Training Day”. Visit the web site www.pcisig.com, register, log-in, and click on http://www.pcisig.com/events/express_trainingday, then click on “PCI Express Technical Training Day presentation”.

The topology and layout guidance for the PI2EQX family

Figure 20 is the real layout of the 28” PI2EQX4402 demo board and is recommended for the layout using the PI2EQX family. All the green pairs are the inputs and all the red pairs are the outputs with 0.1uF AC coupling capacitors. All the pairs in U1 are the Tx pairs in the lanes 0, 1, 2 and 3 while all the pairs in the U5 are the Rx pairs also in the lanes 0, 1, 2 and 3. The reference clock pairs are not showing in this figure for clearer picture. The gerber and schematic files in PDF format are available up on request.

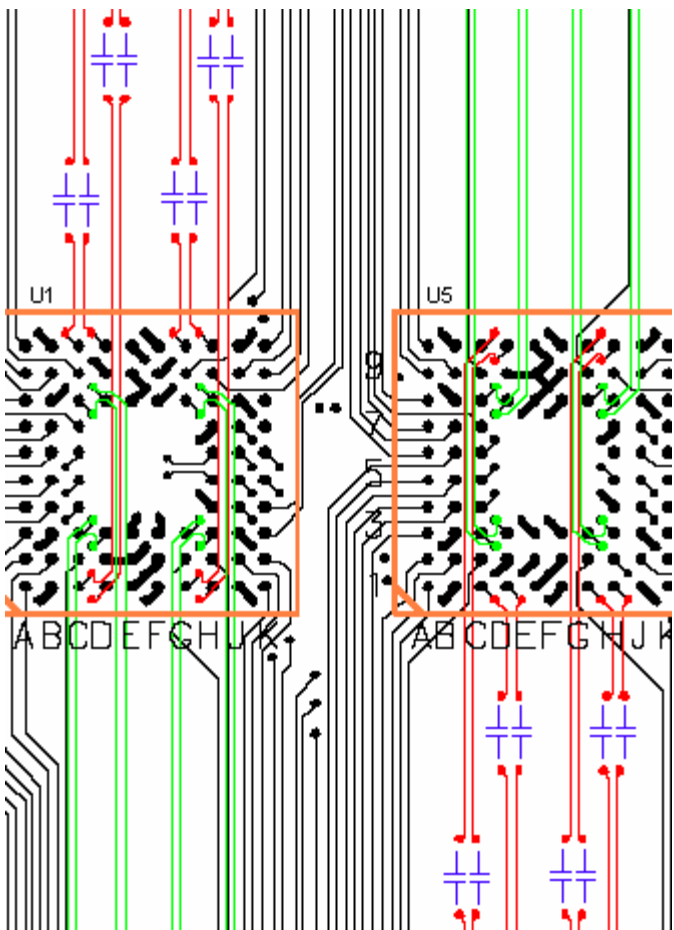


Figure 20: The real layout of the PI2EQX4402 28” demo board

The PCB layout recommended for the PI2EQX family:

- Use 0.22uF in size of 0402 for all the Vdd pins of the PI2EQX4402, as close to the Vdd pins as possible, within 2-3mm if feasible.
- Use dedicated Vdd and GND planes for to minimize the jitters coupled between channel trough power sources.
- To minimize the crosstalk, separate the Tx and Rx pairs by using different layers, if the PCB budget allows.
- It is recommended to use the whole chip of PI2EQX4402 for either Tx or Rx pairs, but not mix the Tx and Rx in the same chip for minimal crosstalk and interference.

The circuit of the PI2EQX family

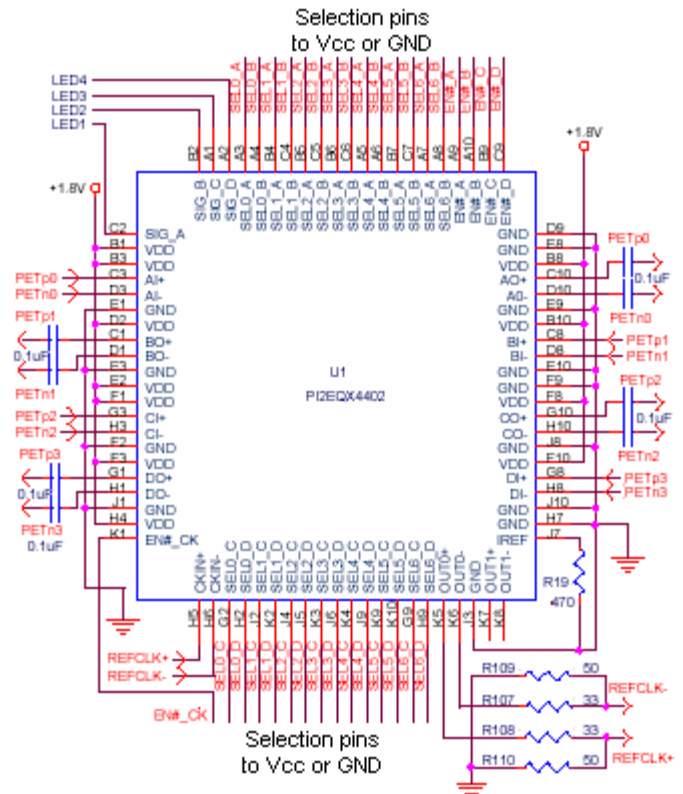


Figure 21: The circuit for the PI2EQX4402

Figure 21 is the circuit for the PI2EQX4402. Only one reference clock needs to be re-driven using one PI2EQX4402. If there is more than one PI2EQX4402 used for more lanes, short the input of the reference clock to ground and leave the output floating.

Please note that:

- The R107 (33-ohm), R108 (33-ohm), R109 (50-ohm) and R110 (50-ohm) are requested for the PI2EQX family as the clock output circuits.
- The 470-ohm R19 is requested for the PI2EQX family.
- The control pins can be directly connected to either Vcc or ground as high or low.
- The 0.1uf AC coupling capacitors are requested by the PCI Express spec.

The compliance test for the PI2EQX family

All the compliance test results in this application note were measured using the Agilent 54855A 6 GHz, 20 GSa/s differential scope, along with the “SigTest 2.0 Beta” compliance test software and the CLB (Compliance-test Load Board) test fixture, compliant to the compliance test requirement.

For the Tx and Rx eyes compliance test, it is recommended to use any of the scopes recommended on the PCI-SIG web site at:

http://www.pcisig.com/specifications/pciexpress/compliance/compliance_library/.

To download the free “SigTest 2.0 Beta” software, visit the web page www.pcisig.com, register and log-in, click on: http://www.pcisig.com/specifications/pciexpress/compliance/compliance_library/, then click on the “PCI Express electrical test software” in the middle of the page.

The CLB (Compliance-test Load Board) test fixture developed by Intel is available on the PCI-SIG web site at: http://www.pcisig.com/specifications/pciexpress/compliance/compliance_library/, click on [CLB and CBB ordering instructions](#) and then follow the purchasing procedure.

Refer to the detailed document on the PCI-SIG web site above on how to use a particular name-brand scope, capturing the waveform data, and save in “xxxx.csv” files. Then, run the “xxxx.csv” files in the “SigTest 2.0 Beta” compliance test software.

How to choose the template files in “SigTest 2.0 Beta” for compliance test

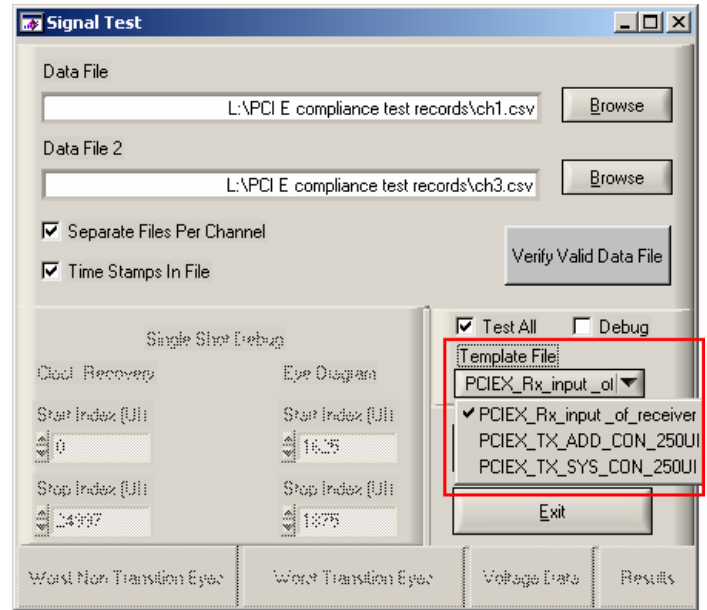


Figure 22: Pop-up window of “SigTest 2.0 Beta” for compliance test

The template file “PCIEX_TX_ADD_CON_250UI” in the red area in Figure 22 is for the add-in card transmitter test as in Figure 23, in which the signal on the edge-finger of the add-in card should be able to further drive the maximum 13” trace on the motherboard. Therefore, it uses the transmitter spec of 514mV/237ps for the transition bit with emphasis and uses the spec of 360mV/237ps for the non-transition bit with de-emphasis, as indicated in Tables 4-6 on page 44 of the “PCI Express card electromechanical specification revision 1.0a”.

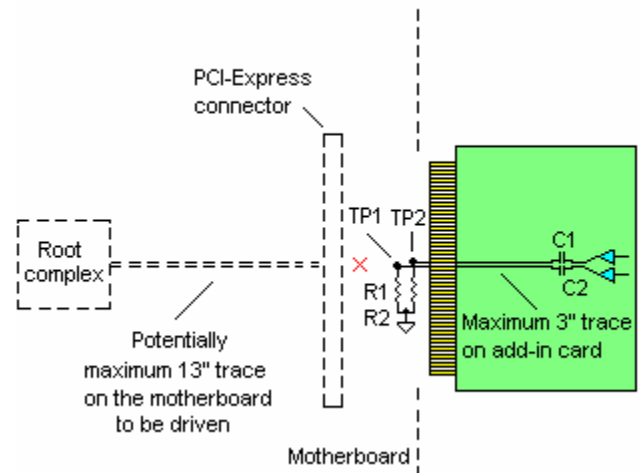


Figure 23: Add-in card transmitter test condition for the template file “PCIEX_TX_ADD_CON_250UI”

Therefore, it is recommended to use the template file "PCIEX_TX_ADD_CON_250UI" in the red area in Figure 22 for the PI2EQX's Tx eye compliance test, if the PI2EQX chip is deployed on the add-in card or on a board with maximum 3" trace between the PI2EQX chip and the edge-finger as in the Figure 23.

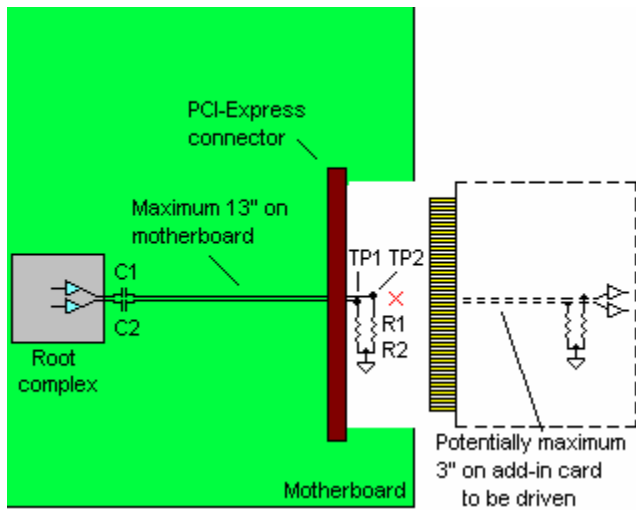


Figure 24: System test condition for the template file "PCIEX_TX_SYS_CON_250UI"

Likewise, the template file "PCIEX_TX_SYS_CON_250UI" is for the system board test as in Figure 24, using the spec in the Tables 4-8 on page 46 of the "PCI Express card electromechanical specification revision 1.0a". Since the signal at the motherboard connector (Figure 24) should be capable of further driving the maximum 3" trace on the add-in card, its specs of 274mV/183ps and 253mV/183ps are higher than the minimum 175mV/0.4UI Rx eye spec specified in the "PCI Express base specification revision 1.0a".

Therefore, it is recommended to use the template file "PCIEX_TX_SYS_CON_250UI" in the red area in Figure 22 for the PI2EQX re-driver test, if the PI2EQX chip is deployed on the motherboard as in the figure 23 with less than 13" trace and will further drive add-in card with a 3" trace as in the figure 24.

But this is not likely the case for the application using the PI2EQX for a long trace or cable.

The template file "PCIEX_Rx_input_of_receiver" in Figure 22 created for the Rx test of the PI2EQX family was not provided in the default template files in "SigTest 2.0 beta". The template file "PCIEX_Rx_input_of_receiver" complies with the minimum 175mV/0.4UI Rx eye spec specified in the Figures 4-26 on page 219 of the "PCI Express base specification revision 1.0a".

It is recommended to create a template file "PCIEX_Rx_input_of_receiver" as in Figure 22 for the PI2EQX Rx eye compliance test, for the eyes measured at the end of a trace longer than 13" or cable longer than 1 meter. Please refer to the section below for how to create the template file.

How to create the template files for the Rx compliance test in the "SigTest 2.0 Beta"

The procedure below shows how to create a template file to be used in the "SigTest 2.0 beta", as the template file "PCIEX_Rx_input_of_receiver" in Figure 22 for the Pericom Rx demo board or for any other tests.

1. Go to the directory where the SigTest 2.0 Beta is installed, it is normally in the C:\program files\ SigTest 2.0 Beta\templates. If it cannot be found in the C drive, try your other local drives to find where it was installed.
2. In the subdirectory C:\program files\ SigTest 2.0 Beta\templates, copy an existing template, e.g. the "PCIEX_TX_ADD_CON_250UI.dat", to a new template file, and rename it to "PCIEX_Rx_input_of_receiver.dat"
3. Open this new file in Microsoft Notepad or equivalent.
4. Towards the end of the file looking for the following statements:

```
; The eye template values
[template]
Upper=.600
Lower=-.600
Point1=".204 0"
Point2=".500 .180"
Point3=".796 0"
Point4=".500 -.180"

; The Transition eye template values
[TransitionTemplate]
Upper=.600
Lower=-.600
Point1=".204 0"
Point2=".500 .257"
Point3=".796 0"
Point4=".500 -.257"
MedianPeakJitterLimit=81.5E-12
```

The "Point1...Point4" above are the (x, y) co-ordinates that define the template (the red diamond in the compliance test result) of the "PCIEX_TX_ADD_CON_250UI". The ".180" and the "-.180" define the +/-360mV template for the non-

transition eye and the “.257” and the “-.257” define the +/- 514mV template for the transition eye, as indicated in the table 4-6 in page 44 of the “PCI Express card electromechanical specification revision 1.0a”.

5. In the following, modify the “Point1...Point4” complying the spec of 175mV/0.4UI, as the minimum receiver eye specified in the Figure 4-26 in page 219 of the "PCI Express base specification revision 1.0a", then save in the “PCIEX_Rx_input_of_receiver.dat” template file.

```
; The eye template values
[template]
Upper=.600
Lower=-.600
Point1=".300 0"
Point2=".500 .0875"
Point3=".700 0"
Point4=".500 -.0875"
```

```
; The Transition eye template values
[TransitionTemplate]
Upper=.600
Lower=-.600
Point1=".300 0"
Point2=".500 .0875"
Point3=".700 0"
Point4=".500 -.0875"
MedianPeakJitterLimit=108.5E-12
```

6. The next time when the “SigTest 2.0 Beta” is used, the new template “PCIEX_Rx_input_of_receiver” is available in the pop-up window as in the Figure 17, in addition to the “PCIEX_TX_ADD_CON_250UI” and the “PCIEX_TX_SYS_CON_250UI”, for the Pericom Rx demo board compliance test.

Conclusion

Pericom has a complete solution for the PCI Express application, including the PI2EQX Re-Driver family, the PI2PCIE PCI Express Signal Switch family and other PCI Express products that are shipping, sampling, or under development. Pericom is recognized in the industry as a technology leader in the high-speed differential switch market. Pericom is the first to develop the PCI Express PI2EQX Re-Driver family and the PI2PCIE Signal Switch family by using cutting edge design technology. The company has already achieved design wins for the PI2EQX and the PI2PCIE families at major global customers that are designing PCI Express systems.

References

1. PCI Express base specifications
2. The “PCI Express technical training” from PCI-SIG