PI3EQX7741ST/PI3EQX7742ST
SuperSpeed ReDriver in Source Application

Introduction

SuperSpeed USB (USB 3.0) delivering data rates up to 5Gbps which is ten times faster than Hi-Speed USB (USB 2.0) with optimized power efficiency. At these high transmission rates, signal integrity issues become increasingly restrictive on PCB trace and cable lengths, and on design implementation and features. Poor signal quality can significantly impact system performance and reliability.

Pericom's PI3EQX7741ST and PI3EQX7742ST are a low power, high performance 5.0Gbps signal ReDriver™ designed specifically for the USB 3.0 protocol. PI3EQX7741ST is a ReDriver support 1 port while PI3EQX7742 support 2 ports. Both parts provide programmable equalization, de-emphasis and the input threshold controls to optimize performance over a variety of physical mediums by reducing Inter-symbol interference (ISI). PI3EQX7741ST and PI3EQX7742 also have the automatic receiver detection and auto power down feature that selectively puts the device into a low power state on a channel by channel basis. Schematic and layout guidelines are provided in this application note.

- **SuperSpeed ReDriver in Source Application**
- **PI3EQX7741ST & PI3EQX772ST control pin setting**
- **SuperSpeed USB Layout Guideline**

SuperSpeed (USB 3.0) ReDriver in Source Application

PI3EQX7741ST is a dual channel (TX± and RX±), single lane USB3.0 ReDriver and PI3EQZX7741ST is a forth channel (2xTX± and 2xRX±). Both part can use in source application such as Notebooks, Desktops, Docking Station, Backplane and Cabling. Each channel offers selectable equalization setting to compensate the different input trace loss. The block diagrams below shows the application on notebook with docking w PI3EQX7741ST and motherboard with PI3EQX7742ST.

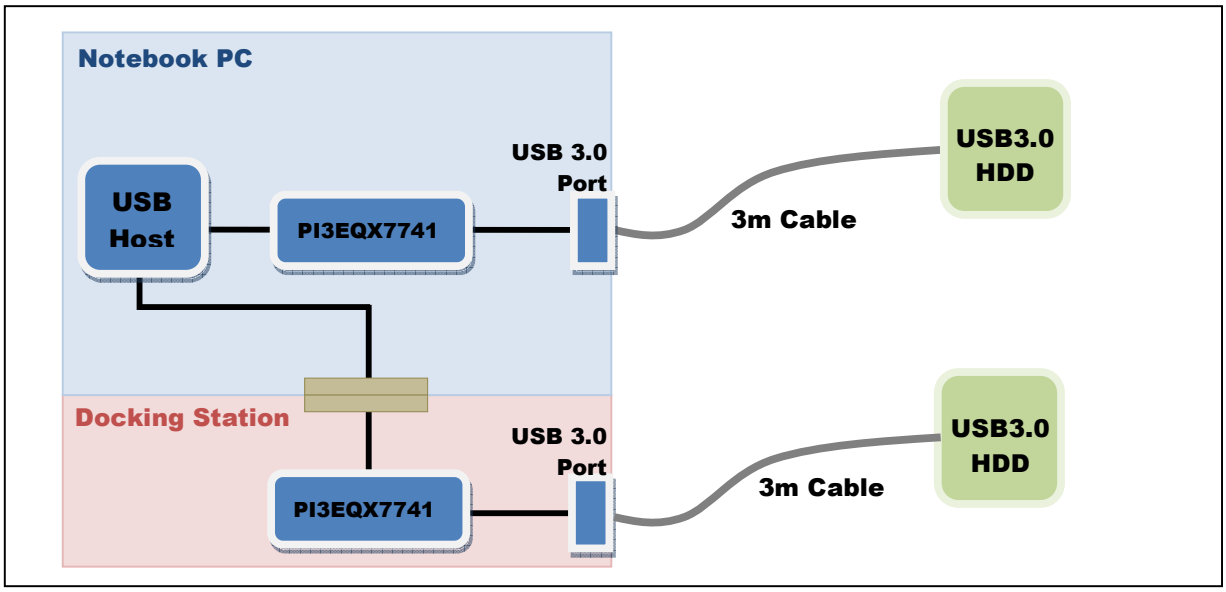


Figure 1: Block Diagram of PI3EQX7741ST on USB 3.0 Source Application

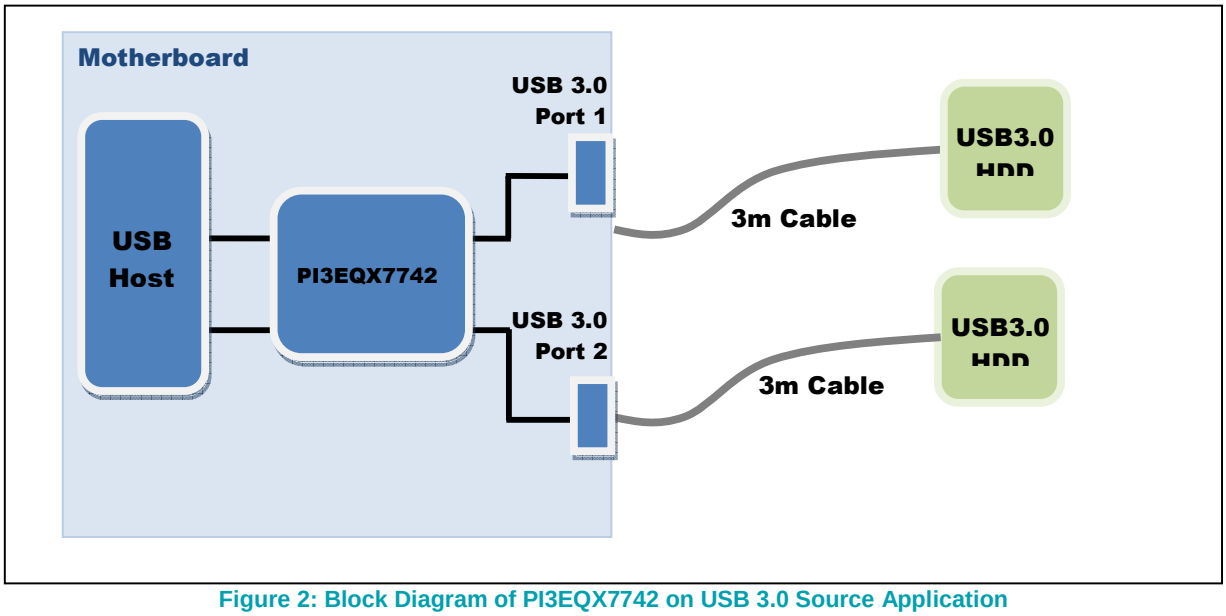
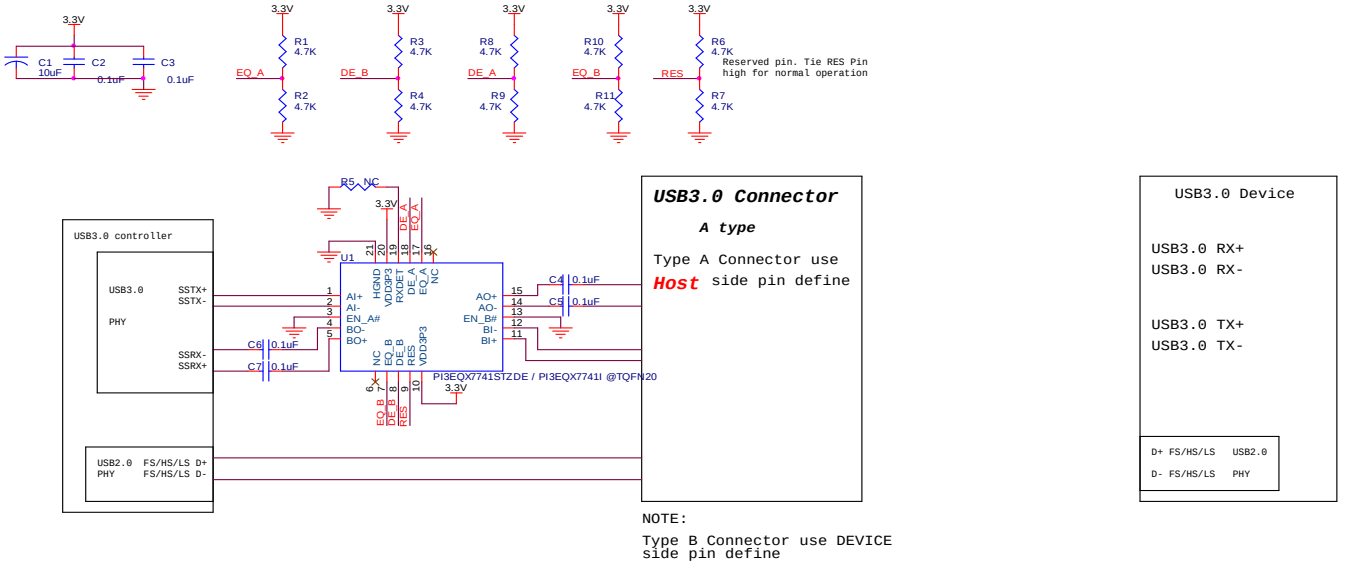


Figure 2: Block Diagram of PI3EQX7742 on USB 3.0 Source Application

Reference Design for Source Application

Below is a reference design of PI3EQX7741ST in source application.



NOTE:
After PCB layout, de-emphasis, and Equalizer should be fine tune

Output de-emphasis setting		
DE_A/B	De-emphasis	Description
0	0 dB	R3 & R8 NC, R4 & R9 on
open	-3.5 dB	R3 & R8 NC, R4 & R9 NC
1	-6 dB	R3 & R8 on, R4 & R9 NC

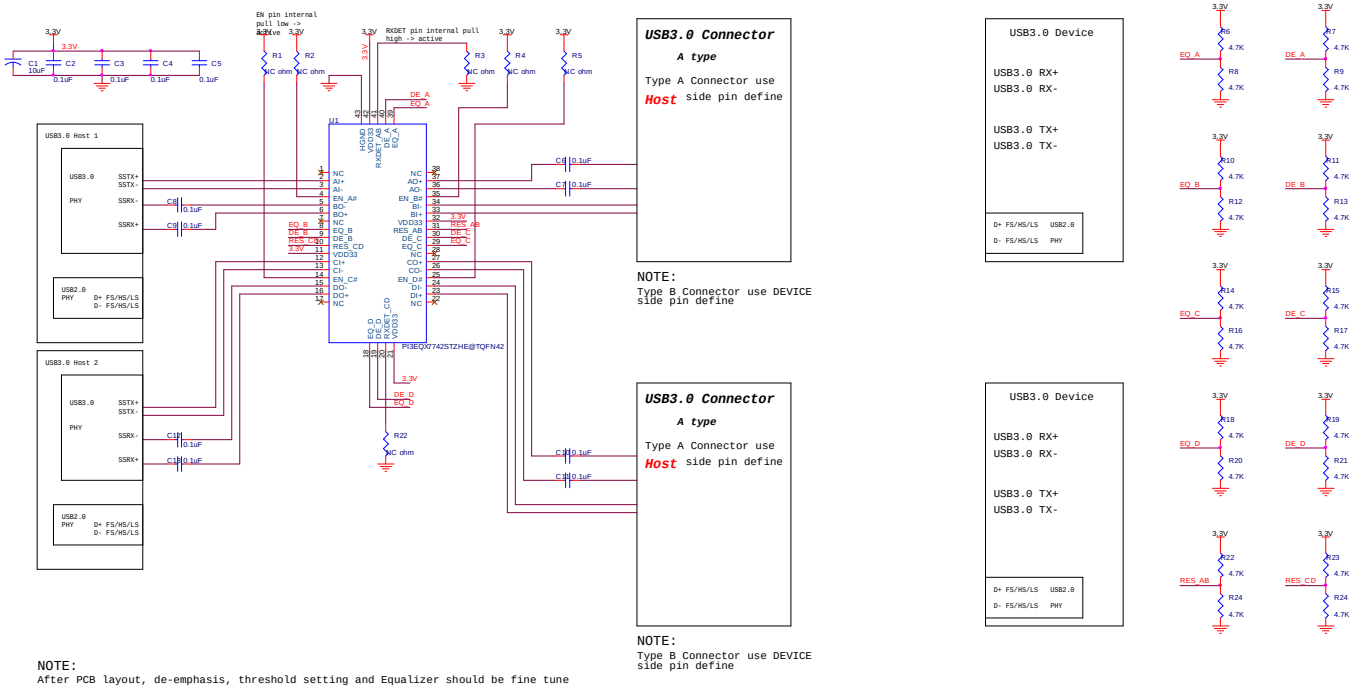
Equalizer setting		
EQ_A/B	@2.5GHz	Description
0	3 dB	R1 & R10 NC, R2 & R11 on
open	6 dB	R1 & R10 NC, R2 & R11 NC
1	9 dB	R1 & R10 on, R2 & R11 NC

EN_x#	RxDet	Input R	Output R
1	X	Hi-Z	Hi-Z
0	1	50 ohm / Hi-Z	50 ohm / Hi-Z
0	0	50 ohm	50 ohm

Figure 2: Reference Schematic of PI3EQX7701 USB3.0 Host Application

PI3EQX7741ST(I)_USB3_Typ App Schematic.pdf

Below is a reference design of PI3EQX7742ST in source application.



Output de- emphasis setting	
DE_A/B/C/D	De-emphasis
0	0 dB
open	-3.5 dB
1	-6 dB

Equalizer setting	
EQ_A/B/C/D	@2.5GHz
0	3 dB
open	6 dB
1	9 dB

EN_x#	RxDet	Input R	Output R
1	X	Hi-Z	Hi-Z
0	1	50 ohm / Hi-Z	50 ohm / Hi-Z
0	0	50 ohm	50 ohm

PI3EQX7742_USB3_TYP APP SCHEMATIC.pdf

According to Universal Serial Bus 3.0 Specification, all transmitters shall be AC coupled. The AC coupling capacitor value should be within 75nF and 200nF.

PI3EQX7741ST & PI3EQX7742ST control pin setting

A. RxDet / RxDet_XX and EN_X# setting

RxDet(1) pin and RxDet_XX(2) is used to enable the programmable receiver detect function. When RxDet/RxDet_XX pin is set to high, the automatic receiver detection will be active and the device will move to power down mode due to inactivity.

EN_X# pins are used to enable the channels of PI3EQX7741ST and PI3EQX7742ST. When EN_X# is set to low, channel X is in normal operation.

EN_X#	RxDet(1)/ RxDet_XX(2)	Function	Input R	Output R
1	X	Channel Disable if both EN_X# are high, Chip Power Down	Hi-Z	Hi-Z
0	0	Chip and channel X enabled, receiver detect is not active	50Ω	50Ω
0	1	Chip and channel X enabled, receiver detect is active	50Ω / Hi-Z	50Ω / Hi-Z

Table 1: EN_A/B and RxDet truth table of PI3EQX7741ST / PI3EQX7742ST

Remark:
(1) RxDet is only offered on PI3EQX7741ST
(2) RxDet_XX is only offered on PI3EQX7742ST

As 200kΩ internal pull-down resistors are implemented in EN_X pins of PI3EQX7741ST and PI3EQX7742ST, leave the pins floating to enable the channel. The RxDet / RxDet_X pin with 200kΩ internal pull up resistor, only external pull-down resistor is required to adjust the receiver detection setting.

B. EQ Settings

Equalization feature offers compensation of deterministic jitter introduced by impedance mismatch. PI3EQX7741ST and PI3EQX7742ST offers 3 equalization levels on all channels for different input trace lengths which can be selected by EQ_X pins.

Input PCB Trace Length	Recommended EQ	EQ_A/EQ_B
2 - 18 inch FR4 (9-mil trace)	3dB	0
15 – 34 inch FR4 (9-mil trace)	6dB	Open
32 – 50 inch FR4 (9-mil trace)	9dB	1

Table 3: EQ setting of channel A and B

External pull-down / pull up resistors or floating on EQ_X pins are required to adjust the equalization setting.

Remark: It's suggested to disable the de-emphasis function at the USB3.0 host output if ReDriver is used. De-emphasis setting will decrease the swing level which may introduce the jitter and noise to the ReDriver input.

C. DE_x Settings

Selectable de-emphasis is provided to compensate the distortion on USB3.0 signal at differential outputs. The de-emphasis level will depend on the cable length and can be selected by DE_X pins.

Output USB3.0 cable length (30AWG)	Recommended DE	DE_A/DE_B
0 – 1m	0dB	0
1 – 3m	-3.5dB	Open
3 – 4m	-6dB	1

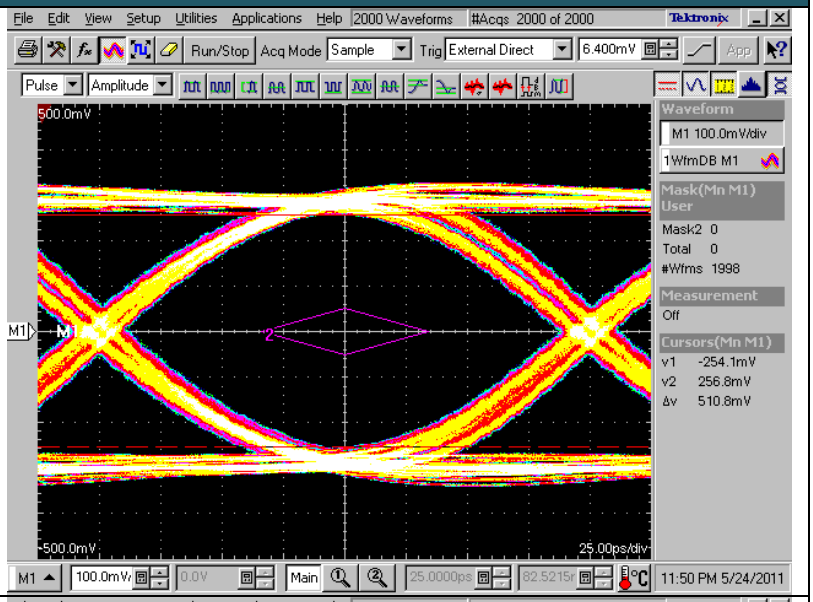
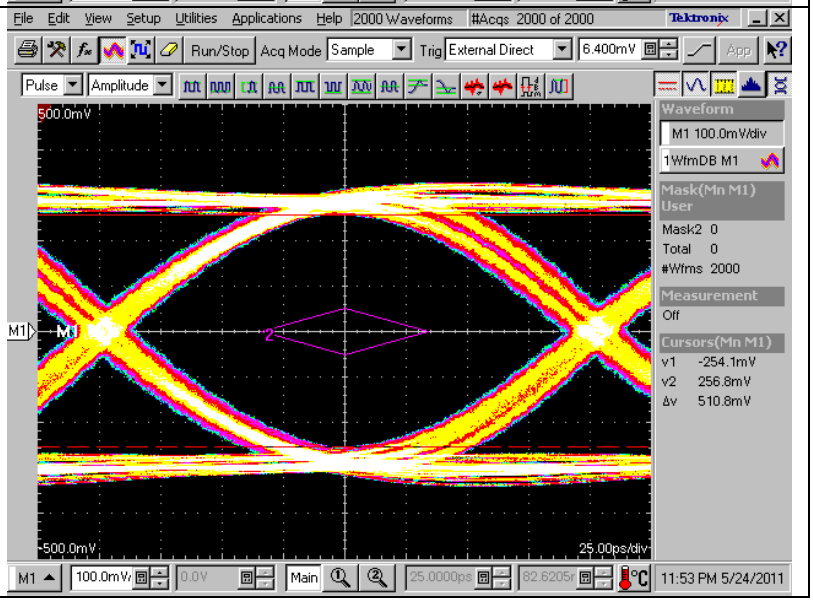
Table 4: DE setting of channel A and B

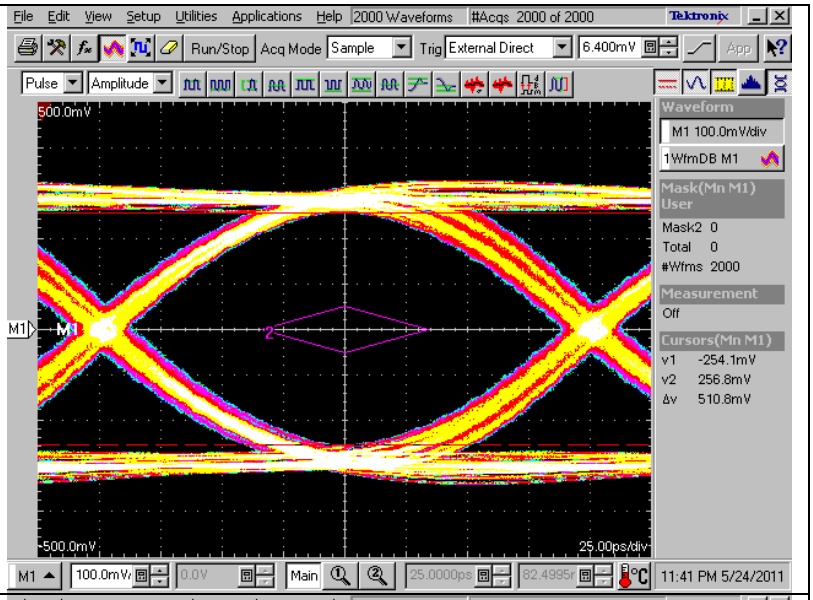
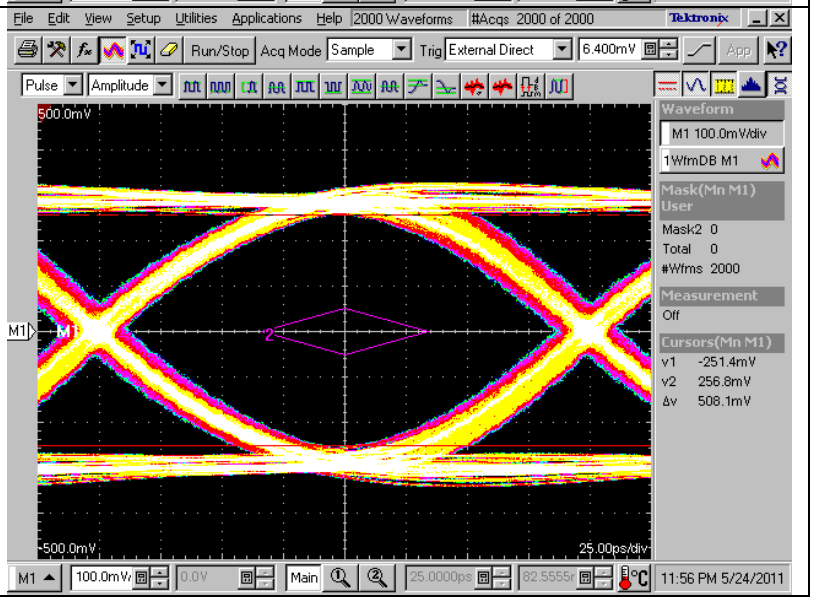
External pull-down / pull up resistors or floating on all DE_X pins are required to adjust the de-emphasis level setting.

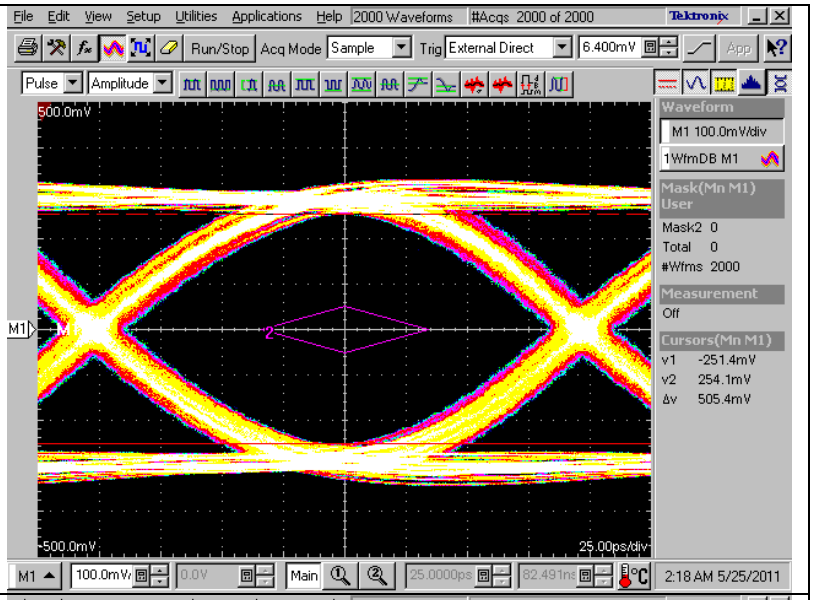
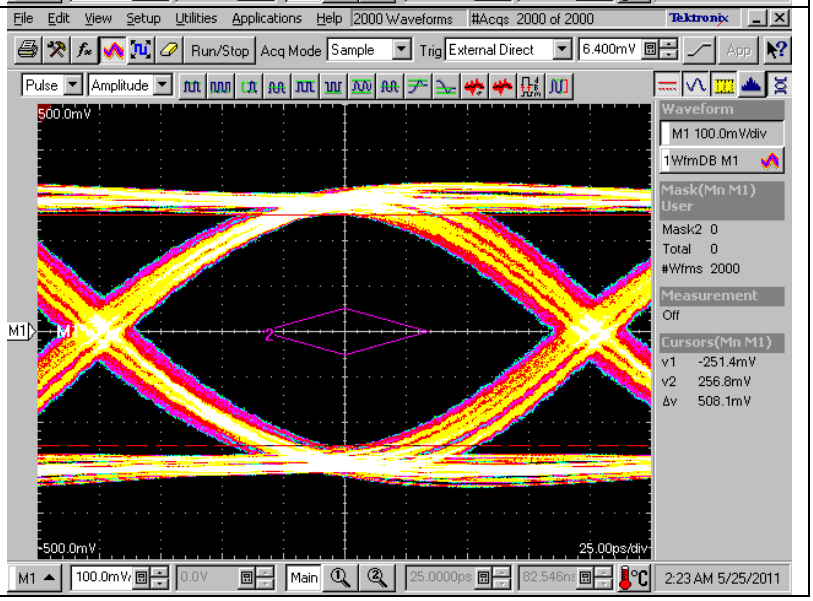
Typical Eye Diagram

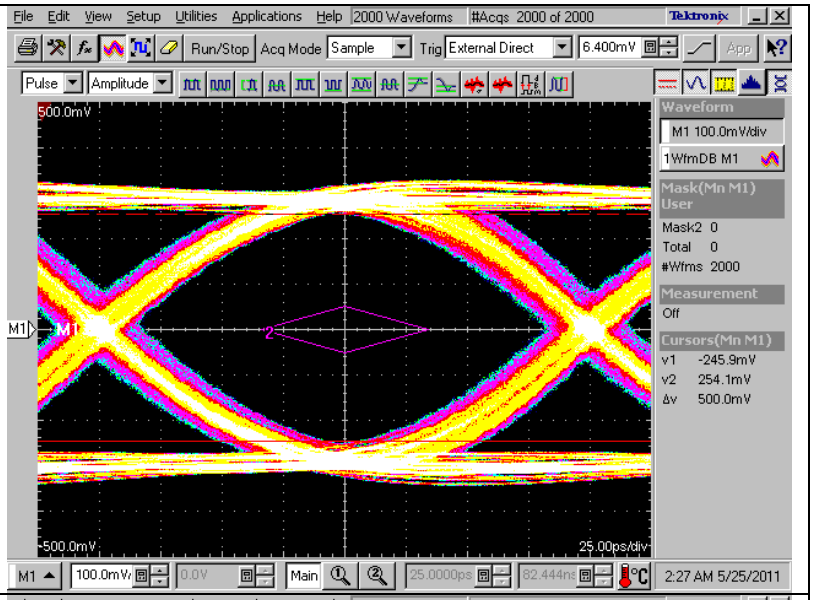
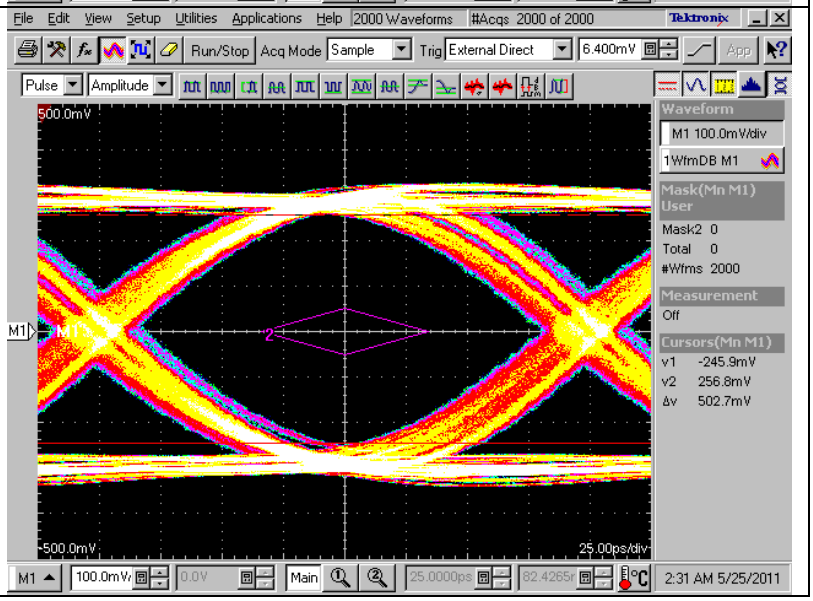
A. EQ Setting vs. Input Trace Length

Input Signal Characteristics:
Data Rate: 5Gbps
Pattern: PRBS7
PCB differential trace: 9/11/9 mil
Differential trace Impedance: 100Ω
Output PCB trace length = 12" (insertion loss ~ 3.6dB -> ~ 1m 30AWG SDP pairs)

PCB Input trace length	De-emphasis and EQ Setting of PI3EQX7741/ PI3EQX7742	
3.9"	De-emphasis setting:- 3.5dB EQ setting: 3dB	
6.0"	De-emphasis setting:- 3.5dB EQ setting: 3dB	

12”	De-emphasis setting:- 3.5dB EQ setting: 3dB	
18”	De-emphasis setting:- 3.5dB EQ setting: 3dB	

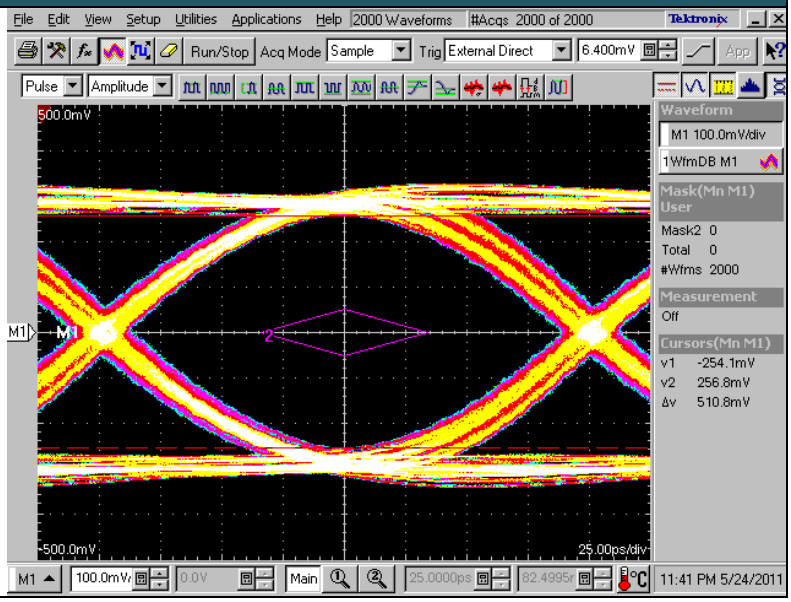
24”	De-emphasis setting:- 3.5dB EQ setting: 3dB	
30”	De-emphasis setting:- 3.5dB EQ setting: 6dB	

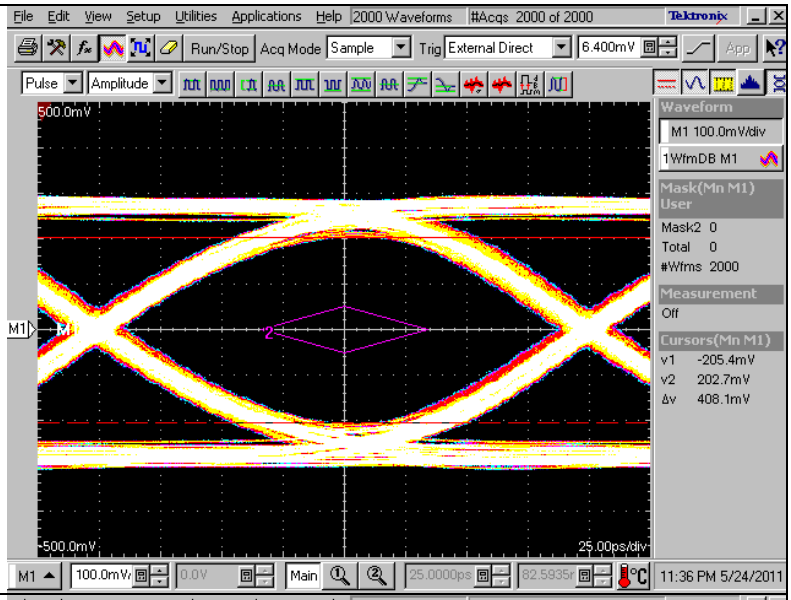
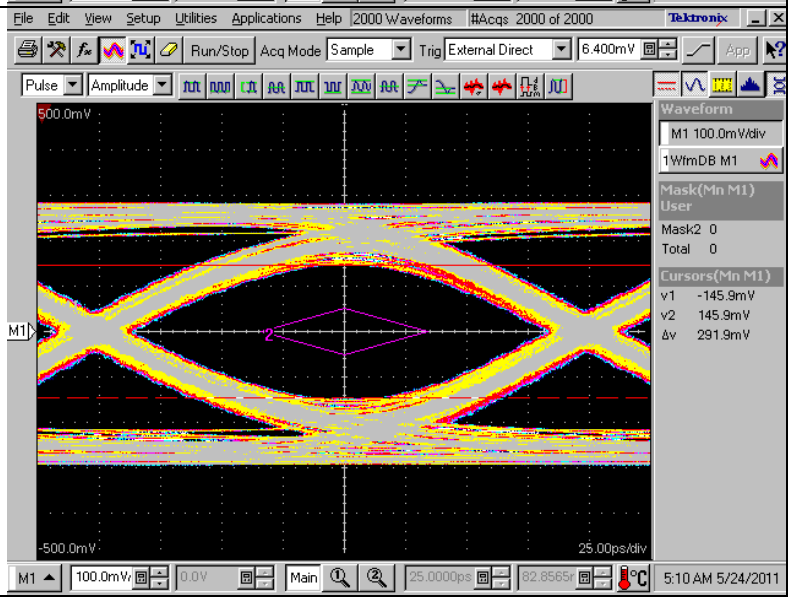
36”	De-emphasis setting:- 3.5dB EQ setting: 6dB	
42’	De-emphasis setting:- 3.5dB EQ setting: 9dB	

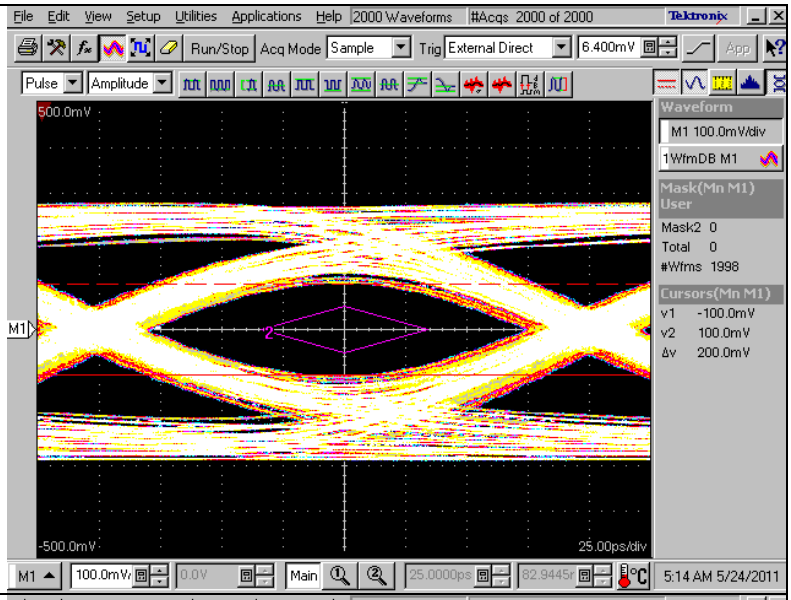
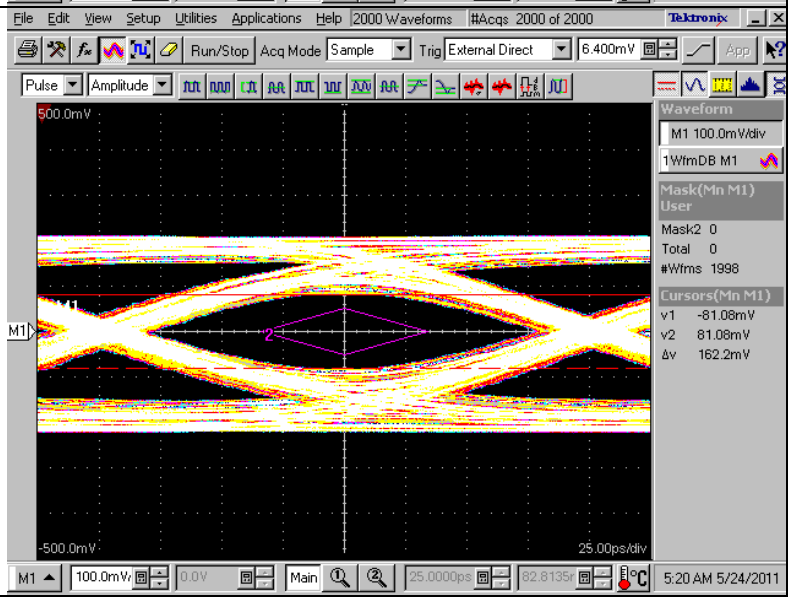
B. DE Setting vs. Output Trace Length

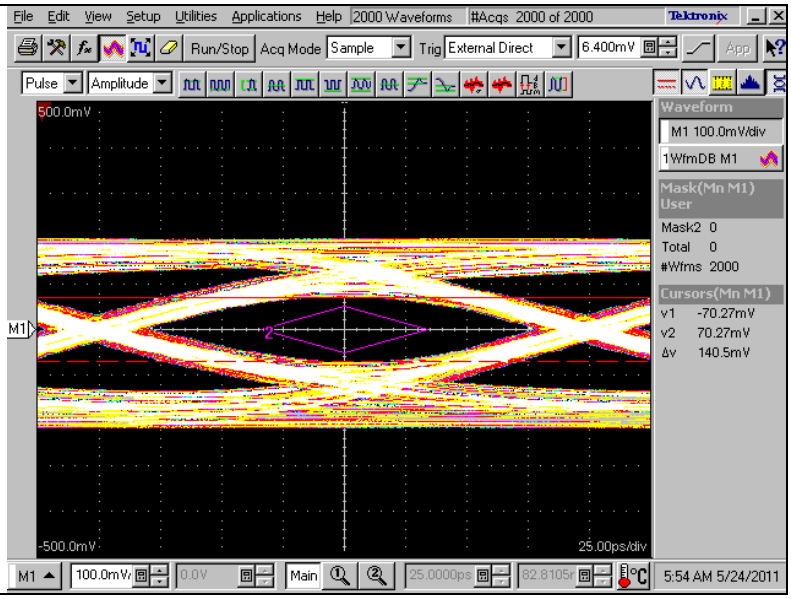
Input Signal Characteristics:
Data Rate: 5Gbps
Pattern: PRBS7
Input PCB trace length = 12” (insertion loss ~ 3.6dB)

PCB Trace length	PCB insertion Loss	Relative USB3.0 cable length (30AWG)	Recommended DE setting
12”	-3.6dB	1.2m	-3.5dB
18”	-5.4dB	1.8m	
24”	-7.5dB	2.5m	
30”	-9.3dB	3.1m	
36”	-11dB	3.6m	-6dB
42”	-12dB	4.0m	

PCB Output trace length	De-emphasis and EQ Setting of PI3EQX7741/ PI3EQX7742	Output Eye Diagram
12”	De-emphasis setting:-3.5dB EQ setting: 3dB	

18”	De-emphasis setting:-3.5dB EQ setting: 3dB	
24”	De-emphasis setting:-3.5dB EQ setting: 3dB	

30”	De-emphasis setting:-3.5dB EQ setting: 3dB	
36”	De-emphasis setting:-6dB EQ setting: 3dB	

42”	De-emphasis setting:-6dB # EQ setting: 6dB	

Remark:
In order to pass the eye diagram test, EQ need to change to 6dB for output 42” PCB trace

Compliance test Result Summary:

1. Link Test: Pass
2. Physical Test:
   a. LFPS test: Pass
   b. TX test: Pass
   c. RX test: Pass
3. CV Chapter 9 test Pass
4. xHCI test Pass

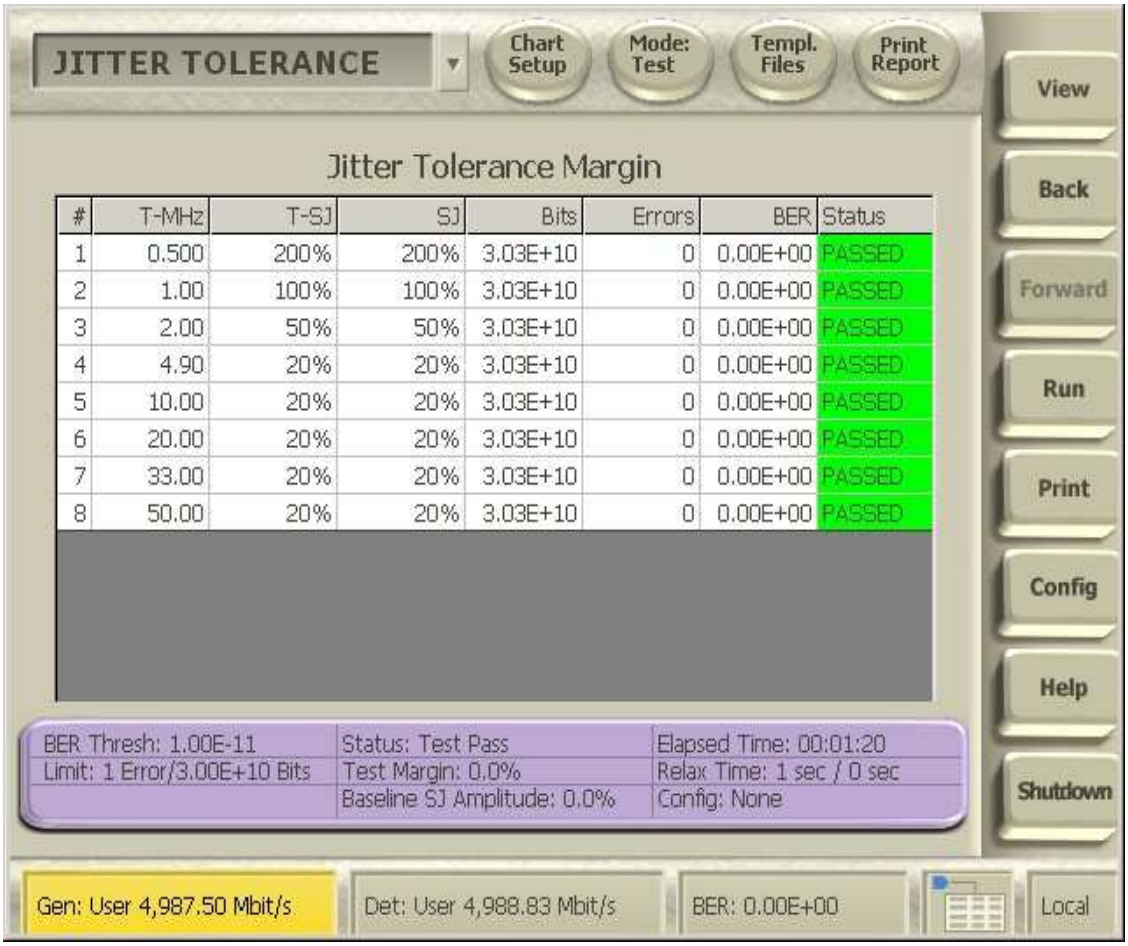
1. Link Test

Test item	Pass / Fail
TD.7.01 Link Bring-up Test	Pass
TD.7.02 Link Commands Framings Robustness Test	Pass
TD.7.03 Link Commands CRC-5 Robustness Test	Pass
TD.7.04 Invalid Link Commands Test	Pass
TD.7.05 Header Packet Framing Robustness Test	Pass
TD.7.06 Data Payload Packet Framing Robustness Test	Pass
TD.7.07 RX Header Packet Retransmission Test	Pass
TD.7.08 TX Header Packet Retransmission Test	Pass
TD.7.09 PENDING_HP_TIMER Deadline Test	Pass
TD.7.10 CREDIT_HP_TIMER Deadline Test	Pass
TD.7.11 PENDING_HP_TIMER Timeout Test	Pass
TD.7.12 CREDIT_HP_TIMER Timeout Test	Pass
TD.7.13 Wrong Header Sequence Test	Pass
TD.7.14 Wrong LGOOD_N Sequence Test	Pass
TD.7.15 Wrong LCRD_X Sequence Test	Pass
TD.7.17 tPortConfiguration Time Timeout Test	Pass
TD.7.18 Low Power initiation for U1 test	Pass
TD.7.19 Low Power initiation for U2 test	Pass
TD.7.20 PM_LC_TIMER Deadline Test	Pass
TD.7.21 PM_LC_TIMER Timeout Test	Pass
TD.7.26 Transition to U0 from Recovery Test	Pass

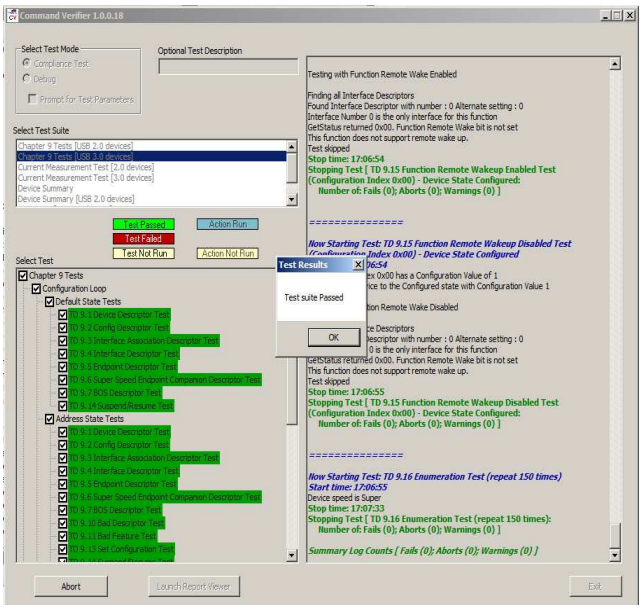
2. Physical Test

LFPS test			
Test	**Measurement**	**Current Value**	**Pass / Fail**
1.1	Polling.LFPS Minimum Burst Width	999 ns	Pass
1.1	Polling.LFPS Mean Burst Width	1.002 µs	Pass
1.1	Polling.LFPS Maximum Burst Width	1.003 µs	Pass
1.1	Polling.LFPS Minimum Burst Repeat Time	9.99 µs	Pass
1.1	Polling.LFPS Mean Burst Repeat Time	10.00 µs	Pass
1.1	Polling.LFPS Maximum Burst Repeat Time	10.02 µs	Pass
1.1	LFPS Period	32 ns	Pass
1.1	LFPS Rise Time	642 ps	Pass
1.1	LFPS Fall Time	642 ps	Pass
1.1	LFPS Duty Cycle	49.4 %	Pass
1.1	LFPS Differential Voltage Peak Peak	928 mV	Pass
1.1	LFPS AC Common Mode Voltage Peak Peak	30.558 mV	Pass
TX Test			
Test	**Measurement**	**Current Value**	**Pass / Fail**
1.3.1	Tj CP1	19.65 ps	Pass
1.3.1	Rj (rms) CP1	1.127 ps	Pass
1.3.2	Phase Jitter Slew Rate Max	2.233 ms/s	Pass
1.3.2	Phase Jitter Slew Rate Min	-2.978 ms/s	Pass
1.3.3	Tj CP1 SigTest	18.36 ps	Pass
1.3.3	Rj (rms) CP1 SigTest	1.145 ps	Pass
1.3.1	Tj CP0	56.20 ps	Pass
1.3.1	Rj (rms) CP0	1.115 ps	Pass
1.3.1	Dj CP0	40.75 ps	Pass
1.3.4	Eye Diagram Mask Hits	0 hits	Pass
1.3.4	Eye Height	223 mV	Pass
1.3.3	Tj CP0 SigTest	60.91 ps	Pass
1.3.3	Rj (rms) CP0 SigTest	1.145 ps	Pass
1.3.3	Dj DD CP0 SigTest	44.81 ps	Pass
1.3.5	Non Trans Violations SigTest	0 hits	Pass
1.3.5	Trans Violations SigTest	0 hits	Pass

RX: Jitter Tolerance Test



3. CV Chapter 9 Test



Test item	Pass / Fail
TD 9.1 Device Descriptor Test	Pass
TD 9.2 Config Descriptor Test	Pass
TD 9.3 Interface Association Descriptor Test	Pass
TD 9.4 Interface Descriptor Test	Pass
TD 9.5 Endpoint Descriptor Test	Pass
TD 9.6 Super Speed Endpoint Companion Descriptor Test	Pass
TD 9.7 BOS Descriptor Test	Pass
TD 9.9 Halt Endpoint Test	Pass
TD 9.10 Bad Descriptor Test	Pass
TD 9.11 Bad Feature Test	Pass
TD 9.14 Suspend/Resume Test	Pass
TD 9.15 Function Remote Wakeup Enabled Test	Pass
TD 9.15 Function Remote Wakeup Disabled Test	Pass
TD 9.22 Set Feature Test	Pass
TD 9.20 LTM Test	Pass
TD 9.19 Time Control Transfer Test	Pass
TD 9.16 Enumeration Test	Pass
TD 9.23 Reset Device Test	Pass

4. xHCI Test

Test item	Pass / Fail
TD1.01 PCI Configuration Register Test	Pass
TD1.02 Capability Register Test	Pass
TD1.03 Register Default Value Test	Pass
TD1.04 Command and Status Registers Test	Pass
TD1.05 Extended Capabilities Registers Test	Pass
TD3.01SuperSpeed Device Attach and Detach Test	Pass
TD3.02USB 2.0 Device Attach and Detach Test	Pass
TD3.03Port Power Test	Pass
TD3.05USB 2.0 Port Disable Test	Pass
TD3.08USB 2.0 Port Suspend and Resume Test	Pass
TD3.03Port Power Test	Pass
TD3.04SuperSpeed Port Disable Test	Pass
TD3.06SuperSpeed Port Warm Reset Test	Pass
TD3.07SuperSpeed Port Suspend and Resume Test	Pass
TD3.10USB 2.0 Port Remote Wakeup Test	Pass

SuperSpeed USB Layout Guideline

A. Decoupling capacitor of VDD

It is recommended to put 0.1uF decoupling capacitor at each VDD pin of Pericom IC. Below is a layout reference of decoupling capacitor placement on a PI3EQX7741ST demo board. Two decoupling capacitors circled in pink below are located next to the four VDD pins (pins 10 and 20) of PI3EQX7741ST.

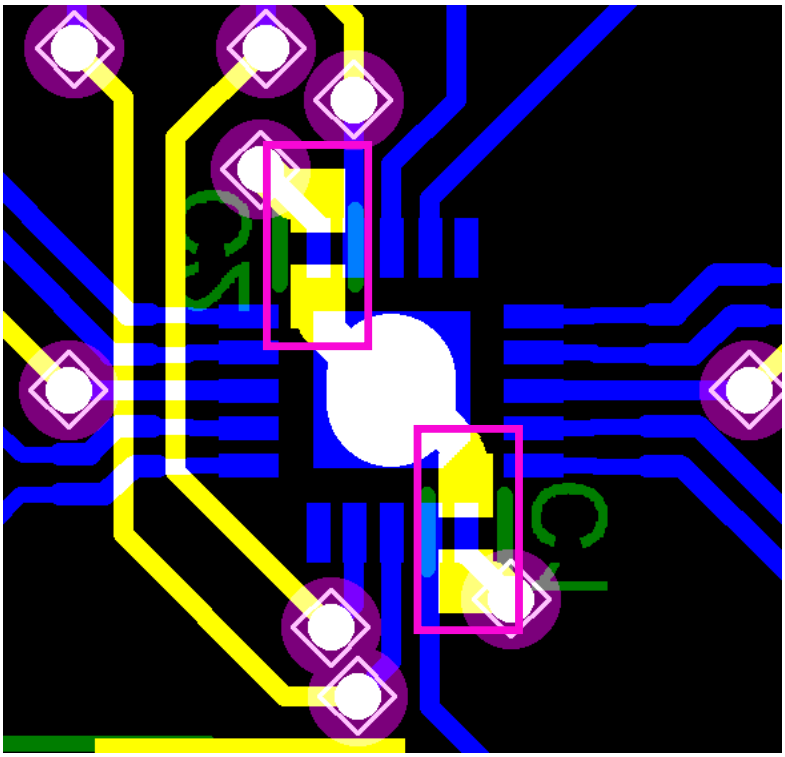


Figure 3: Decoupling Capacitor Placement on PI3EQX7741ST

B. PCB layers

It is recommended to use at least four layers PCB for SuperSpeed USB design. Every data signal trace should be routed entirely over the ground plane on an adjacent layer.

Recommendation on 4-layer PCB setting:

Layer	Setting 1	Setting 2
Top	Data signal, Clock	Power, Control Signal
2nd	GND	Power, GND
3rd	Power, GND	GND
Bottom	Power, Control signal	Data signal, Clock

C. Routing around the USB connector

On the host design, USB receptacle connector is used on the PCB. For the Vbus trace, it's suggested to insert a ferrite bead. For the shielding of USB connector (shielding of USB cables), AC isolation to the ground (such as proper value of inductor, instead of connecting the cable shield directly to the PCB ground plane).

For the SuperSpeed signal trace, the impedance should be maintained. Avoiding any stubs and removing any routing that cause signal discontinuity and severe EMC noise issue. Also, do not put any metal between all SuperSpeed signal pair pins on every layer when using receptacles with pins stabbing the PCB.

Crosstalk between the signal trace

There are 3 pairs of signal (SSTX± /SSRX±/ D±) for USB3.0 and these signal pairs will cause three typical type near-end crosstalk:

i. SSTX± to D± in RX mode
ii. SSTX± to SSRX±
iii. D± to SSRX± in TX mode

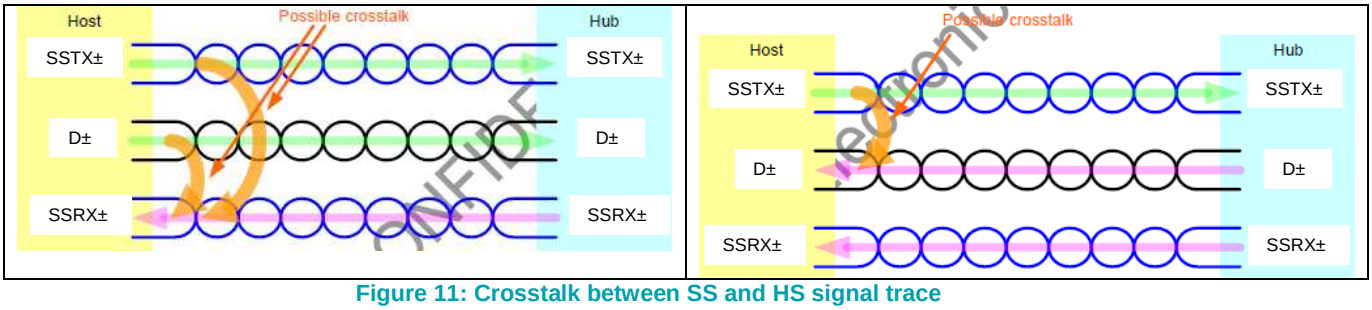
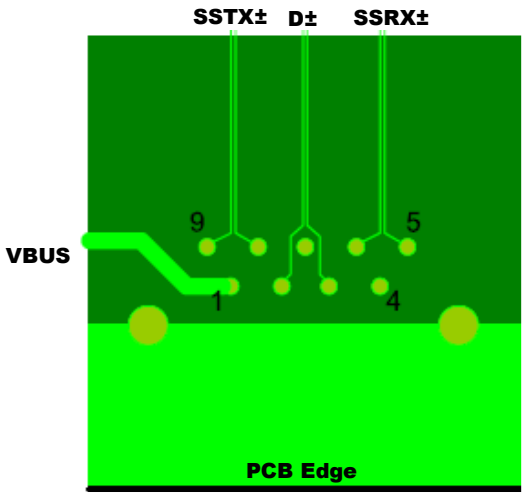


Figure 11: Crosstalk between SS and HS signal trace

In order to minimize the crosstalk issue, the routing of the signal trace between SSTX±/ SSRX± and D± pairs should not be closed to each other.

For Standard-A receptacles:

Example 1:



Example 2:

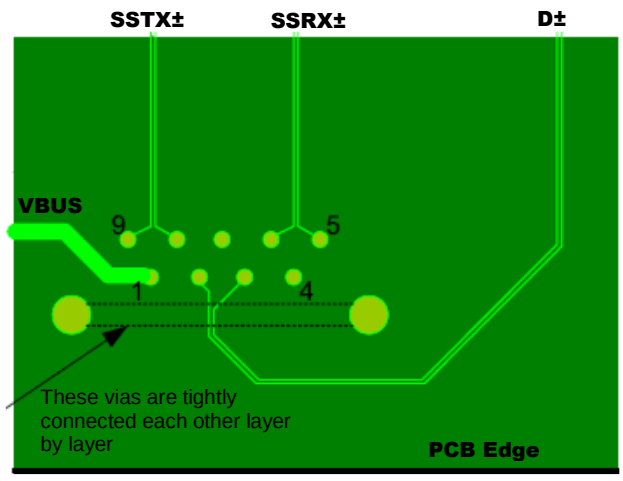
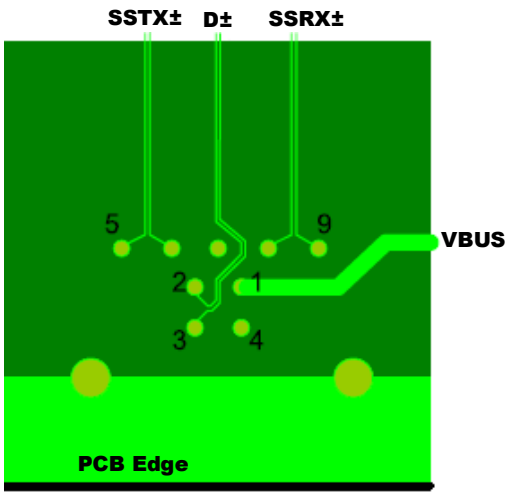


Figure 12: Example of routing on Standard-A receptacle connector

For Standard-B receptacles:

Example 1:



Example 2:

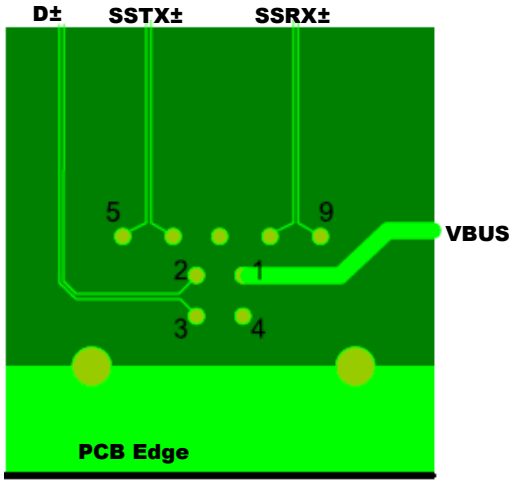


Figure 13: Example of routing on Standard-B receptacle connector

For Standard-A double-stack receptacles:

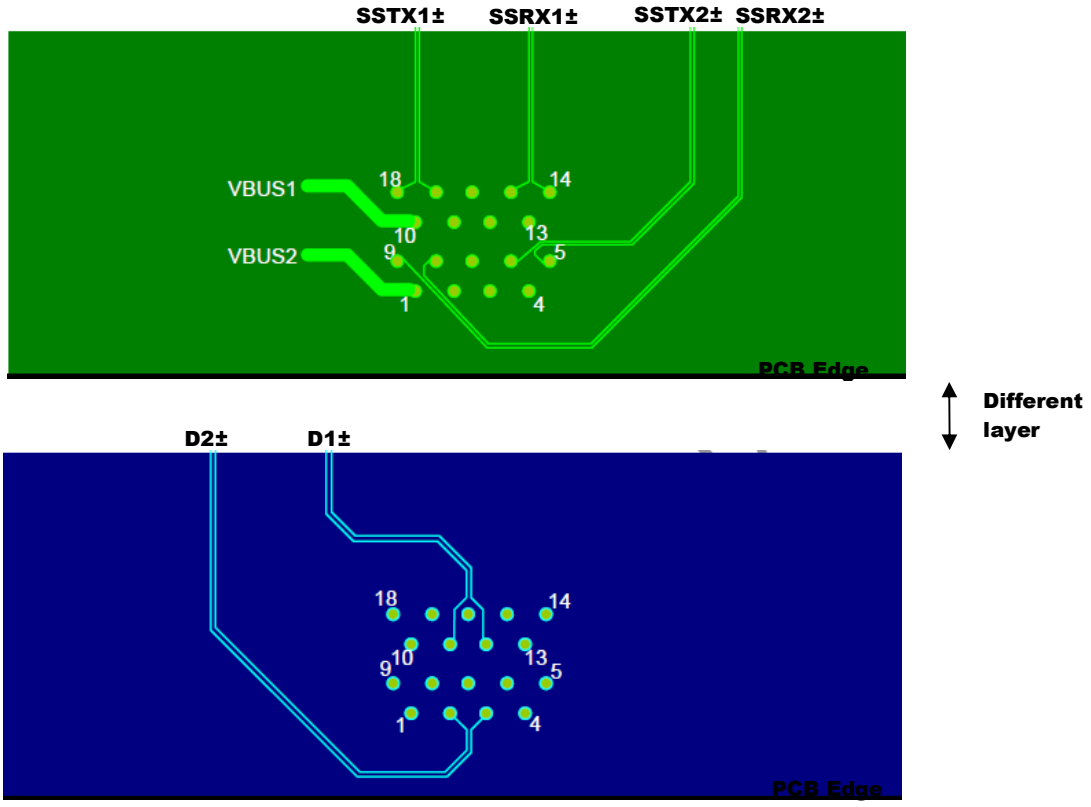


Figure 14: Example of routing on Standard-A double-stack connector

SuperSpeed signal trace impedance

The layout around USB3.0 receptacle connector is routed as one or more large metal planes in specific layer (such as GND layer). In order to maintain the differential impedance of any SuperSpeed signal trace, make sure there is no metal between pins for any differential pair.

For Standard-A receptacles:

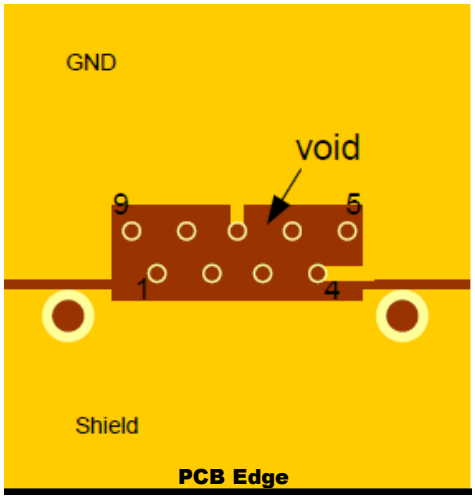
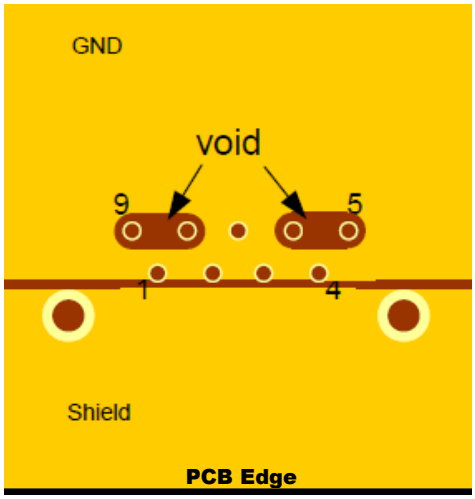
Example 1: Void at whole area around pins	Example 2: Void around SuperSpeed related pins
	

Figure 15: Example of the ground routing at GND layer with Standard-A receptacle connector

For Standard-B receptacles:

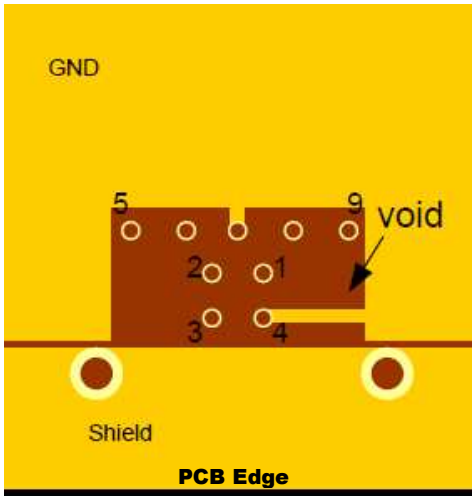
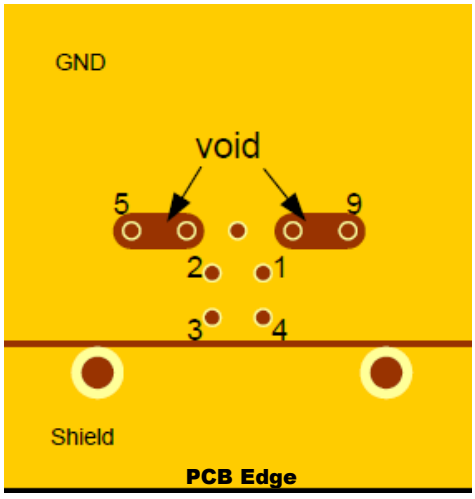
Example 1: Void at whole area around pins	Example 2: Void around SuperSpeed related pins
	

Figure 16: Example of the ground routing at GND layer with Standard-B receptacle connector

Stub on SuperSpeed trace

The pin on USB3.0 receptacle connector becomes an open stub if the SS signal trace pair is designed on the top layer which will cause the signal discontinuity issue.

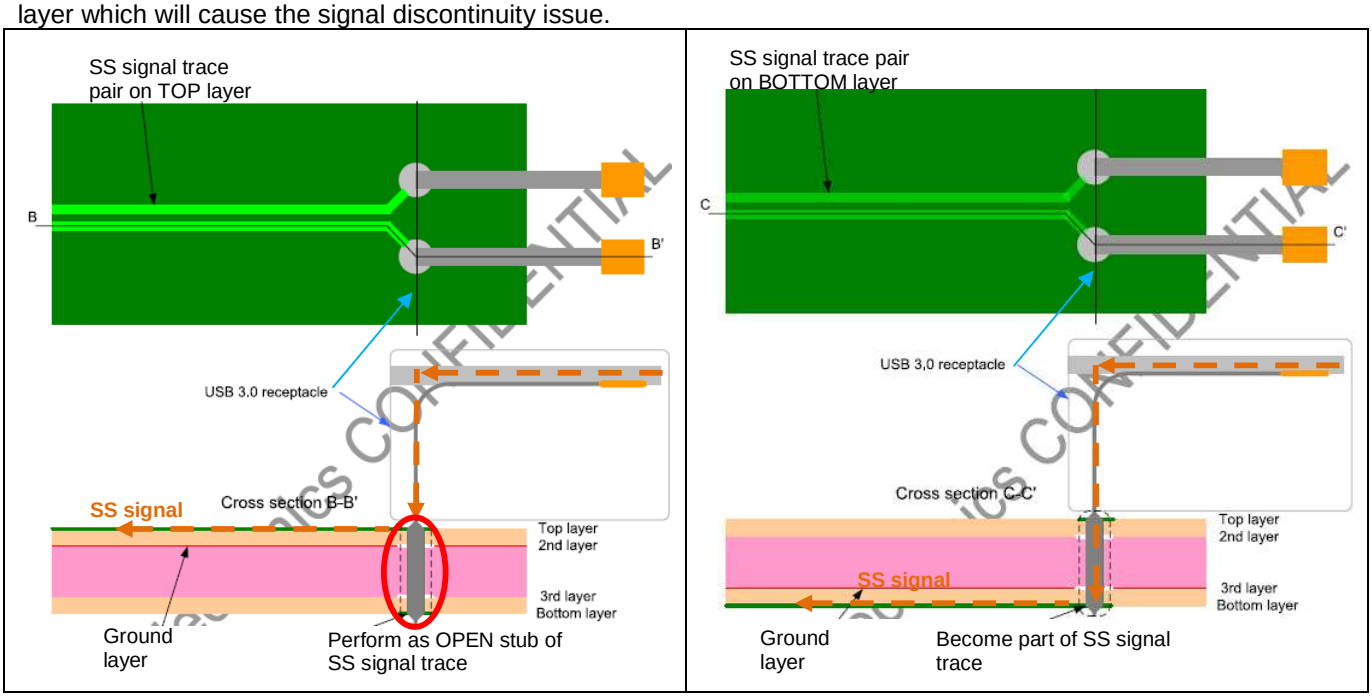


Figure 17: Example of the SS signal trace routing with receptacle connector

D. Routing around the USB Controller

Because high speed signal is sensitive to power signal, the routing on power and ground design of USB controller need to be carefully done. Same as section (A), the decoupling cap is needed for each power pin and it should be placed as close as the power pad of USB controller. As USB controller contains both analog and digital section, analog power and digital power is required. In order to avoid the interference from the digital signal, which causes the malfunction on the analog circuit, the routing between analog power and digital signal trace should be placed as far as possible (including the signal trace). For the same voltage level's analog power and digital power, a ferrite bead should be added in between for noise filtering.

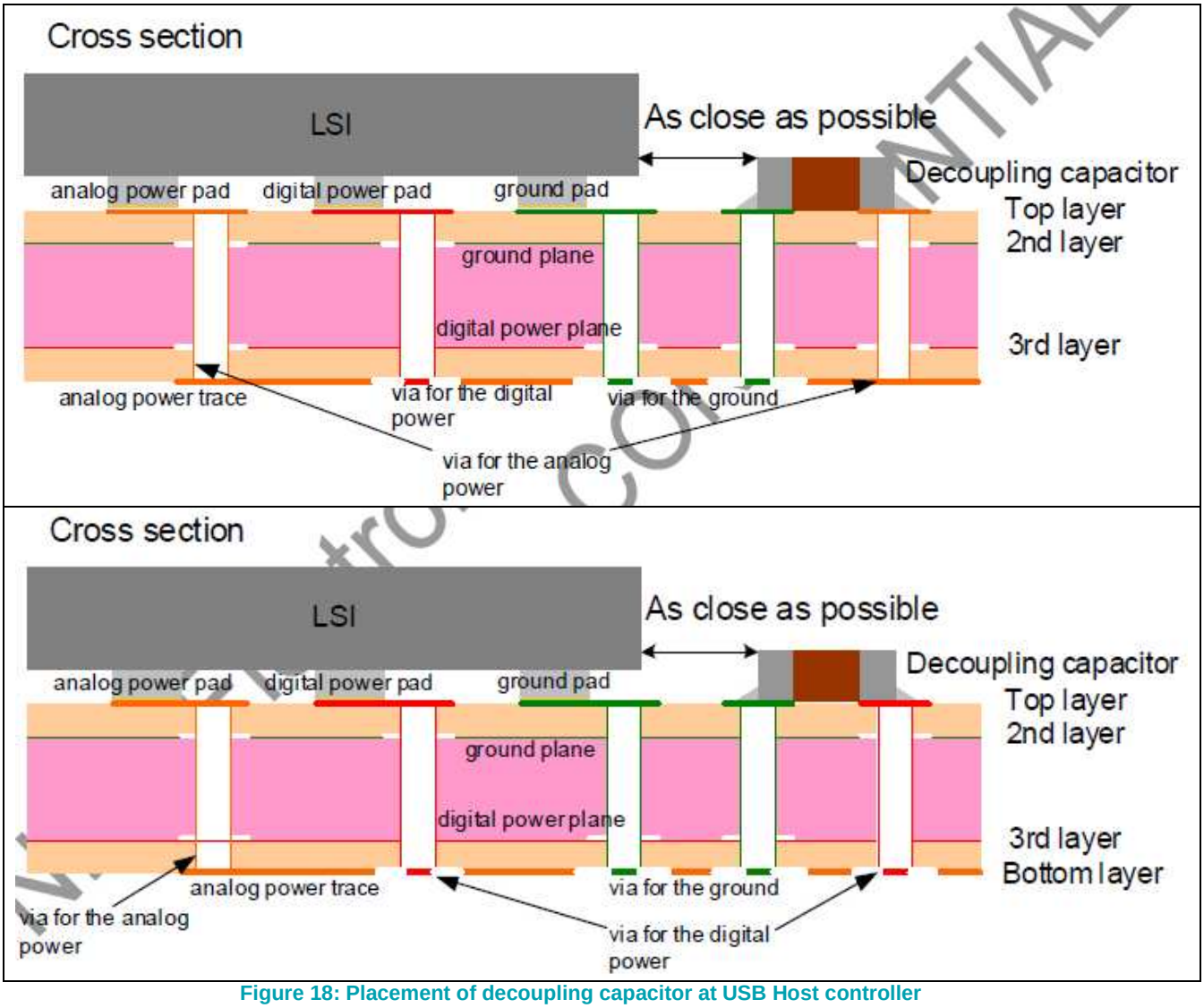


Figure 18: Placement of decoupling capacitor at USB Host controller