

Memory Systems Multiplexing for High-Performance Workstations

by S. Banerjee, May 11, 2000

Introduction

Memory technology lags behind current microprocessor performance. To avoid bottlenecks between the processor and the memory systems, sometimes a very wide data bus-based memory module is used. Using a bidirectional multiplexer and demultiplexer between the processor and the memory system helps increase the throughput. Some advanced processors, such as SUN's SPARC, handle very wide data buses (e.g., 72 bits and 144 bits). However, memory multiplexing and isolation become necessary to reduce loading on the bus, and to solve some timing constraints.

Solutions

Several multiplexer/demultiplexer components that are available from Pericom Semiconductor are specifically designed for memory system application and isolation. Memory system multiplexing can be accomplished with no-drive FET switch products (for example, Pericom's PI5C16212, PI5C16292, or PI3B16248). Use of these devices is discussed in Application Briefs 18 and 22.

When using FET switches, notice that they cannot latch signals nor do they offer any kind of current drive. So, if latching and driving the data is necessary, then the ALVCH162268 is a better solution. In the following paragraph, we discuss the use of the

ALVCH162268, which is an active drive, double-registered mux/demux (used primarily as a bus exchanger unit).

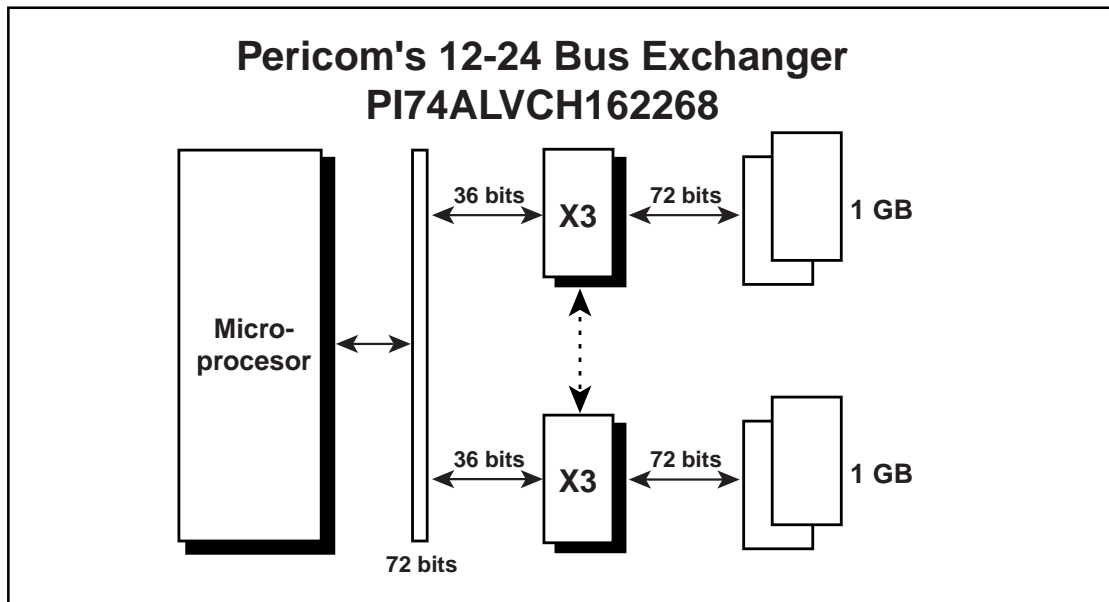
PI74ALVCH162268

Pericom's PI74ALVCH162268 functions as a 12-bit-to-24-bit multiplexer/demultiplexer. It is fabricated using Pericom's 0.5 micron CMOS technology. The device can exchange data synchronously between two buses and between two ports. All data transfers occur during the transition of the clock.

Conventional signals control the direction of the data flow through the device (for detailed operational information, refer to Pericom's PI74ALVCH162268 datasheet).

The Work Station Application diagram (see below) shows the use of the PI74ALVCH162268 in a 144-bit-to-72-bit (and vice versa) data transfer application between the CPU and the memory system. The memory system bus is 144-bits (16 bytes of data and 2 bytes of parity). Data from the memory systems is read and written in two chunks of 6-bits each. The data and the direction control of the PI74ALVCH162268 are provided by the processor, or chipsets associated with the processor.

For a complete list of interface products offered by Pericom, please log on to www.pericom.com.



Work Station Application