Interfacing HSTL to LVCMOS and HSTL to SSTL_2 Using the PI74HSTL1212

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Introduction

New signaling standards are constantly emerging. Two recent signaling standards are HSTL and SSTL-2. HSTL can be either single-ended or differential with signal swing of 1.5V. An expanded version of it, Expanded HSTL has voltage swing of 1.8V. SSTL-2 is also a fairly new signaling standard. SSTL-2 is a differential signal with voltage swing of 2.5V. Table 1 below shows some basic characteristic of some of the signaling protocols. Pericom Semiconductor offers the PI74HSTL1212 that will bridge the gap between these mixed-signal systems. The PI74HSTL1212 is a bi-directional voltage level shifter. This application note will explain how to interface HSTL to LVCMOS and HSTL to SSTL-2.

Table 1.
Electrical Characteristics for Different Types of Signals

Signal Types	V_{CC}	V_{REF}	V_{IH}(dc)	V_{IL}(dc)	V_{OH}(dc)	V_{OL}(dc)
LVCMOS	3.3V	N/A	2V (min)	0.8V (max)	2.4V (min)	0.5V (max)
SSTL_2	2.5V	1.25V	V_{REF}+0.18V (min)	V_{REF}–0.18V (max)	1.82V* (min)	0.68V* (max)
Expanded HSTL	1.8V	0.90V	V_{REF}+0.1V (min)	V_{REF}–0.1V (max)	V_{CC}A–0.4V (min)	0.4V (max)
HSTL	1.5V	0.75V	V_{REF}+0.1V (min)	V_{REF}–0.1V (max)	V_{DD}–0.4V (min)	0.4V (max)

Note: *Based on a Class I Buffer with V_{DD} = 2.5V

Interfacing HSTL to LVCMOS: A Single-ended Application

The PI74HSTL1212 is designed for 1.8V and 3.3V operation. At these operating voltage levels, V_{REF} has little affect on the output signal. Translations from 1.8V to 3.3V, and vice versa, can easily be done without any restriction.

The PI74HSTL1212 can operate down to 1.5V and 2.5V operation. When interfacing HSTL (V_{CC}A=1.5V) or Expanded HSTL (V_{CC}A=1.8V) to 2.5V LVCMOS (V_{CC}B=2.5V), V_{REF} becomes very critical. It is important that the voltage at V_{REF} is corrected, since incorrect voltage can lead to undesirable duty cycle. So the big question is... "How do we provide a third voltage to V_{REF} in a two-power supply system"? In order to provide the third voltage to V_{REF}, a voltage divider circuit is needed. Figure 1 shows the circuit diagram. V_{REF} can be calculated using the following formula:

$$V_{REF} = [R2/(R1+R2)] * V_{CC} \qquad \text{Eq. 1}$$

Calculation for V_{REF} should be limited to values between 0.850V (min) to 0.950V (max). It is also important that the calculation for V_{REF} is based on values of R2 in the range of 5K-Ohm for minimal power consumption. For values of R2 that are too high, it can couple noise to V_{REF}. Contrary, if R2 is too small, it can draw excessive current (I=V/ R2). A 0.1µF decoupling capacitor should also be placed between V_{REF} and GND to minimize V_{CC} ripple and GND bounce at V_{REF}.

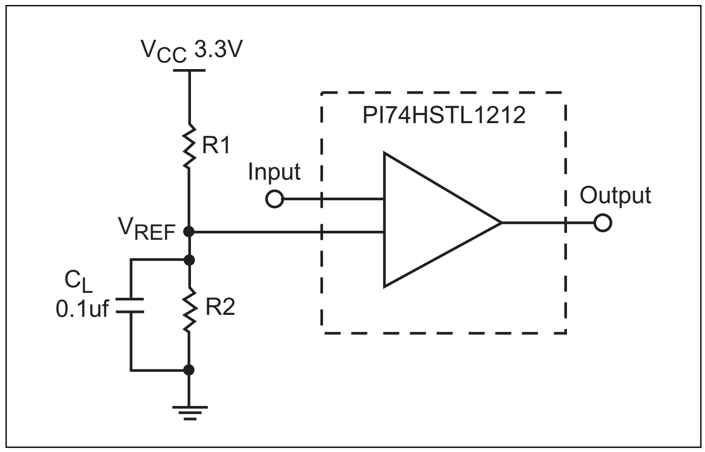

Figure. 1
Voltage divider circuit for V_{REF} in single-ended applications

It should be noted that V_{REF} is only critical when interfacing HSTL, or Expanded HSTL, to 2.5V LVCMOS. V_{REF} has no effect on the output signal when interfacing HSTL, or Expanded HSTL, to 3.3V LVCMOS. Similarly, V_{REF} has no affect on the output signal when the translation direction is going from a higher voltage to a lower voltage [i.e. translating 2.5V or 3.3V LVCMOS (B port) to 1.5V HSTL or 1.8V Expanded HSTL (A port)]. It is a good idea to keep V_{REF} in a known state. Table 2 below shows the affect of V_{REF} and how it imposed on the duty cycle. The suggested values for V_{REF} are for reference only. Actually value of V_{REF} may vary from one application to another.

Table 2. V_{REF} Values under Various Conditions
(Signal going from A port to B port)

VCCA	VCCB	VREF	Duty Cycle
1.80V →	2.50V	0.95V	~ 50% vs. 50%
1.80V →	2.50V	0V	~ 62% vs. 38%
1.50V →	2.50V	0.85V	~ 50% vs. 50%
1.50V→	2.50V	0V	~ 60% vs. 40%
1.80V →	3.30V	0.95V	~ 49% vs. 51%
1.80V →	3.30V	0V	~ 51% vs. 49%
1.50V →	3.30V	0.85V	~ 48% vs. 52%
1.50V→	3.30V	0V	~ 48% vs. 52%

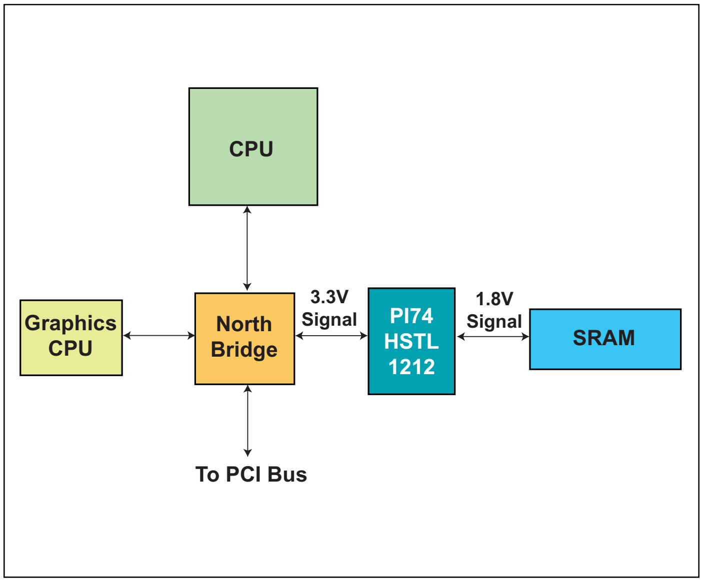

Figure 2. * General usage of the PI74HSTL1212 in a system application (Expanded HSTL interfacing with 3.3V LVCMOS)
***See Waveform in Figure 3**

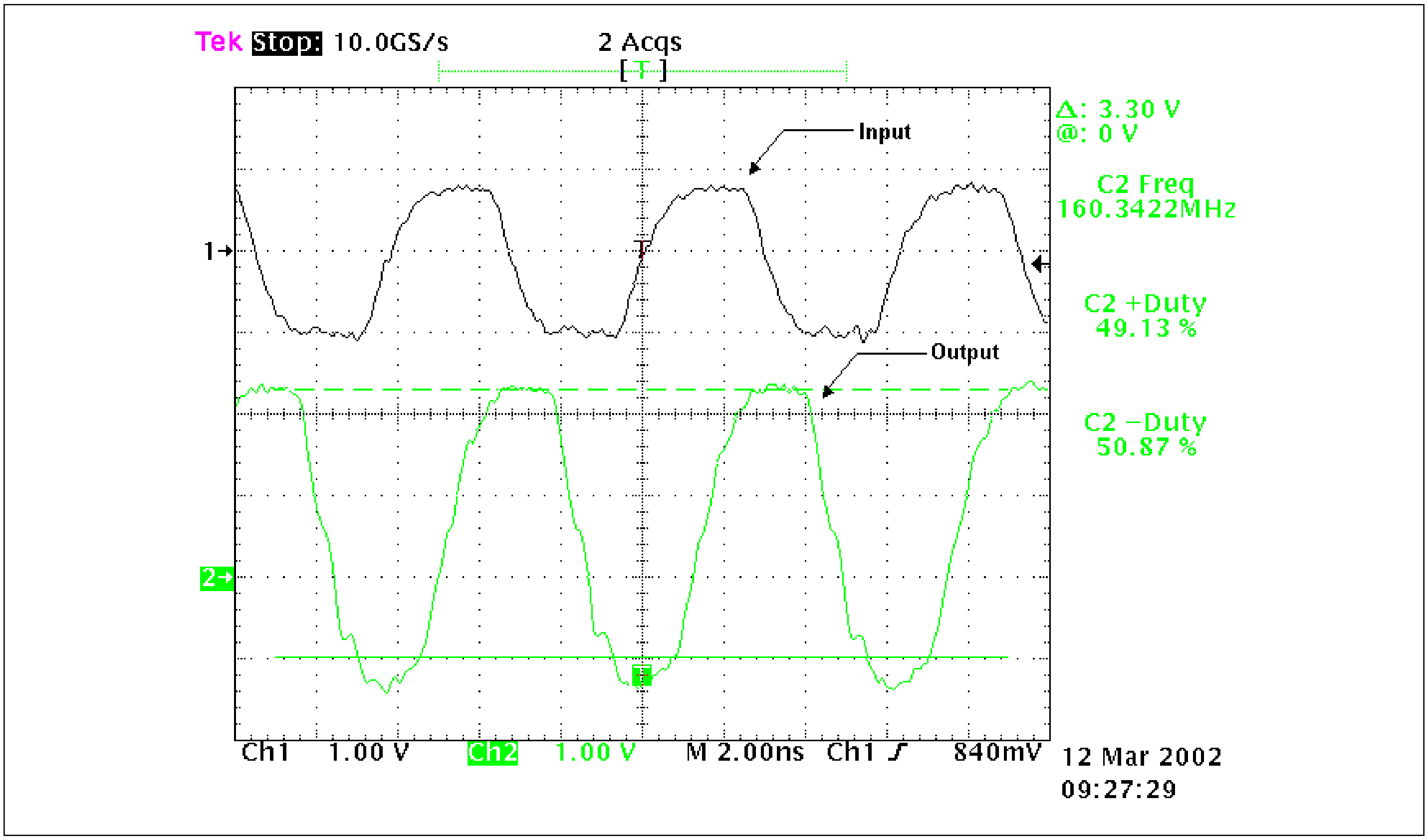

Figure 3.
A single-ended voltage translation application, 1.8V to 3.3V. Duty cycle is ~ 50%. Signal with V_{REF} = 0.95V

Below, Figures 4 and 5 show a low-voltage application with HSTL ($V_{CC}A$=1.5V) and LVCMOS ($V_{CC}B$=2.5V). Under these voltages, V_{REF} become a key factor for good duty cycle. The two figures below show the comparison between output signals when V_{REF} = 0V, and V_{REF} = 0.85V, respectively with $V_{CC}A$=1.5V and $V_{CC}B$=2.5V.

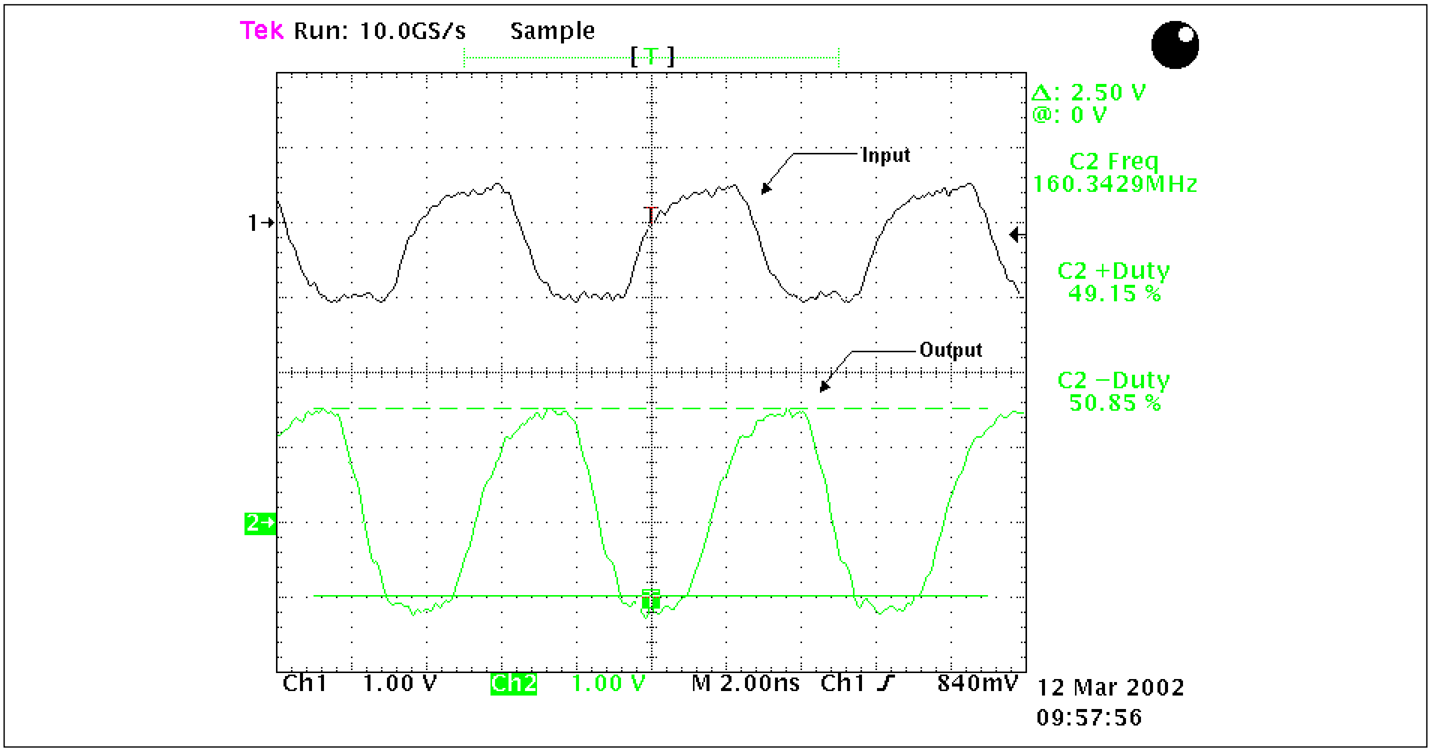

Figure 4. A single-ended voltage translation application, 1.5V to 2.5V. Duty cycle is ~ 50%. Signal with V_{REF} = 0.85V

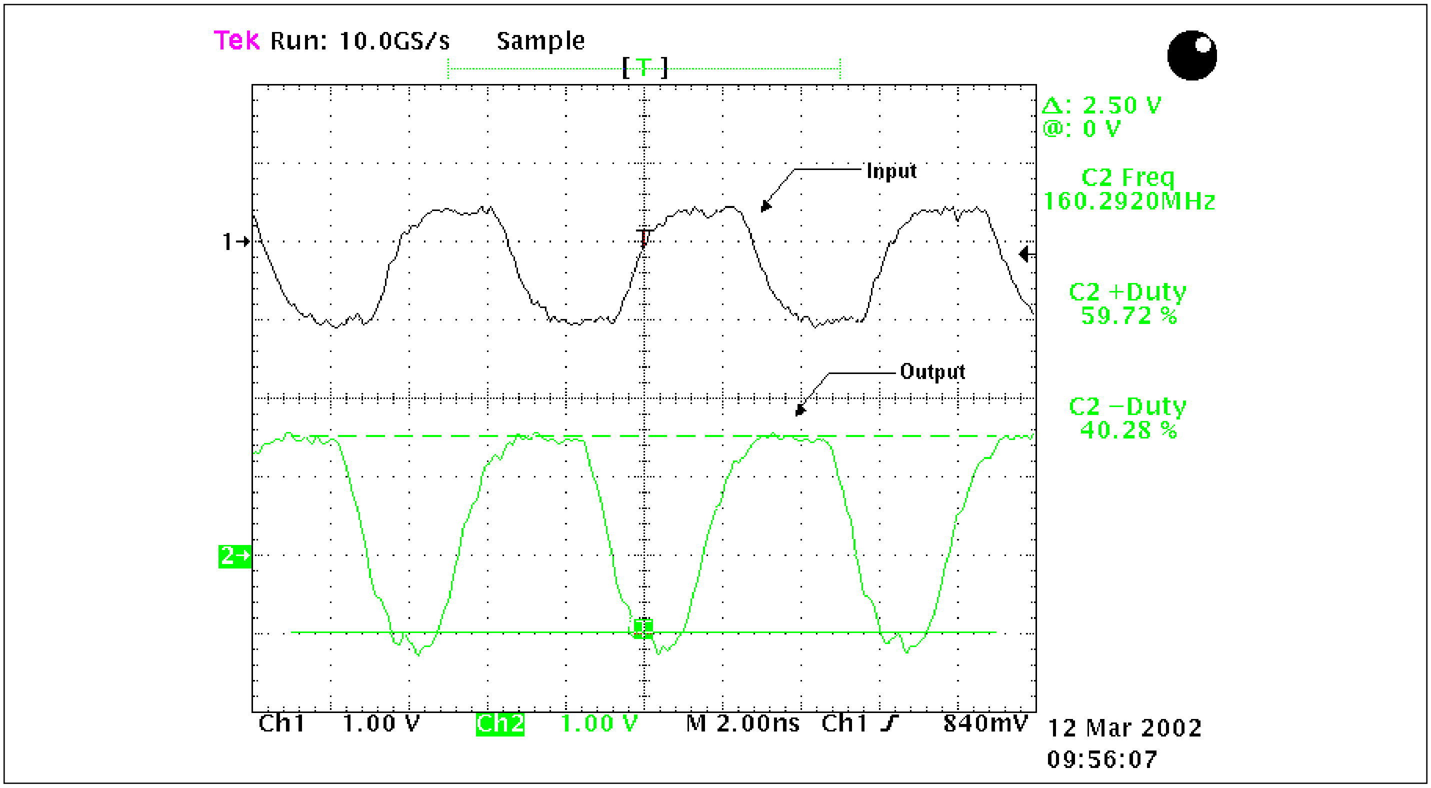

Figure 5. A single-ended voltage translation application, 1.5V to 2.5V. Duty cycle is ~ 60% vs. 40%. Signal with V_{REF} = 0V

Interfacing HSTL to SSTL_2: A Differential Application

When interfacing differential HSTL to SSTL_2, voltage levels are in the range of 1.5V and 2.5V. At these voltages, it is important that the V_{REF} value is correct since improper voltage levels will result in undesired duty cycle. As a consequence, the cross-point value will be offset from standard specification of $V_{DD}/2$. Suggested values for V_{REF} values are similar to the single-ended application. Again, similar to a single-ended application, a voltage divider circuit is needed to provide the correct voltages to V_{REF}. Figure 6 shows the circuit diagram for V_{REF} in a differential application. Figures 7 and 8 show a comparison between two differential signals with different a V_{REF} value at 0V and 0.85V respectively. From these two figures, it shows how dramatically V_{REF} can affect the duty cycle and cross point of the output signal.

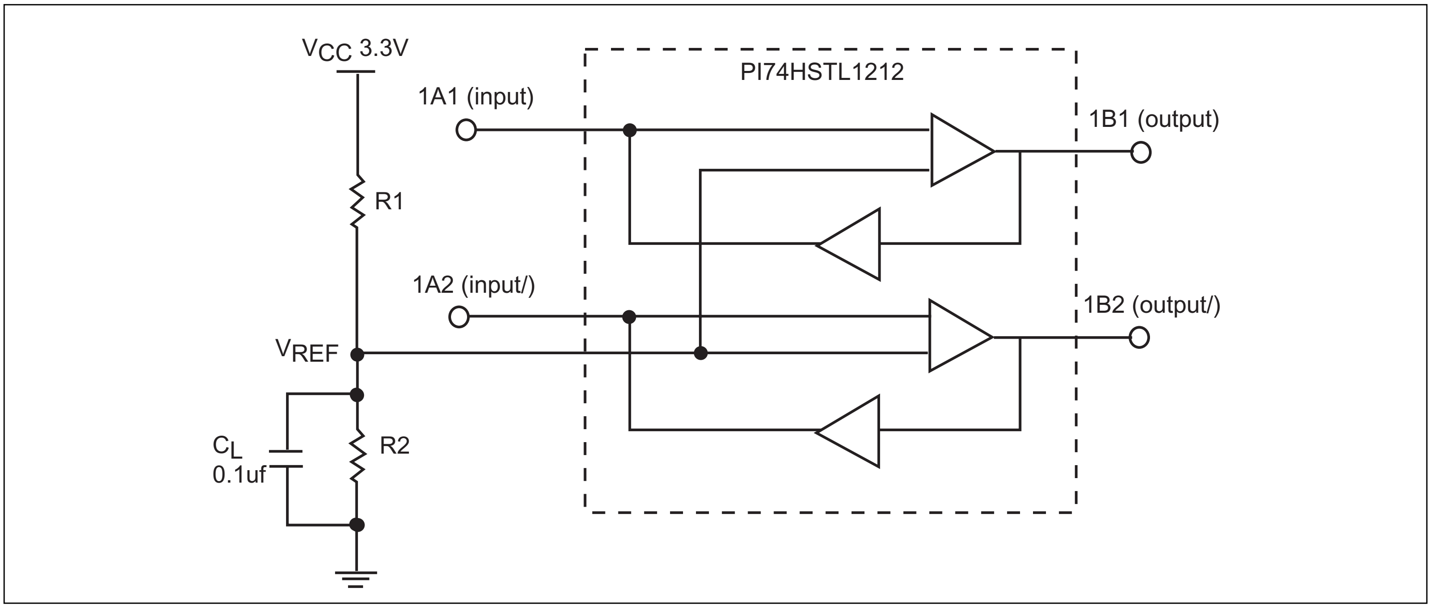

Figure 6. Voltage divider circuit for V_{REF} for differential applications

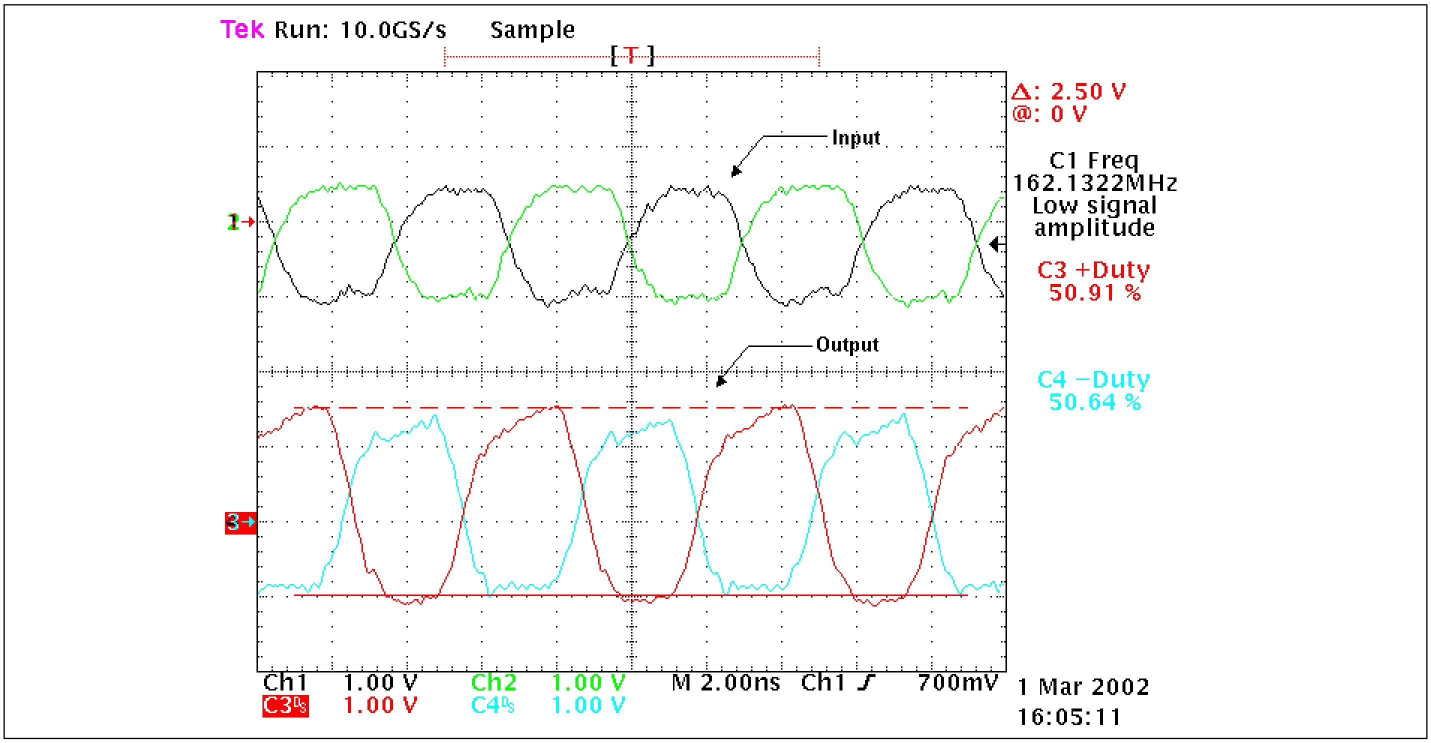

Figure 7. Differential application HSTL to SSTL_2. Duty cycle is ~ 50%.
V_{REF} is adjusted to 0.85V. As a result, cross point value is closer to $V_{DD}/2$.

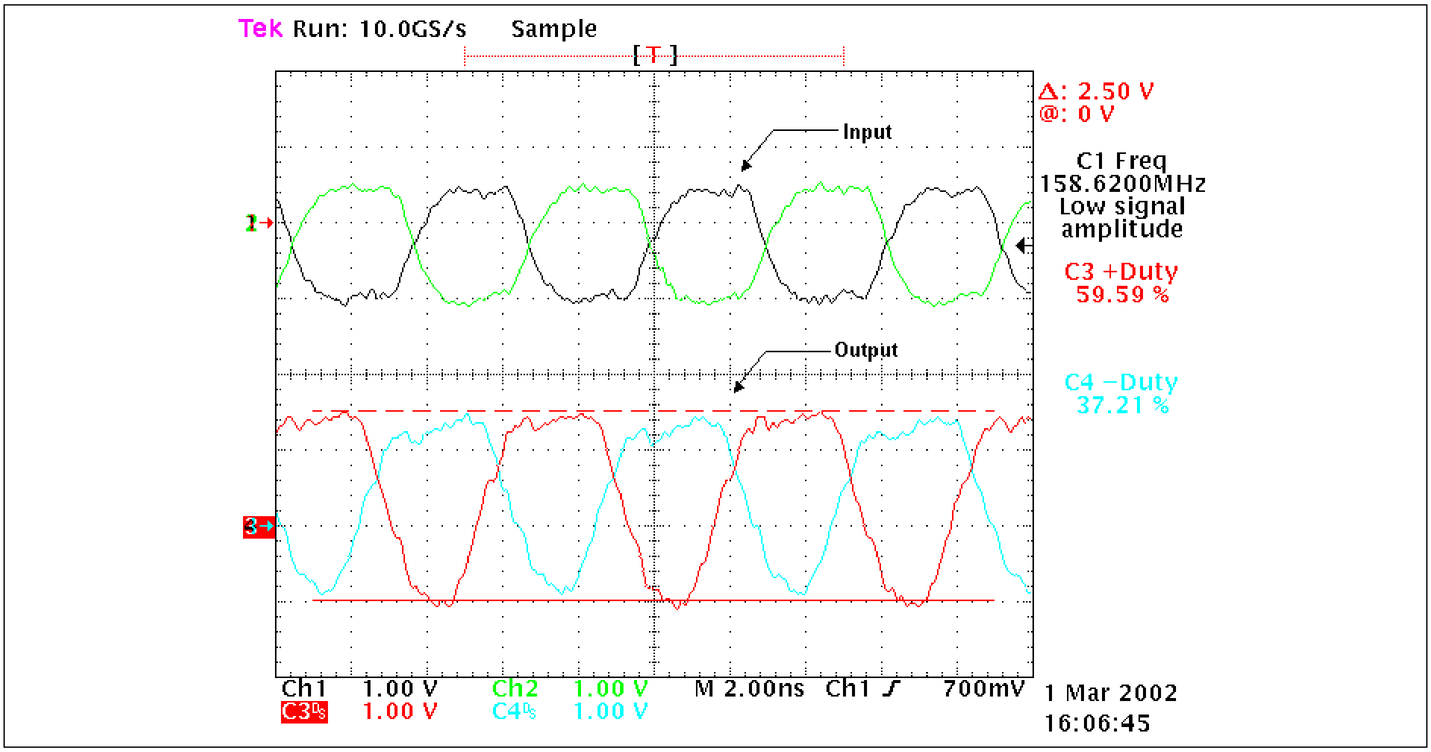

Figure 7. Differential application HSTL to SSTL_2. Duty cycle is unbalance. V_{REF} = 0V. Cross point value is offset away from $V_{DD}/2$

Design Notes

As in any design application, some basic considerations should be contemplated to get the best performance from the device. It is also important to note that as operating voltages become lower, some design limitation should be taken in consideration. Pericom Semiconductor only guaranteed what is specified in the datasheet.

Design Considerations

- A 0.47µF and 0.01µF decoupling capacitor should be connected between V_{CC} pin and GND for all V_{CC} pins. A 0. 1µF decoupling capacitor should be connected between V_{REF} and GND. Placement of all decoupling capacitors should be as close as possible to the V_{CC} pin.
- In addition to the 0.47µF, 0.01µF, and 0. 1µF decoupling capacitors connected between V_{CC} (V_{REF}) pin and GND pin of the device, there should be a sufficient amount of capacitance added to the main power supply.
- Selection of R1 and R2 should take into account noise-related issues and power consumption.
- Have proper termination to match trace impedance. Use a controlled impedance trace with proper termination to match the trace impedance. Output impedance of the device will vary according to V_{CC}. Lower V_{CC} will result in higher output impedance.
- Minimized the trace length to be as short as possible. If a differential signal is used, have equal differential trace lengths to avoid skew differences between the two differential signals.
- Avoid looping signal if possible. If serpentine technique is required to provide equal trace length, use arcs or 45^{o} turns rather than 90^{o} turns to avoid impedance discontinuities.
- Use minimal vias to avoid impedance discontinuity, which introduce more skews and reflections.
- Use a solid GND plane and do not route any signals in the GND and power planes.

Conclusion

With the emergence of low-voltage technology, the requirements of higher voltage signals interacting with lower voltage signals creates a need for the right interface. Pericom's PI74HSTL1212 is one solution to bridge these mixed-signal systems together.

References and Related App Notes:

EIA/JEDEC STANDARD: EIA/JESD8-6: High Speed Transceiver Logic (HSTL) A 1.5V Output Buffer Supply Voltage Based Interface Standard for Digital Integrated Circuits, August 1995

Pericom Application 38: Voltage Translation using PI3C3245 By: Paul Li

Pericom Application 49: Voltage Translation: The Differences between Switch Translators and the PI74AVC164245 By: Jimmy Ma