WLED Backlighting Solution for Medium-sized LCD Panel Designed with AP3616A&AP3039A

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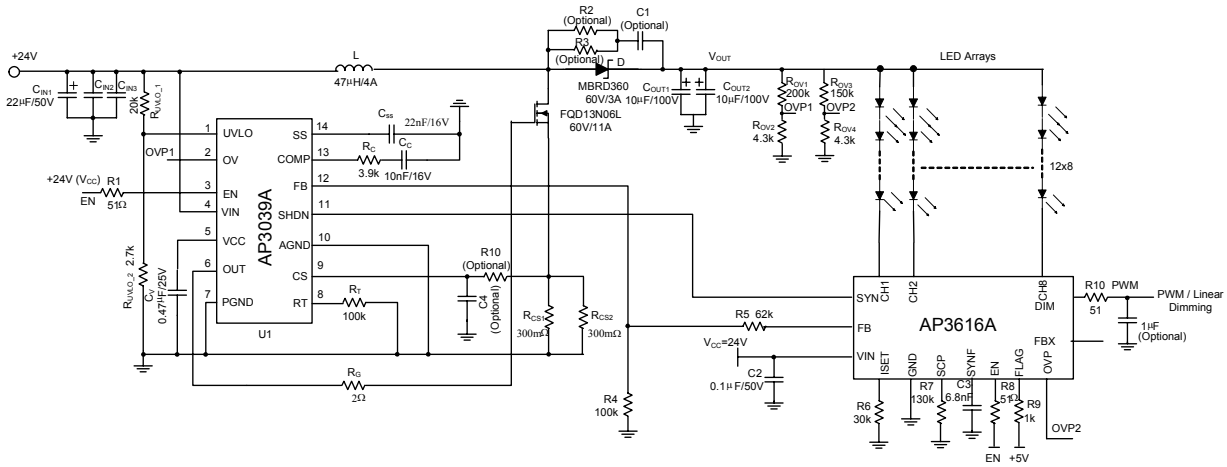
1. Introduction

With the enhancement of environment-protecting consciousness, WLED backlighting is more popular than traditional CCFL backlighting. Nowadays, WLED becomes the mainstream of the small-sized LCD panel backlighting instead of CCFL. Because of so many advantages of WLED, such as fast response, safety, long lifetime, small size and so on, WLED will become more and more important in the medium-sized and large-sized LCD panel backlighting in the future. Compared with the small-sized LCD panel, medium and large size LCD panel need tens of WLEDs. It means many new requirements are needed to be met, for example, higher drive voltage and current matching between WLED strings.

BCD semiconductor proposes a WLED backlight solution for medium-sized LCD panel under this condition.

1.1 Description to The Total Solution

The solution schematic is shown in Figure 1, which consists of two ICs: AP3616A and AP3039A. The solution can drive totally 144WLEDs, and the current matching accuracy between any two strings is within ±1.5% .The operation frequency can be adjustable, which allows trade-offs between external component size and system efficiency. WLED brightness can be adjusted by PWM dimming function. The internal soft-start circuit effectively reduces the inrush current when start-up. The solution has multiple features to protect the system from fault conditions. It features under voltage lockout protection, over voltage protection, over temperature protection, LED short circuit protection, WLED opens protection and FBX&SYN pins enable AP3616A parallel application.



Single Chip Application (12S8P)

Figure 1. BCD Solution Schematic with AP3616A&AP3039A

1.2 Description to AP3039A

The AP3039A is a high voltage low-side N-channel MOSFET controller ideal for boost converter. It adopts current-mode and its operation frequency is adjustable from 150kHz to 1MHz. In this solution, the boost converter built up by AP3039A generates a high output voltage for WLEDs.

The functional block diagram of AP3039A is shown in Figure 2. Operation process can be expressed as below: at the start of each oscillation cycle, the SR latch is set and external power switch Q (refer to Figure 1.) turns on. The switch current will increase linearly. The voltage on external sense resistor R_{CS} (refer to Figure 1.) is proportional to the switch current. This voltage is added to a stabilizing ramp and the result is fed into the non-inversion input of the PWM comparator. When this non-inversion input voltage exceeds the inversion input voltage of PWM comparator which is the output voltage level of the error amplifier EA, the SR latch is reset and the external power switch turns off. This voltage level is the amplified signal of the voltage difference between feedback voltage and reference voltage of 0.5V. It is clear that the voltage level at inversion input of PWM comparator sets the peak current level to keep the output in regulation.

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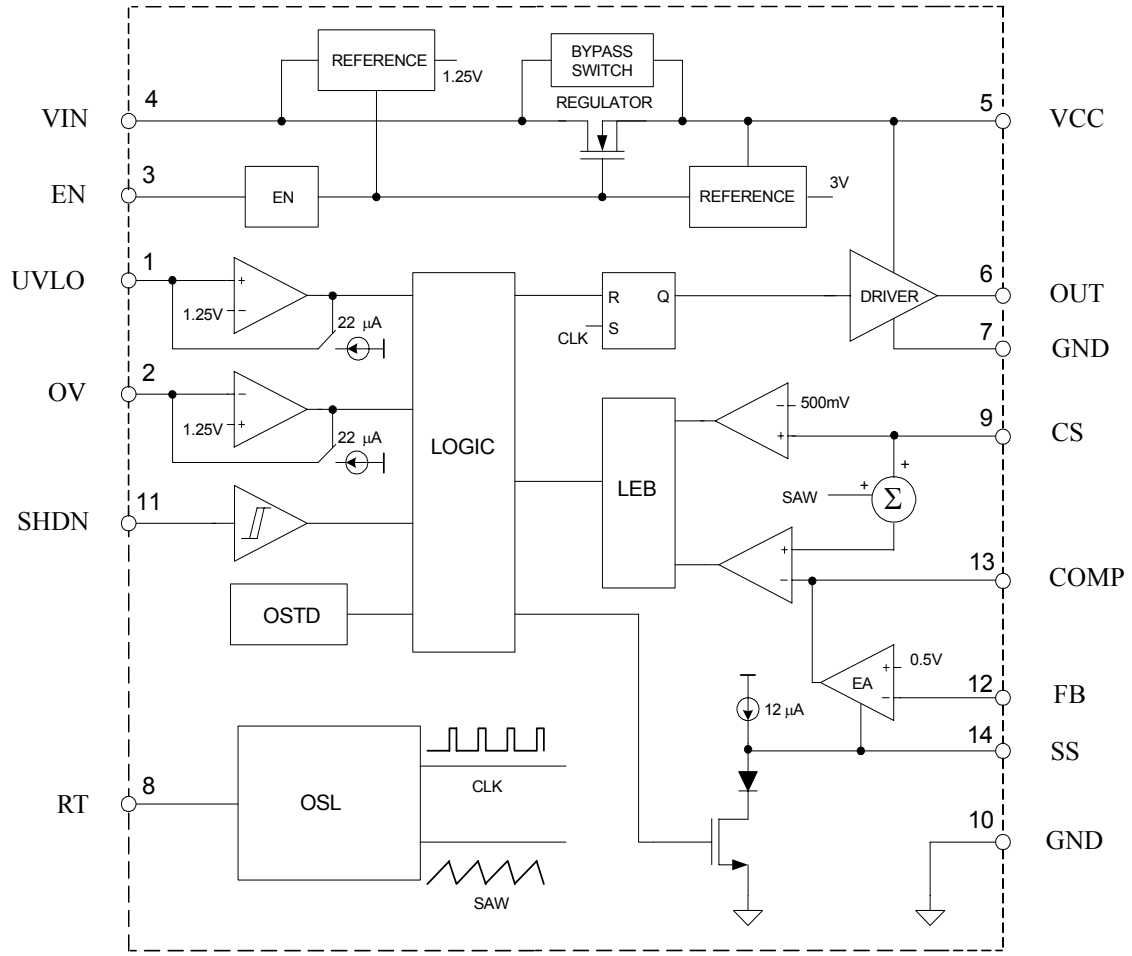

Figure 2. Functional Block Diagram of AP3039A

1.3 AP3616A Description

The AP3616A is designed for WLED display application, which contains eight well-matched current sinks to provide constant current through WLED. The full-scale WLED current can be adjusted from 40mA to 150mA per channel with an external resistor. The maximum output current is 1.2A when all the 8 channels are enabled. The SYN pin and FB pin are the interface terminals for working with AP3039A. The FB pin samples voltage of each channel, and exports the lowest voltage of the string to AP3039A. The dimming can be achieved by feeding a PWM signal to PWM pin. The functional block diagram of AP3616A is shown in Figure 3.

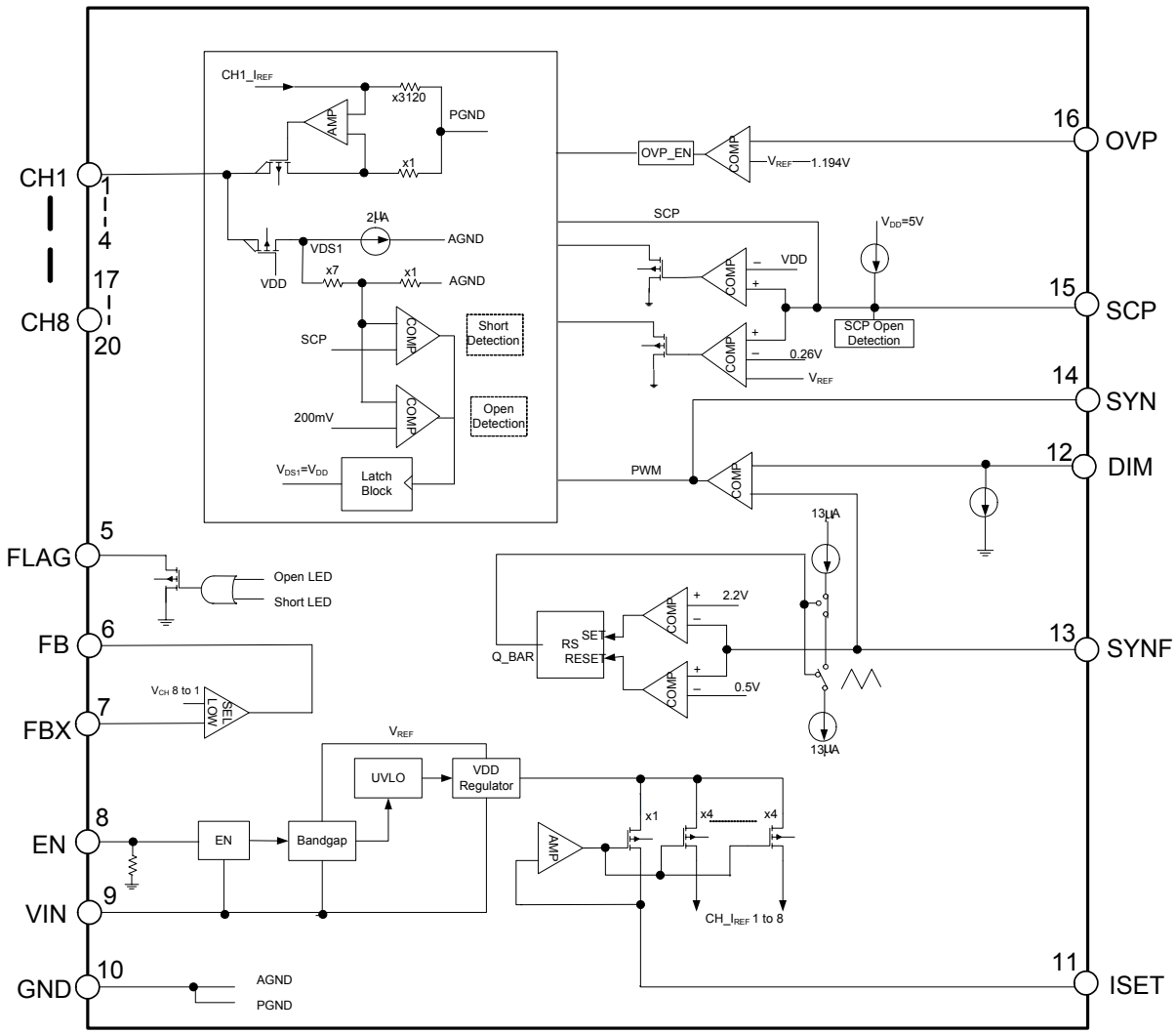

Figure 3. Function Block of AP3616A

2. Component Selection

Several peripheral components are needed in this solution shown in Figure 1. This section will give some suggestion on how to right-select these components.

2.1 Peripheral Component Selection to AP3039A

2.1.1. C_{IN1}

The input capacitor (C_{IN1}) of AP3039A filters the current peaks drawn from the input supply and reduces noise injection into the IC. A 22μF electrolytic capacitor is recommended in this typical application.

2.1.2. L

When choosing an inductor, the first step is to determine the operation mode: Continuous Conduction Mode (CCM) or Discontinuous Conduction Mode (DCM). When CCM mode is chosen, the ripple current and the peak current of the inductor can be minimized. If a small-sized inductor is required, DCM mode can be chosen. In DCM mode, the inductor ripple current and peak current are higher than those in CCM.

When the value of inductor is less than $L_{CCM(MIN)}$, the

$$L_{CCM(MIN)} = \left(\frac{V_{IN}}{V_{OUT}}\right)^2 \left(\frac{V_{OUT} - V_{IN}}{I_{OUT} * f_{osc}}\right) * \frac{\eta}{2}$$

system operates in DCM mode.

Where η is the expected efficiency (the value can be taken from an appropriate curve in the datasheet).

2.1.3. D

The boost converter requires a diode D to carry the inductor current during MOSFET off time. Schottky diodes are recommended due to their fast recovery time and low forward voltage. D should be rated to handle the maximum output voltage (plus switching node ringing) and the peak switching current. The conduction loss of diode is calculated by:

$$P_{DIODE}=I_{RMS\_OFF} * V_F$$

Where V_F is the forward voltage of the Schottky diode.

2.1.4. MOSFET Q

When selecting the power MOSFET Q, some tradeoffs between cost, size, and efficiency should be made. Losses in the MOSFET can be calculated by:

$$P_{MOS}=P_{CONDUCTION}+P_G+P_{SW}$$

Where $P_{CONDUCTION}$ is the conduction loss, P_G is gate charging loss, and P_{SW} is switching loss.

$$P_{CONDUCTION}=k_{TH} * I_{RMS\_ON}^2 * R_{DSON}$$

Where k_{TH} is the factor for the increase in on resistor of MOSFET due to heating. For an approximate analysis, the factor can be ignored and the maximum on resistor of the MOSFET can be used.

Gate charging loss, P_G, results from the current required to charge and discharge the gate capacitance of the power MOSFET and is approximated as:

$$P_G=Q_g * V_{CC} * f_{OSC}$$

Where Qg is the total gate charge of the MOSFET. Power of VCC is applied by VIN and the MOSFET driving current flows through VCC regulator. This loss P_{VCC} is estimated as:

$$P_{VCC} = (V_{IN}-V_{CC}) * Q_g * f_{OSC}$$

So, the total gate charging loss is

$$P_{G\_TOTAL}= P_G + P_{VCC}$$

The total gate charging loss occurs in IC and not in the MOSFET itself actually. Switching loss, P_{SW}, occurs in transition period as the MOSFET turns on and off. This loss is consisted of turn-on loss and turn-off loss.

$$P_{TURN-ON} = \frac{1}{6}\left(I_{IN} - \frac{\Delta I_L}{2}\right) * V_{OUT} * t_{RISING} * f_{OSC}$$

$$P_{TURN-OFF}\left(I_{IN} + \frac{\Delta I_L}{2}\right) * V_{OUT} * t_{FALLING} * f_{OSC}$$

$$\Delta I_L = \frac{(V_{OUT} - V_{IN}) * V_{IN}}{L * f_{OSC} * V_{OUT}}$$

$P_{SW}=P_{TURN-ON}+P_{TURN-OFF}$

The maximum drain-to-source voltage applied across the MOSFET is V_{OUT} plus the ring due to parasitic inductance and capacitance. The maximum drive voltage at the gate of the MOSFET is V_{CC} plus the ring from gate to source. So the voltage rating of the MOSFET selected must be able to withstand the maximum drain-to-source voltage as well as the maximum gate-to-source voltage. The MOSFET with V_{DS}=60V and V_{GS}>10V is recommended in typical application.

2.1.5 C_{OUT}

The output capacitor of the boost converter is used for output filtering and keeping the loop stable. The ESR value is the most important parameter of the C_{OUT}, because it directly affects the system stability and the output ripple voltage.

The total output ripple can be calculated by the following equations:

$\Delta V_{OUT}=\Delta V_{OUT(COUT)}+\Delta V_{OUT(ESR)}$

$$\Delta V_{OUT(COUT)} = \frac{I_{OUT}}{C_O} * \left(\frac{V_{OUT} - V_{IN}}{V_{OUT} * f_{OSC}}\right)$$

$\Delta V_{OUT(ESR)}=I_{L\_PEAK} * R_{ESR(COUT)}$

$$I_{L\_PEAK} = \frac{\Delta I_L}{2} + I_{IN}$$

Where $\Delta V_{OUT(COUT)}$ is caused by the charging and discharging on the output capacitor, and $\Delta V_{OUT(ESR)}$ is caused by the capacitor's equivalent series resistor (ESR).

To get low output ripple, a low ESR capacitor is a good choice. The capacitance of 20μF is recommended.

2.1.6. R_{UVLO1}& R_{UVLO2}

The AP3039A contains an under voltage lockout (UVLO) circuit. Two resistors R_{UVLO1}, R_{UVLO2} are connected from UVLO pin to GND and VIN pin respectively (refer to Figure 4.). The resistor divider must be designed such that the voltage on the UVLO pin is higher than 1.25V when V_{IN} is in the desired operating range. If this under voltage threshold is not met, all functions of AP3039A are disabled and the system remains in a low-power standby state. The UVLO threshold rising edge can be calculated by:

$$V_{IN\_UVLO} = \left(\frac{R_{UVLO1}}{R_{UVLO2}} + 1\right) * 1.25V$$

The UVLO hysteresis is accomplished by an internal 22μA current source which is switched on or off into the impedance of the set-point divider. When the UVLO threshold is exceeded, the current source is activated. When the UVLO pin voltage falls below the threshold, the current source is turned off. The UVLO hysteresis can be calculated by:

$V_{UVLO\_HYS}=R_{UVLO1}*22\mu A$

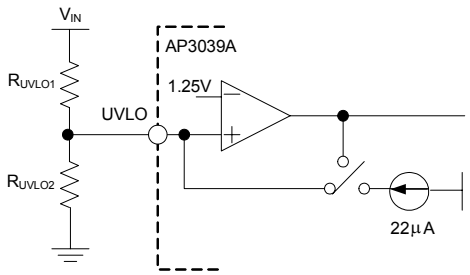

Figure 4. UVLO Protection Circuit

2.1.7. R_{OV1}&R_{OV2}

The AP3039A has an over voltage protection (OVP) circuit. Two resistors R_{OV1}, R_{OV2} are connected from OV pin to ground and the output V_{OUT} (refer to Figure 5). When the loop is open or the output voltage becomes excessive in any case, the voltage on OV pin will exceed 1.25V, as a result, all functions of AP3039A are disabled and the output voltage will fall. The OVP threshold rising edge can be calculated by:

$$V_{OUT\_OVP} = \left(\frac{R_{OV1}}{R_{OV2}} + 1\right) * 1.25V$$

The OVP hysteresis is accomplished with an internal 22μA current source and the operation process is the same as UVLO. The OVP hysteresis can be calculated by: $V_{OVP\_HYS}=R_{OV1} * 22\mu A$

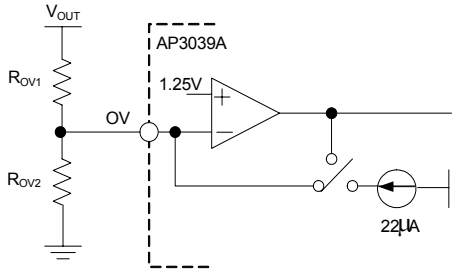

Figure 5. OVP Protection Circuit

2.1.8. R_T

An external resistor R_T is connected from RT pin to GND to set the operating frequency (refer to Figure 1). Operating frequency range is from 150kHz to 1MHz (as shown in Table 1). High frequency operation optimizes the regulator for the smallest component size, while low frequency operation can reduce the switch losses.

Table 1. Frequency Selection

R_T (kΩ)	Operating Frequency (kHz)
470	150
390	200
147	400
95	600
68	800
51	1000

2.1.9. C_{SS}

The AP3039A has a soft-start circuit to limit the inrush current during start-up. The soft-start feature allows the boost converter output to gradually reach the initial steady state output voltage, thereby reducing startup stresses and current surges. The startup time is controlled by an internal 12μA current source and an external soft-start capacitor C_{SS} which connected from SS pin to GND (refer to Figure1). At power on, after the V_{IN} UVLO threshold is satisfied, the internal 12μA current source charges the external capacitor CSS. The capacitor voltage will ramp up slowly and limit V_{COMP} and the switch current.

2.1.10. C_V

The AP3039A includes an internal low dropout linear regulator with the output pin VCC. This pin is used to power internal PWM controller, control logic and MOSFET driver. On the condition that $V_{IN} \geqslant 13.5V$, the regulator generates a 10V supply. If $6V \leqslant V_{IN} \leqslant 12.5V$, V_{CC} is equal to V_{IN} minus drop voltage across bypass switch. When V_{IN} is less than 6V, connect VCC to VIN.

The VCC pin of AP3039A should be decoupled with a ceramic capacitor placed as close to the AP3039A as possible. This capacitor keeps V_{CC} voltage steady when the system operates at a high frequency. The X5R or X7R ceramic capacitor should be adopted as decoupling capacitor because of their good thermal stability, and A 0.47μF capacitor is recommended.

2.1.11. R_{CS}

An external resistor R_{CS} is connected from CS pin to PGND to detect switch current signal for current-mode boost converter. The current limit threshold voltage VCS of AP3039A is fixed at 500mV. The required resistor R_{CS} is dependent to the peak inductor current at the end of the switch on-time, and can be calculated by the following equations:

$$R_{CS\_MAX} = \frac{V_{CS}}{I_{L\_PEAK}}$$

$P_{RCS}=I_{RMS\_ON}^2 * R_{CS}$

$$I_{RMS\_ON}^{2} = \frac{V_{OUT} - V_{IN}}{V_{OUT}} * \left(I_{IN}^{2} + \frac{\Delta I_L^{2}}{12} \right)$$

2.2 AP3616A Peripheral Component Selection

2.2.1 C_{IN2}

The VCC pin of the AP3616A should be decoupled with a ceramic capacitor placed as close to the AP3616A as possible. The X5R or X7R ceramic capacitor should be adopted as decoupling capacitor because of their good thermal stability, and the capacitance of 0.1μF is recommended.

2.2.2 R_{ISET}

The WLED current can be set up to 150mA per channel via ISET pin. To set the reference current (I_{SET}), connect a resistor (R_{ISET}) between this pin and ground. The relationship of ISET and RISET can be expressed by:

I_{SET}=1.194V/R_{ISET}

This reference current is multiplied internally with a gain (k) of 3120, and then mirrored on all enabled channels. This sets the WLED current, referred to as 100% current (I_{CHX}). The value can be calculated by the following formula:

I_{CHX} =k*I_{SET}

The WLED current can be reduced from 100% by PWM dimming control.

2.2.3 R_{FB}

FB pin is an interface terminal, which samples the voltage of each channel, and outputs the lowest voltage of the string to DC/DC converter (i.e. AP3039A). The value can be calculated by the following formula:

$$V_{FB} = 0.5 * \left(\frac{R_{FB1} + R_{FB2}}{R_{FB2}} \right)$$

The maximum channel current that the AP3616A can provide is related to the voltage of FB pin, $I_{CH(MAX)}$ in different value of FB is shown in table 2.

Table 2. $I_{CH(MAX)}$ Selection (Recommended Setting)

$I_{CH(MAX)}$ (mA)	$V_{FB(MIN)}$ (V)	R_{FB1} (kΩ)	R_{FB2} (kΩ)
40	0.3	0	100
60	0.5	0	100
120	0.8	62	100
150	1.0	100	100

2.2.4 R_{SCP}

The LED short trigger voltage can be set via SCP pin. This pin is used to set the LED short circuit protection voltage level. To set the Trigger voltage, connect a resistor (R_{SCP}) between this pin and ground. The relationship of V_{SCP} and R_{SCP} can be expressed by:

V_{SCP}=13.5μA * R_{SCP}

The circuit will trigger the LED short protection when the LED short voltage above this level (V_{SCP}). A 130kΩ resistor is recommended.

2.2.5 C_{SYNF}

This capacitor is used to set synchronous PWM frequency. A nF level of cap should be connected to this pin to set PWM frequency at about 80Hz to 25kHz. A 6.8nF capacitor is recommended. The frequency in different cap value is shown in table 3.

Table 3. SYNF Selection

C_{SYNF}(nF)	Frequency (kHz)
33	0.108
6.8	0.54
0.22	15.4

2.2.6 ROV3 &ROV4

The AP3616A has an over voltage protection (OVP) circuit. Two resistors ROV3, ROV4 are connected from OVP pin to ground and the output (refer to Figure 1.)

When the loop is open or the output voltage becomes excessive in any case, the voltage on OVP pin will exceed 1.194V, then AP3616A will start the LED open protection. The OVP threshold rising edge can be calculated by:

$$V_{OUT-OVP} = \left(\frac{R_{OV3}}{R_{OV4}} + 1\right) * 1.194V$$

3. Operation

3.1 Initialization

When peripheral components are ready, the solution should be initialized following the steps below.

3.1.1 I_{CHX}

Set the WLED current of all used channels according to the application, the detail information please refers to 2.2.2 section.

3.1.2 R_{FB}

Set the FB voltage level (i.e. the maximum channel current), the detail information please refers to 2.2.3 section.

3.1.3 R_{SCP}

Set the LED short circuit protection voltage level, the detail information please refers to 2.2.4 section.

3.1.4 C_{SYNF}

Set the synchronous PWM frequency, the detail information please refers to 2.2.5 section.

3.1.5 R_{OV3} & R_{OV4}

Set the over voltage protection voltage level, the detail information please refers to 2.2.6 section.

3.2 Dimming

After initialization is finished, the system goes into normal working mode, when the dimming function of the solution provides less WLED color distortion and can be used to adjust the LCD brightness according to different application.

The AP3616A provides two dimming methods: DC voltage input (linear dimming) or external PWM signal (PWM dimming).

3.2.1 Linear Dimming

Under this mode, the DC Voltage (0.5V to 2.2V) added in the DIM pin, compares with the triangle wave in SYNF pin. An example for linear dimming is shown in Figure 5. If the voltage is higher than V_{SYNF} , the WLED turns on and the 100% current flows through WLED. If the voltage is lower than V_{SYNF}, the WLED turns off and almost no current flows through WLED. So the average current through WLED is changed and the brightness is adjusted. An example for PWM dimming is shown in Figure 6.

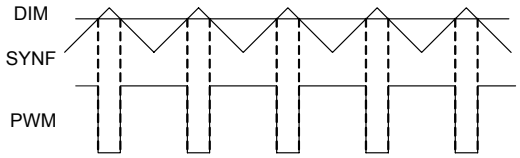

Figure 6. Linear Dimming Mode (Example)

3.2.2 PWM Dimming

Under this mode, all enabled channels can be adjusted at the same time and the brightness can be adjusted from 1%*I_{CHX} to 100%*I_{CHX}. During the "high level" time of the PWM signal, the WLED turns on and the 100% current flows through WLED. During the "low level" time of the PWM signal, the WLED turns off and almost no current flows through WLED. So the average current through WLED is changed and the brightness is adjusted. The external PWM signal applied to DIM pin should be in the range of 100Hz to 25kHz for good dimming accuracy.

An example for PWM dimming is shown in Figure 6. All 8 channels are set to the maximum current I_{CHX_MAX} at the beginning. When a 50% duty cycle PWM signal is applied to DIM pin, average current

valued 50%*I_{CHX_MAX} flows through the 8 channels. When an 80% duty cycle PWM signal is applied to DIM pin, average current valued 80%*I_{CHX_MAX} flows through the 8 channels.

Under PWM dimming mode, the AP3616A gives a signal synchronous with PWM signal to the AP3039A via SYN pin. During the "high level" time of the PWM signal, the AP3039A supplies the proper output voltage to WLEDs according to the signal of FB pin from the AP3616A. During the "low level" time of the PWM signal, the AP3039A keeps the output voltage regardless of the signal of FB pin, that is to say, signal of FB pin from the AP3616A can not control the boost loop during PWM "low level" time.

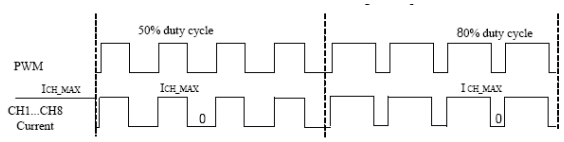

Figure 7. PWM Dimming Mode (Example)

3.3 Protection

3.3.1 UVLO Protection

This solution involves the UVLO protection. Both the AP3039A and AP3616A have the UVLO function. The system is disabled until V_{IN} of AP3039A exceeds the UVLO threshold and V_{CC} of AP3616A exceeds the UVLO threshold at the same time. The UVLO threshold and hysteresis of AP3039A can be set according to different application. The detailed information please refers to 2.1.6 section. The UVLO threshold and hysteresis of AP3616A is fixed, the typical UVLO threshold value is 3.8V and the typical hysteresis value is 200mV.

3.3.2 Over Voltage Protection

The solution involves the OV protection. Set the proper OV threshold according to the number of WLEDs in different applications. The detailed information please refer to 2.1.7 and 2.2.6 section. Under normal working mode, if any channel is open or excessive output voltage was added, the output will go high. Once the output voltage reaches the OV protection threshold (1.194V), the AP3616A will start the LED open protection and If OV pin reaches the AP3039A OVP threshold 1.25V , the AP3039A will turn off the external MOSFET and the system goes into disabled mode . The AP3039A will start to work after the output voltage drops below the OV protection threshold and the system goes into enabled mode again.The triggering voltage of AP3616A should be lower than the OVP voltage of AP3039A.

3.3.3 Open WLED Protection

This solution involves the self-check and protection against open WLED. If any used WLED string opens, voltage on the corresponding CHX pin goes to zero and the FB pin of AP3616A exports the zero voltage to AP3039A, V_{OUT} will boost up until the voltage at the AP3616A OVP pin reaches an approximate 1.194V threshold. The IC will automatically ignore the open string(s) whose CHX pin voltage is less than 100mV and the remaining string(s) will continue operating. Once the circuit returns to normal operation, the voltage on the CHX pin is regulated to the normal level. An example is shown in Figure 8. CH1, CH2 and CH3 are used channels while CH4 to CH8 are unused channels. If CH3 opens for any reason, the voltage on CH3 goes to zero. FB pin of AP3616A samples the lowest voltage of CH1, CH2 and CH3, so FB pin exports the zero voltage to the AP3039A and the AP3039A makes the output voltage go high. As a result, the voltage at the AP3616A OVP pin reaches an approximate 1.194V threshold, the AP3616A begins checking the opened channel. After finding the open channel CH3, the AP3616A removes the CH3 from boost control loop, and boost converter returns to normal operation. Once the system returns normal operation, the voltage on the CH1 and CH2 are regulated to the normal level.

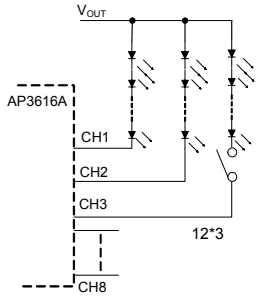

Figure 8. Open WLED Protection (Example)

3.3.4 Short WLED Protection

The system can avoid destroy when some WLEDs are short. CH1 to CH8 pin of the AP3616A can endure at least 60V high voltage. During normal operation, any short-circuited LED will cause the corresponding LED pin voltage to rise. If any LED pin voltage exceeds 8 times the voltage at VSCP pin, the corresponding LED current sink will be latched off. The LED short trigger voltage can be set by using the SCP pin with connecting a resistor (R_{SCP}) between this pin and ground. The detailed information please refer to 2.2.4 section. The circuit will trigger the LED short protection once the LED short voltage above this level (V_{SCP}).

An example is shown in Figure 9, even though the WLEDs of CH3 are all short for any reason, the CH3 LED pin voltage rise to V_{OUT} immediately and exceeds 8 times the voltage at VSCP pin we set, the corresponding CH3 LED current sink will be latched off. The AP3616A can still keep safety.

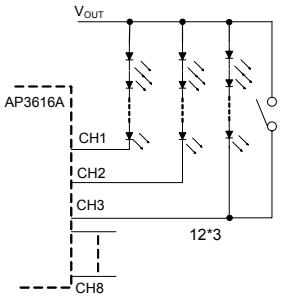

Figure 9. Short WLED Protection (Example)

3.3.5 Over Temperature Protection

The solution involves over temperature protection (OTP). Both the AP3039A and AP3616A have the OTP circuit. The threshold of the OTP is typically 160 ℃ , and the hysteresis of the OTP is typically 20 ℃ .

3.3.6 Soft-start

The AP3039A in the solution has a soft-start circuit to limit the inrush current during startup. The detailed information please refers to 2.1.9 section.

3.3.7 FLAG

The AP3616A has an error flag pin. This pin is an open drain, which connects to a DC voltage with a resistor. During normal operation, the flag pin puts low, when LED load goes to error (short or open), the flag pin pulls high.

4. PCB Layout Guideline

The system performance can be seriously affected due to poor layout. To produce an optimal solution for medium LCD backlighting, good layout and design of the PCB are as important as the component selection. The following PCB layout guideline should be considered:

4.1 There are two high-current loops in the solution. One is the high-current input loop, and the other is the high-current output loop. The high-current input loop goes from the positive terminal of the C_{IN1}&C_{IN2}&C_{IN3} to the inductor, to the MOSFET, then to the current-sense resistor, and to the C_{IN1}&C_{IN2}&C_{IN3} negative terminal. The high-current output loop goes from the positive terminal of the C_{IN1}&C_{IN2}&C_{IN3} to the inductor, to the diode, to the positive terminal of the C_{OUT}, reconnecting between the C_{OUT} and the C_{IN1}&C_{IN2}&C_{IN3} ground terminals. Minimize the area of the two high-current loops to avoid excessive switching noise. The trace connected these two high-current loops must be short and thick.

4.2 Create two ground islands. One is called power ground island (PGND), the other is called analog ground island (AGND). PGND consists of C_{IN1}&C_{IN2}&C_{IN3} and C_{OUT} ground connections and negative terminal of the current-sense resistor R_{CS}. Maximizing the width of the PGND traces improves efficiency and reduces output voltage ripple and noise spike. AGND consists of the OV and UVLO detection-divider ground connection, the ISET and RT resistor ground connections, C_V, C_{SS} and C2 ground connections, and the device`s exposed backside pad. Connect the AGND and the PGND directly to the exposed backside pad. Make no other connections between these separate ground planes.

4.3 Place the bypass capacitor C_V and C2 as close to the device as possible. The ground connection of these

capacitors should be connected directly to AGND pins with a thick trace.

4.4 Keep the feedback trace far away from the switching node, and make sure the feedback trace is short and thick. Place the OV and UVLO detection-divider resistors as close to the OV pin and UVLO pin as possible respectively. The divider`s center trace should be kept short. Avoid running the sensing trace near switching node.