AN1167

DGD2181M DGD21814M Application Note

The DGD2181M and DGD21814M, High-Side/Low-Side gate drivers are used to optimally drive the gate of MOSFETs or IGBTs. DGD2181M package is SO-8. DGD21814M package is SO-14 with a separate logic ground pin Vss, this can be used when required to separate power ground and logic ground. Below (Figure 1) is an example application using the DGD2181M with MOSFETs as part of the power switching circuit in the primary side of a full-bridge converter. In this application note, the important parameters needed to design in the DGD2181M and DGD21814M are discussed. The main sections are bootstrap resistor, diode, and capacitor selection, gate driver component selection, decoupling capacitor discussion, and PCB layout suggestions.

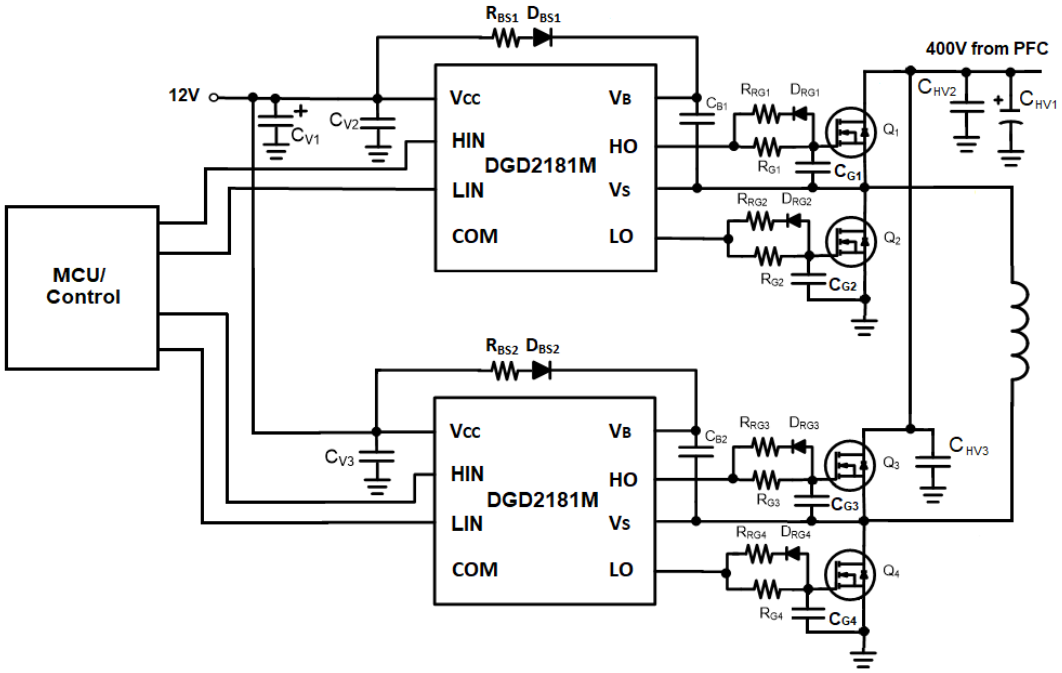

Figure 1. Primary side of full-bridge converter with DGD2181M

Bootstrap Component Selection

Bootstrap Resistor

Considering Figure 1, when the low-side MOSFET (Q2 or Q4) turns on, Vs pulls to GND and the bootstrap capacitor (C_{B1} or C_{B2}) is charged. When the high-side MOSFET (Q1 or Q3) is turned on, V_S swings above Vcc and the charge on the bootstrap capacitor (C_B) provides current to drive the IC high-side gate driver. The first charge of C_B from Vcc through the bootstrap resistor (R_{BS1} or R_{BS2}) and bootstrap diode (D_{BS1} or D_{BS2}) occurs when power is first applied and the low-side turns on the first time. At this time the charge current is the largest as typically C_B is not discharged fully at each cycle.

A bootstrap resistor (R_{BS}) is included in the bootstrap circuit to limit the inrush current that charges C_B when Vs pulls below Vcc; this inrush current is largest with the first charge. Limiting inrush current is desirable to limit noise spike on Vs and COM, potentially causing shoot-through. The amplitude and length of time of the inrush current is determined mostly by the component value of R_{BS} and C_{BS} as well as Vcc level. The aim in resistor selection for the application is to slow down the inrush current but have minimal effect on the RC time constant of charging C_{BS}.

Typically, values for R_{BS} are 3Ω to 10Ω, enough to dampen the inrush current but have little effect on the V_{BS} turn on. Figures 2-5 illustrate the effect of different R_{BS} values.

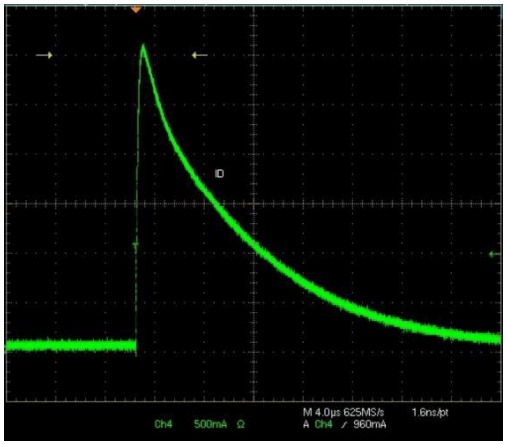

Figure 2. Bootstrap Peak inrush current ≈3A with RBS=3Ω, CBS=2.2µF

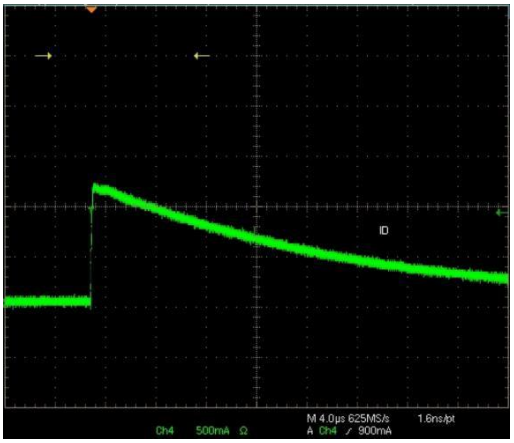

Figure 3. Bootstrap Peak inrush current ≈1.2A with RBS=10Ω, CBS=2.2µF

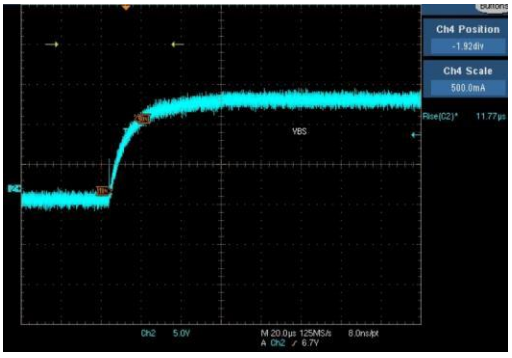

Figure 4. VBS Rise Time (11.8µs) with RBS=3Ω, CBS=2.2µF

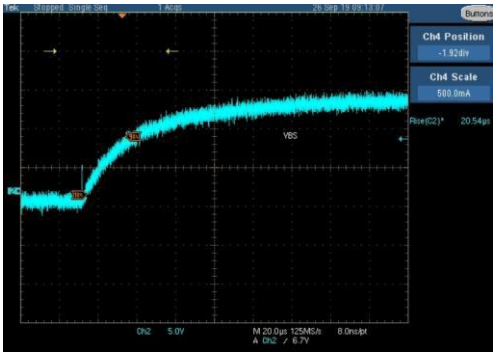

Figure 5. VBS Rise Time (20.5µs) with RBS=10Ω, CBS=2.2µF

Bootstrap Diode

The chosen bootstrap diode (D_{BS}) should be rated higher than the maximum rail voltage since the diode must be able to block the full rail voltage and any spikes seen at the V_S node. The diode's current rating is simply the product of total charge (QT) required by the HVIC (High Voltage Integrated Circuit) and the switching frequency. An ultrafast recovery diode is recommended to minimize any delay of charging the C_{BS} cap. A 1A ultrafast recovery diode is typical for DGD2181M and DGD21814M applications.

Bootstrap Capacitor

The initial step in determining the value of the bootstrap capacitor is to determine the minimum voltage drop (ΔV_{BS}) that can be guaranteed when the high-side device is turned on. In other words, the minimum gate-source voltage (V_{GS_min}) must be greater than the UVLO of the high-side circuit, specifically V_{BSUV-} level. Therefore, if V_{GS_min} is the minimum gate-source voltage such that:

$V_{GS\_min} > V_{BSUV-}$

Then:

$\Delta V_{BS} = Vcc - V_f - V_{GS\_min} - V_X$

Where
- Vcc is the supply voltage to the DGD2181M
- V_f is the voltage drop across the bootstrap diode (D_{BS})
- V_X is the voltage drop across the MOSFET

For an IGBT, V_X is V_{CE_ON} of the IGBT at the specific output current. For a MOSFET, it is calculated as the current seen across the MOSFET multiplied by its R_{DS_ON}.

In addition to the voltage drops across these components, other factors that cause V_{BS} to drop are leakages, charge required to turn on the power devices, and duration of the high-side on time. The total charge (QT) required by the gate driver then equals:

$Q_T = Q_G + Q_{LS} + [I_{LK\_N}] * T_{H\_ON}$

Where:

Q_G = gate charge of power device
Q_{LS} = level shift charge required per cycle
T_{H_ON} = high-side on time
I_{LK_N} = sum of all leakages that include:
- I_{GSS}/I_{GES}: Gate-source leakage of the power device
- I_{LK_DB}: Bootstrap diode leakage
- I_{LK_IC}: Offset supply leakage of HVIC
- I_{Q_BS}: Quiescent current for high-side supply
- I_{LK_CB}: Bootstrap capacitor leakage

Bootstrap capacitor leakage (I_{LK_CBS}) only applies to electrolytic types. Therefore, it is best not to use an electrolytic capacitor. Thus, bootstrap capacitor leakages will not be included in the calculations.

Q_{LS} is not listed in the datasheet; depending on the process technology, it could range anywhere from 3-20nC for 500V to 1200V process respectively. Assuming a value of 10nC for the 600V process should be sufficient with added margin.

From the basic equation, then the minimum bootstrap capacitor is calculated as:

$C_{B\_min} \geq Q_T / \Delta V_{BS}$

Example using IGBT, DGTD65T15H2TF

HVIC=DGD2181M

Vcc = 15V
Q_G = 61nC
I_{GSS} = 100nA
T_{H_ON} = 10µs
V_{CE} = 1.5V
Iout = 5A
I_{Q_BS} = 150µA
I_{LK_IC} = 50µA
Q_{LS} = 10nC
V_F = 1.0V
I_{LK_DB} = 100µA
V_{GSmin} = 10.0V

From equations:

ΔV_{BS} = 15V- 1.0V-10V-1.5V) = 2.5V

$Q_T = Q_G + Q_{LS} + (I_{LK\_N} * T_{H\_ON})$ where $I_{LK\_N} * T_{H\_ON}$ = 3.0nC

= 61nC + 10nC + 3.0nC

= 74nC

Thus C_{BS} min = 74nC/2.5V = 30nF

The bootstrap capacitor calculated in the above example is the minimal value required to supply the needed charge. It is recommended that a margin of 2-3 times the calculated value be used. Utilizing values lower than this could result in over charging of the bootstrap capacitor especially during –VS transients.

Typically for power supply applications C_{BS} = 1µF to 2.2µF are used, and for motor applications, C_{BS} = 1µF to 10µF are used. It is also recommended to use low ESR ceramic capacitors as close to the V_B and V_S pin as possible (see PCB layout suggestions section).

Gate Resistor Component Selection

The most crucial time in the gate drive is the turn on and turn off of the MOSFET, and performing this function quickly, but with minimal noise and ringing is key. Too fast a rise/fall time can cause unnecessary ringing and poor EMI, and too slow a rise/fall time will increase switching losses in the MOSFET.

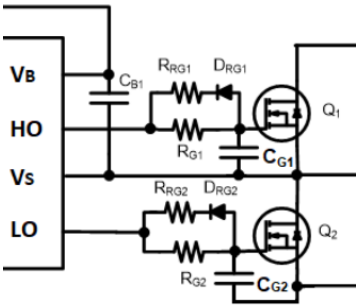

Figure 6. Gate Drive High-Side and Low-Side Components for DGD2181M

Considering the gate driver components for DGD2181M in Figure 6, with the careful selection of R_{G1} and R_{RG1}, it is possible to selectively control the rise time and fall time of the gate drive. For turn on, all current will go from the IC through R_{G1} and charge the MOSFET gate capacitor, hence increasing or decreasing R_{G1} will increase or decrease rise time in the application. With the addition of D_{RG1}, the fall time can be separately controlled as the turn off current flows from the MOSFET gate capacitor, through R_{RG1} and D_{RG1} to the driver in the IC to VS for high-side and COM for low-side. So, increasing or decreasing R_{RG1} will increase or decrease the fall time. Sometimes finer control is not needed and only R_{G1} and R_{G2} is used.

Increasing turn on and turn off has the effect of limiting ringing and noise due to parasitic inductances, hence with a noisy environment, it may be necessary to increase the gate resistors. Gate component selection is a compromise of faster rise time with more ringing, and a poorer EMI but better efficiency, and a slower rise time with better EMI, better noise performance but poorer efficiency. The exact value depends on the parameters of the application. Generally, for motors the switching speed is slower, and the application has more inherent noise, higher values are recommended, for example R_G = 20Ω - 100Ω.

To have equal switching times for high-side and low-side, it is recommended that the gate driver components for high-side and low-side are mirrored. For example $R_{RG1} = R_{RG2}$, $D_{RG1} = D_{RG2}$ and $R_{G1} = R_{G2}$.

The gate to source capacitors, CG1 and CG2, are used to minimize unexpected shoot through in the half-bridge. This shoot through can decrease efficiency or even damage the MOSFETs; this phenomenon is discussed further on page 6.

V_{CC} Decoupling Capacitor Selection

For optimal operation, Vcc decoupling is crucial for all gate driver ICs. With poor decoupling, larger Vcc transients will occur at the IC when switching, and for greater and longer Vcc drop the IC can go into UVLO.

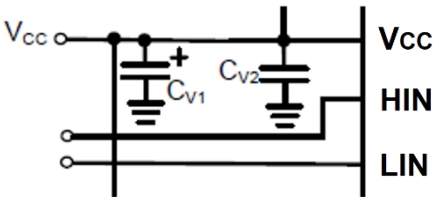

Figure 7. Suggested V_{CC} decoupling

As shown Figure 7, two decoupling capacitors are recommended C_{V1} and C_{V2}, C_{V1} can be a larger electrolytic, for example 47µF, 50V and is used to dampen low frequency drains on supply: C_{V1} does not need to be right next to the IC. But C_{V2} is used to decouple faster edge changes to Vcc, and should be a low ESR ceramic capacitor placed close to the Vcc pin. This component provides stability when Vcc is quickly pulled down with load from the IC; typical values are 0.1µF to 1µF.

For applications with multiple gate driver ICs (for example a full-bridge converter as shown in Figure 1), one larger electrolytic (C_{V1}) can be used and the two ceramic caps (C_{V2}, C_{V3}) should be used close to the Vcc pin (see PCB Layout section also).

High Voltage Decoupling Capacitors

Considering the performance of the whole half-bridge, it is important to have appropriate high voltage decoupling capacitors (see C_{HV1}, C_{HV2} and C_{HV3} in Figure 1). For best stability (best high frequency performance), C_{HV2} and C_{HV3} are small ceramic capacitors (say 1µF 450V) placed close to the drain of the MOSFETs at the half-bridge (less than 25mm); and C_{HV1} is the electrolytic bulk capacitor which is typically part of the on board power supply. If the small decoupling capacitors (C_{HV2} and C_{HV3}) are not used, then for optimal operation, the bulk capacitor (C_{HV1}) should be close to the drain of the MOSFETs (less than 25mm).

Input Resistors

The IC PWM inputs, HIN and LIN, are very high impedance inputs with pull-down resistors for both inputs to COM (see Figure 8). The pull-down resistors have an approximate value of 200kΩ.

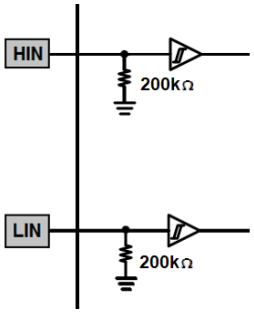

Figure 8. Input Logic for DGD2181M

Separate Logic Ground

In some system designs, to better separate the greater ringing on power ground from logic ground, a separate power ground and logic ground is used. DGD21814M has a V_{SS} pin, and internally the logic ground (V_{SS}) and power ground (COM) are separated. The V_{SS} pin is rated to operate from -5V to +5V (where 0V is COM, power ground).

Matching Gate Driver with MOSFET or IGBT

IC drive current and MOSFET/IGBT gate charge

Gate Driver ICs are defined by their output drive current, their ability to source current to the gate of the MOSFET/IGBT at turn on and to sink current from the gate of the MOSFET/IGBT at turn off. For the DGD2181M, the drive current is IO+=1.9A typical and IO-=2.3A typical.

For a given MOSFET/IGBT, with the known drive current of the DGD2181M, you can calculate how long it will take to turn on/off the MOSFET/IGBT with the equation:

t = Qg/I

Qg = total charge of the MOSFET/IGBT as provided by the datasheet
I = sink/source capability of the gate driver IC
t = calculated rise/fall time with the given charge and drive current

For example with Diodes' DGTD65T15H2TF, 650V IGBT, Qg = 61nC; and with the DGD2181M I_{O+}/I_{O-}, tr = 32ns and tf = 27ns. These are estimates as the total charge given in the datasheet may not be the same conditions in the application. Also, an addition of a gate resistor will increase the tr and tf.

Unexpected shoot-through with dV_{DS}/d_t

Unwanted MOSFET turn-on, caused by C_{GD} x dV_{DS}/d_t (see Figure 9) is often the cause of unexplained shoot through in the half-bridge circuit. Depending on the ratio of the C_{GS}/ C_{GD} , when the dV_{DS}/d_t across low-side MOSFET (Q2) occurs (i.e when high-side MOSFET turns on), there can be a voltage applied to the gate of the Q2 MOSFET, turning on Q2 and causing shoot through. In effect, a gate bouncing occurs causing a ringing on the VS line and the power ground.

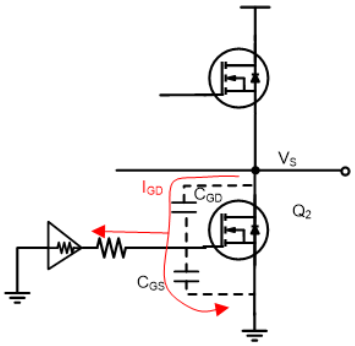

Figure 9. Unexpected shoot through with dV_{DS}/d_t

Considering Figure 9,

$I_{GD} = C_{GD}$ x dV_{DS}/d_t

I_{GD} will flow towards the resistive load (and small inductive due to parasitics) of the gate driver and the C_{GS} of the MOSFET. Hence this unwanted condition may be minimized by looking at the Ciss/Cres in the MOSFET datasheet (Ciss/Cres gives an indication of C_{GS}/C_{GD}); having a Ciss/Cres as large as possible will minimize this phenomenon. Also, an external capacitor can be added to the gate-source of the MOSFET (for example 1nF) which will increase C_{GS}/C_{GD}.

Minimum Pulse Requirement

The DGD2181M and DGD21814M have an RC filter on the input lines to be more resilient in noisy environments. With a rising edge at the input to the gate driver, and then after the propagation delay of the IC, delay from gate resistor, and rise time of the MOSFET, the half-bridge will turn on producing bus voltage at the output. This MOSFET turn on produces significant system noise. For optimal operation, it is suggested to provide a minimum pulse width at the input to the IC from the MCU to ensure the turn off occurs after this event. As a rule of thumb, this minimum pulse should be 2 x propagation delay for high-side/low-side gate drivers; hence for the DGD2181M and DGD21814M, the minimum pulse recommended at the logic inputs is 360ns.

During typical operation, the DGD2181M and DGD21814M will respond to an input pulse greater than about 50ns (approximate value from the RC input filter response). Hence for an input pulse greater than 50ns approximately, the IC will follow the pulse as expected; and for an input pulse less than 50ns, there will be no response from the IC.

PCB layout suggestions

Layout plays an important role in minimizing unwanted noise coupling, unpredicted glitches, and abnormal operation which can arise from poor layout of the associated components. Figure 10 shows a schematic with parasitic inductances in the high-current path (L_{P1}, L_{P2}, L_{P3}, L_{P4}), which would be caused by inductance in the metal of the trace. Considering Figure 10, the length of the tracks in red should be minimized, and the bootstrap capacitor (C_B) and the decoupling capacitor (C_D) should be placed as close to the IC as possible as well as use low ESR ceramic capacitors. And finally, the gate resistors (R_{GH} and R_{GL}) and the sense resistor (R_S) should be surface mount devices. These suggestions will reduce the parasitics due to the PCB traces.

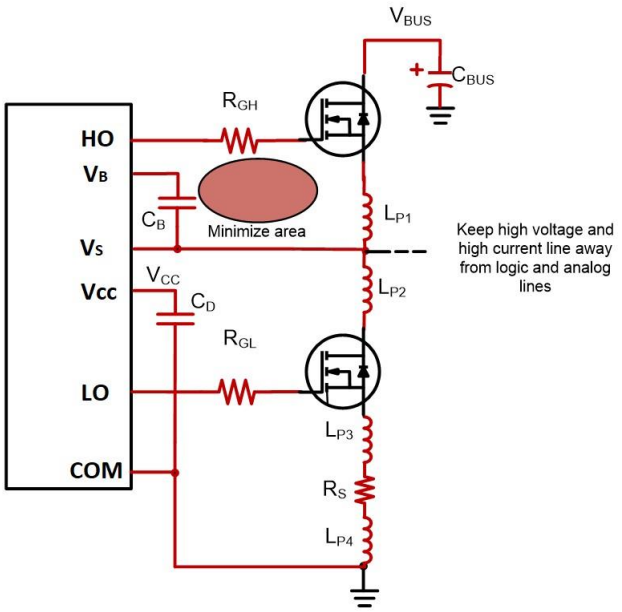

Figure 10. Layout suggestions for DGD2181M in a half-bridge, lines in red should be as short as possible.

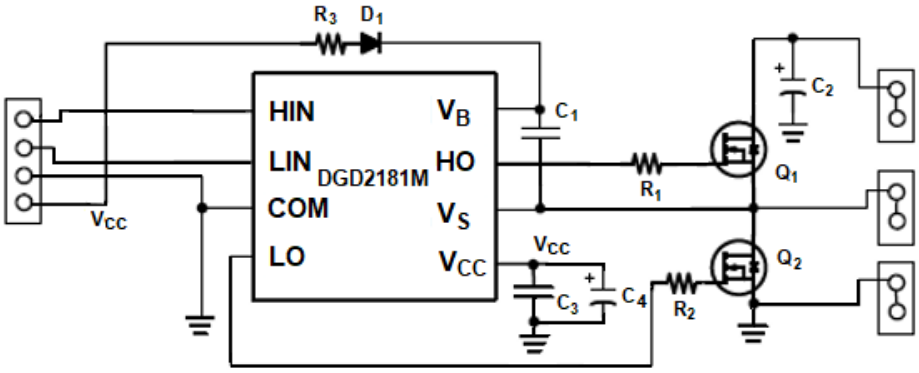

Figure 11. Schematic for layout example in Figure 12

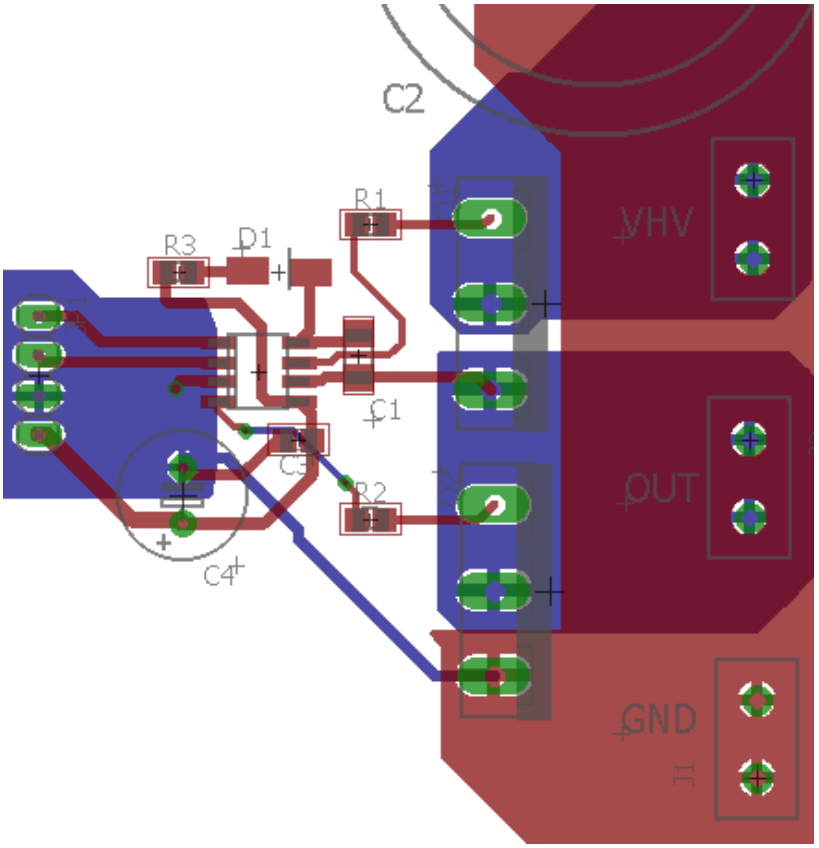

Figure 12. Layout of the schematic shown in Figure 11, DGD2181M in SO-8, MOSFETs in TO-220, and only bottom of bulk electrolytic capacitor (C2) shown.

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