Design and Application Notes for AP3765 System Solution

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1. Introduction

The AP3765 uses Pulse Frequency Modulation (PFM) method to realize Discontinuous Conduction Mode (DCM) operation for flyback power supplies. The principle of PFM is different from that of Pulse Width Modulation (PWM), so the design of transformer is also different.

The AP3765 can provide accurate constant voltage, constant current (CV/CC) regulation by using Primary Side Regulation (PSR).

The AP3765 can also achieve ultra-low standby power due to its PFM operation and an innovative ultra-low startup current technique. Less than 30mW standby power can be obtained to meet five-star charger criteria with AP3765 system solution.

A typical AP3765 application circuit is shown in Figure 1.

2. Operation Description

2.1 Constant Primary Peak Current

The primary current ip(t) is sensed by a current sense resistor R_S as shown in Figure 1. The current rises up linearly at a rate of:

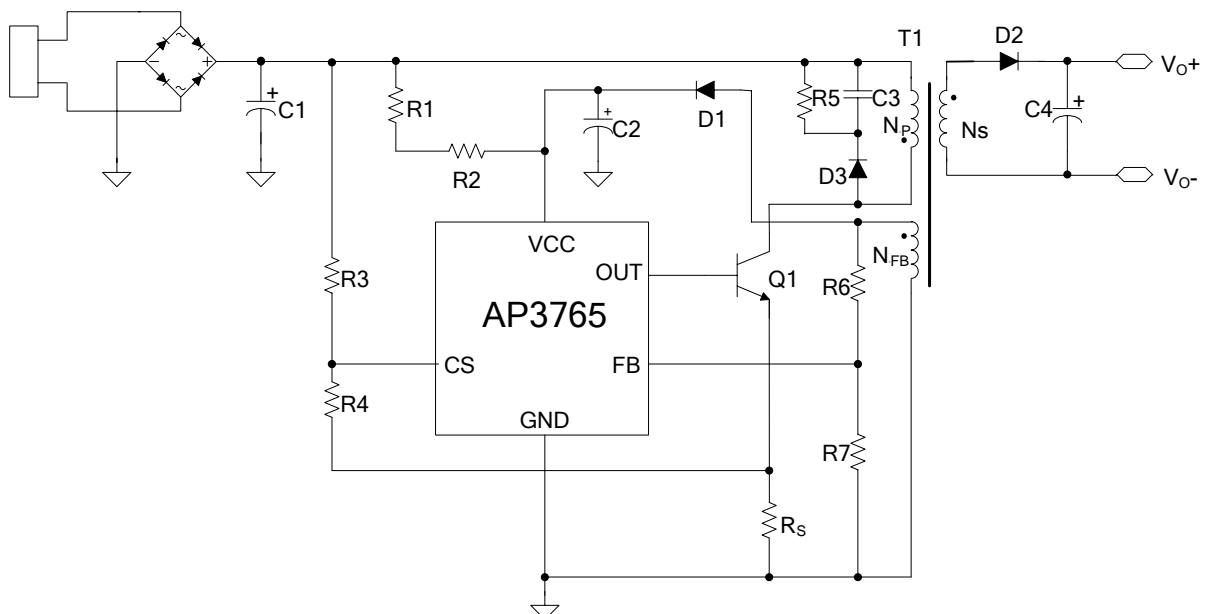$$\frac{dip(t)}{dt} = \frac{vg(t)}{L_M} \tag{1}$$
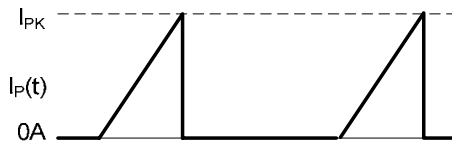

Figure 1. Typical Schematic of AP3765 Solution

Figure 2. Primary Current Waveforms

As illustrated in Figure 2, when the current $I_P(t)$ rises up to I_{PK}, the switch Q1 turns off. The constant peak current is given by:

$$Ipk = \frac{V_{CS}}{R_S} \tag{2}$$

The energy stored in the magnetizing inductance L_M each cycle is therefore:

$$Eg = \frac{1}{2} \cdot L_M \cdot Ipk^2 \tag{3}$$

So, the power transferring from input to output is given by:

$$P = \frac{1}{2} \cdot L_M \cdot Ipk^2 \cdot f_{SW} \tag{4}$$

Where the f_{SW} is the switching frequency. When the peak current I_{PK} is constant, the output power depends on the switching frequency f_{SW}.

2.2 Constant Voltage Operation

The AP3765 captures the auxiliary winding feedback voltage at FB pin and operates in constant voltage (CV) mode to regulate the output voltage. Assuming the secondary winding is master, the auxiliary winding is slave during the D2 on-time and the auxiliary voltage is given by:

$$V_{AUX} = \frac{N_{AUX}(V_o + V_d)}{N_S} \tag{5}$$

where the Vd is the diode forward drop voltage. N_{AUX} is the turns of auxiliary winding, and N_S is the turns of secondary winding.
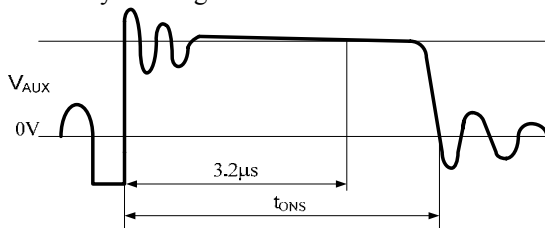

Figure 3. Auxiliary Voltage Waveform

The output voltage is different from the secondary voltage in a diode forward drop voltage that depends on the current. If the secondary voltage is always detected at a fixed secondary current, the difference between the output voltage and the secondary voltage will be a fixed Vd. For AP3765, the voltage detection point is at 3.2μs of the D2 on-time, which means the the secondary voltage is detected at a fixed secondary current. The CV loop control function of AP3765 then generates a D2 off time to regulate the output voltage.
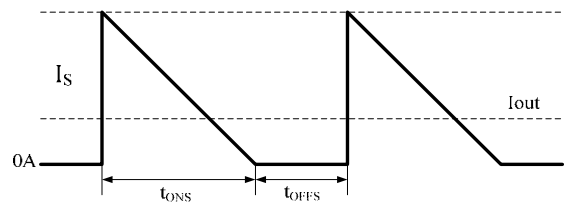
2.3 Constant Current Operation

Figure 4. Secondary Current Waveform

In CC operation, the CC loop control function of AP3765 will keep a fixed proportion between D2 on-time t_{ONS} and D2 off-time t_{OFFS} by discharging or charging the built-in capacitance connected. The fixed proportion is

$$\frac{t_{ONS}}{t_{OFFS}} = \frac{4}{3} \tag{6}$$

The relationship between the output constant current and secondary peak current Ipks is given by:

$$Iout = \frac{1}{2} \times Ipks \times \frac{t_{ONS}}{t_{ONS} + t_{OFFS}} \tag{7}$$

At the instant of D2 turn-on, the primary current transfers to the secondary at an amplitude of:

$$Ipks = \frac{Np}{Ns} \times Ipk \tag{8}$$

Thus the output constant-current is given by:

$$Iout = \frac{1}{2} \times \frac{Np}{Ns} \times Ipk \times \frac{t_{ONS}}{t_{ONS} + t_{OFFS}} = \frac{2}{7} \times \frac{Np}{Ns} \times Ipk \tag{9}$$

2.4 Leading Edge Blanking

When the power switch is turned on, a turn-on spike will occur on the sense-resistor. To avoid false termination of the switching pulse, a 750ns leading

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edge blanking is built in. During this blanking period, the current sense comparator is disabled and the gate driver can not be switched off.

2.5 CCM Protection

The AP3765 is designed to operate in Discontinuous Conduction Mode (DCM) in both CV and CC modes. To avoid operating in Continuous Conduction Mode (CCM), the AP3765 detects the falling edge of the FB input voltage on each cycle. If a 0.075V falling edge of FB is not detected at the end of t_{ONS}, the AP3765 will stop switching.

2.6 OVP & OCkP

The AP3765 includes over-voltage protection (OVP) and open circuit protection (OCkP) circuitries as shown in Figure 5. If the voltage at FB pin exceeds 8V, 100% above the normal detection voltage, the AP3765 will enter OVP mode. However, if the AP3765 doesn't monitor 0.075V rising edge of FB input at the end of t_{ONP} or high voltage (>0.075V) after t_{SAMPLE}, it will enter OCkP mode. When AP3765 enters OVP or OCkP mode, it will sends out a fault detection pulse every 18ms until the fault has been removed.
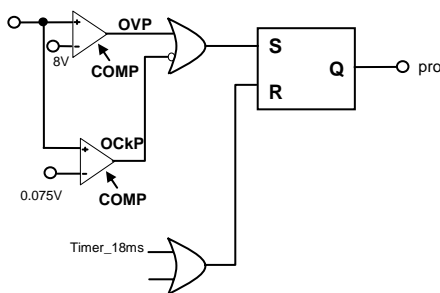

Figure 5. OVP & OCkP Function Block

3. Design Guidelines
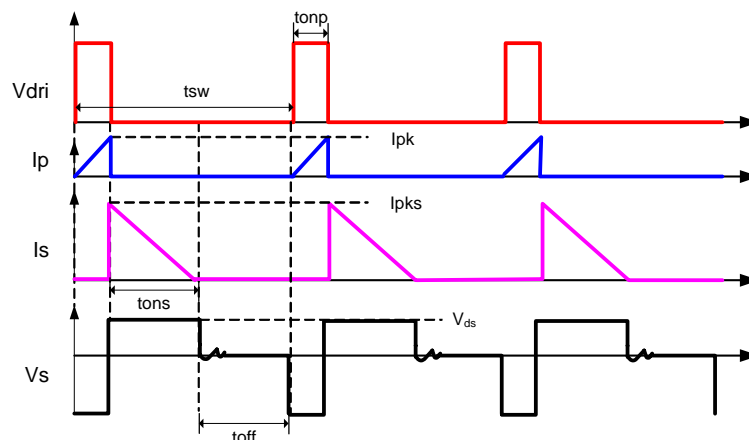### 3.1 Low Standby Power Design

The tradeoff between the low standby power and the output overshoot at no load should be considered during the selection of the dummy resistor R8. In order to achieve less than 30mW standby power while having an acceptable output voltage rise at no load, 5.1K to 10k is recommended for R8. The power consumed in the startup resistors (R1+R2) also becomes considerable in no load or light load conditions. So 10MΩ to 13MΩ resistance is recommended for the sum of R1 and R2 considering the target of less than 30mW standby power and less than 3s turn-on delay time. And the bias capacitor C2 is recommended as 1μF to 1.5μF accordingly.

3.2. Transformer Design

Figure 1 describes a flyback converter controlled by AP3765 with a 3-winding transformer---Primary winding (N_P), Secondary winding (N_S) and Auxiliary winding (N_A) for bias power and output voltage detecting. The AP3765 senses the auxiliary winding feedback voltage at FB pin and obtains power supply at VCC pin. In Figure 6, a series of relative ideal operation waveforms are given to illustrate some parameters used in following design steps. And the nomenclature of the parameters in Figure 6 is as the following:

V_{dri}---a simplified driving signal of primary transistor
I_P---the primary side current
I_S ---the secondary side current
V_S---the secondary side voltage
t_{sw}---the switching period of frequency
f_{sw}---the switching frequency
t_{onp}---the time of primary side "ON"
t_{ons}---the time of secondary side "ON"
t_{off}---the discontinuous time
I_{pk}---peak current of primary side
I_{pks}---peak current of secondary side
V_{ds}---the sum of Vo and the forward voltage drop of rectification diode

Figure 6. Operation Waveforms

4. Design Steps:

Step 1. Select a Reasonable I_{pk} for the Flyback Converter with AP3765

1-1. Calculate the Maximum Turn Ratio of XFMR

The maximum turn ratio of transformer should be designed first, which is to ensure that the system should work in DCM in all working conditions, especially at the minimum input voltage and full load.

If the system can meet equation (10) at minimum input voltage and full load, it can work in DCM in all working conditions.

$$t_{SW} \geq t_{ONP} + t_{ONS} \tag{10}$$

For the primary side current,

$$t_{ONP} = I_{pk} \frac{L_p}{V_{indc}} \tag{11}$$

Where L_p is the inductance of primary winding. V_{indc} is the rectified DC voltage of input.

When V_{indc} is the minimum value, the maximum t_{ONP} can be obtained. So,

$$t_{ONP\_MAX} = I_{pk} \frac{L_p}{V_{indc\_min}} \tag{12}$$

For the secondary side current,

$$t_{ONS} = I_{pks} \frac{L_S}{V_S} \tag{13}$$

In (13), L_s is the inductance of secondary winding.

$V_S = V_O + V_d$, V_d is the forward voltage drop of the secondary diode.

For (13), in CV regulation, the V_s is a constant voltage, so t_{ONS} is a constant value with different input voltage.

In the flyback converter, when the primary transistor turns ON, the energy is stored in the magnetizing inductance L_p. So the power stored in L_p is given by,

$$P_{in} = \frac{1}{2} L_p I_{pk}^2 f_{SW} \tag{14}$$

Then,

$$t_{SW} = \frac{L_p I_{pk}^2}{2P_{in}} \tag{15}$$

t_{SW}, t_{ONP} and t_{ONS} in (10) are replaced with (15), (12) and (13),

$$\frac{L_p I_{pk}^2}{2P_{in}} \geq I_{pks} \frac{L_s}{V_s} + I_{pk} \frac{L_p}{V_{indc\_min}} \tag{16}$$

Because the peak current and inductance of primary side and secondary side have the following relationship,

$$I_{pks} = n_{ps} \times I_{pk} \tag{17}$$

$$L_s = \frac{L_p}{n_{ps}^2} \tag{18}$$

Where n_{PS} is the turn ratio of primary winding to the secondary winding.

With (16), (17) and (18), then,

$$\frac{I_{pk}}{2P_{in}} \geq \frac{1}{V_S n_{ps}} + \frac{1}{V_{in}} \tag{19}$$

Because,

$$P_{in} = \frac{V_O I_O}{\eta} \tag{20}$$

Where η is the system efficiency.

At maximum load, the system will work in the boundary between CV and CC stages. I_O can be given by,

$$I_O = \frac{1}{2} \times \frac{t_{ONS}}{t_{SW}} I_{pks} \tag{21}$$

Then, I_{pks} can be defined,

$$I_{pks} = kI_O \tag{22}$$

In the design of AP3765,

$k = \dfrac{2t_{SW}}{t_{ONS}} = 3.5$ (In CC mode, the proportion of t_{ONS} and t_{OFFS} is 4:3) (23)

So it can be obtained,

$$n_{ps} \leq V_{indc\_min}(\frac{k \times \eta}{2V_O} - \frac{1}{V_S}) \qquad (24)$$

Therefore, the maximum turn ratio of primary and secondary side N can be obtained.

$$N \leq V_{indc\_min}(\frac{k \times \eta}{2V_O} - \frac{1}{V_O + V_d}) \qquad (25)$$

Because above calculations are all based on ideal conditions without considering precision of system, k is given an experiential value 3.85 to replace the real value 3.5.

1-2. Calculate the Peak Current of Primary Side and Current Sensed Resistor

I_{pk} can be calculated by the output current.

$$I_{pk} = \frac{I_{pks}}{n_{ps}} = \frac{k \times I_O}{n_{ps}} \qquad (26)$$

Here, k=3.85
n_{PS} is the calculated value of n_{MAX}.

In AP3765, 0.5V is an internal reference voltage. If the sensed voltage V_{CS} reaches 0.5V, the power transistor will be shut down and t_{ONP} will be ended.

$$R_{CS} = \frac{0.5V}{I_{pk}} \qquad (27)$$

So R_{CS} can be obtained from equation (27) and selected with a real value from the standard resistor series. After R_{CS} is selected, I_{pk} should be modified based on the selected R_{CS}.

From now on, Ipk and R_{CS} have been designed.

Step 2. Design Transformer

2-1. Calculation of the Primary Side Inductance ---L_P

The primary side inductance L_P is relative with the stored energy. L_P should be big enough to store enough energy, so that P_{o_Max} can be obtained from this system.

From formula (20), the output power can be given by,

$$P_O = \frac{1}{2}L_p I_{pk}^2 f_{SW}\eta \quad (\eta\text{: system efficiency}) \qquad (28)$$

Then, L_P can be got by,

$$L_P = \frac{2P_O}{I_{PK}^2 f_{SW}\eta} \qquad (29)$$

Here, to achieve good overall system performance, the optimum switching frequency f_{SW} is recommended to be 50kHz to 60kHz under full Load.

2-2. Re-calculate the Turn Ratio of Primary and Secondary Sides---n_{PS}

From formula (26), the turn ratio of primary and secondary side n can be re-calculated.

$$n_{ps} = \frac{k \cdot I_O}{I_{pk}}\,(k = 3.85) \qquad (30)$$

2-3. Calculate the Turns of Primary, Secondary and Auxiliary Sides

First, the reasonable core-type and ΔB should be selected. Then, the turns of 3-winding transformer can be obtained respectively.

The turns of primary winding,

$$N_p = \frac{L_P I_{PK}10^4}{Ae \times \Delta B}\,(L_p\text{:mH},I_{pk}\text{:mA},Ae\text{:mm}^2, \Delta B\text{:GS})$$
$$(31)$$

The turns of secondary winding,

$$N_S = \frac{N_P}{n_{PS}} \qquad (32)$$

The turns of auxiliary winding,

$$N_A = \frac{N_S V_A}{V_S} \qquad (33)$$

Here, V_A can be set a typical value of 20V.
V_s is equal to V_o+V_d.
Ae can be got automatically after core-type is selected.

Step 3. Select Diode and Primary Transistor

3-1. Select Diodes of Secondary and Auxiliary Sides
Maximum reverse voltage of secondary side

$$V_{dr} = V_O + \frac{V_{indc\_max}N_S}{N_P} \qquad (34)$$

Maximum reverse voltage of auxiliary side,

$$V_{dar} = V_A + \frac{V_{indc\_max} N_A}{N_P} \quad (35)$$

In (34) and (35), the maximum DC input voltage should be used.

3-2. Select the Primary Side Transistor

$$V_{dc\_max} = V_{dc\_spike} + V_{indc\_max} + \frac{V_S N_P}{N_S} \quad (36)$$

Be careful that the value of V_{dc_spike} will be varied with different snubber circuit.

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5. Design Example

Specification:
Input voltage: $85V_{AC}$-$265V_{AC}$
Output voltage: V_O=5V
Output current: I_O=0.7A
System Efficiency: 75%
Switching frequency: f_{SW}=60kHz
Forward voltage of secondary diode: V_d=0.4V
Forward voltage of auxiliary diode: Vda=1V
Feedback voltage of auxiliary winding: Va=20V
Core_type: EE16 (Ae=19.2mm^2)
ΔB : ΔB=2450GS
V_{dc_spike}=100V (with snubber circuit)
Output cable: 28AWG, 1.5m long, 0.214Ω/m
Secondary diode turns on duty cycle: D_{ons} = 4/7
Feedback resistor: R6=36.5k, R7=9.1k

Design Steps:

Step 1. A Reasonable Ipk of Flyback with AP3765 Should be Designed

1-1. Calculate the Max. Turn Ratio of XFMR

$$N_{MAX} = V_{indc\_min}\left(\frac{k \times \eta}{2V_O} - \frac{1}{V_O + V_d}\right)(k \approx 3.85) \quad (37)$$

$$V_{indc\_min} = V_{inac\_min} \times \sqrt{2} - 40 \quad (\text{ when } I_O=0.7A, \text{ Set: } V_{indc}$$
drops about 40V) $\quad (38)$

$$N_{MAX} = 8.3 \quad (39)$$

1-2. Calculate the Peak Current of Primary Side and Current Sensed Resistor

$$I_{pk} = \frac{I_{pks}}{N} = \frac{k \times I_O}{N} \quad (40)$$

$$I_{pk\_max} = 325mA \quad (41)$$

Sensed current resistor,

$$R_{CS} = \frac{0.5V}{I_{pk}} \quad (42)$$

$$R_{CS} \approx 1.538\Omega \quad (\text{Set}: R_{CS} = 1.54\Omega) \quad (43)$$

Re-calculate peak current of primary side,

$$I_{pk\_max} = 325mA \quad (44)$$

Step 2. Design Transformer

2-1. Calculation of the Inductance of Primary Side---Lp

$$L_P = \frac{2P_O}{I_{PK}^2 f_{SW} \eta} \quad (45)$$

$$L_p = 1.47mH \quad (46)$$

2-2. Re-calculate the Turn Ratio of Primary and Secondary Side---N

$$N = \frac{k \cdot I_O}{I_{pk}}(k \approx 3.85) \quad (47)$$

$$N = 8.3 \quad (48)$$

2-3. Calculate the Turns of Primary, Secondary and Auxiliary Sides

The turns of primary winding,

$$N_p = \frac{L_P I_{PK} 10^4}{Ae \times \Delta B} \quad (49)$$

$$N_P = 102 \text{ N} \quad (50)$$

The turns of secondary winding,

$$N_S = \frac{N_P}{N} \quad (51)$$

$$N_S = 12T \quad (52)$$

The turns of auxiliary winding,

$$N_A = \frac{N_S V_A}{V_S} \qquad (53)$$

$$N_A = 44T \qquad (54)$$

Step 3. Select Diode and Primary Transistor

3-1. Select Diodes of Secondary and Auxiliary Sides

Maximum reverse voltage of secondary side

$$V_{dr} = V_O + \frac{V_{indc\_max} N_S}{N_P} \qquad (55)$$

$$V_{dr} = 49.1V \qquad (56)$$

Maximum reverse voltage of auxiliary side

$$V_{dar} = V_A + \frac{V_{indc\_max} N_A}{N_P} \qquad (57)$$

$$V_{dar} = 181.8V \qquad (58)$$

3-2. Select Primary Side Transistor

$$V_{dc\_max} = V_{dc\_spike} + V_{indc\_max} + \frac{V_S N_P}{N_S} \qquad (59)$$

$$V_{dc\_max} = 520.9V \qquad (60)$$

Step 4. Select Reasonable Feedback Resistor R6 and R7

$$V_{FB} = 4V = Va \times \frac{R7}{R6 + R7} \ (\text{Set:R7=9.1k}\Omega,\text{R6=36.5k}\Omega)$$

$$(61)$$

Design Results Summary:

1. Calculate the Maximum Peak Current of Primary Side and R_{CS}			
$I_{PK}=$	325	mA	Peak current of primary side
$R_{CS}=$	1.54	Ω	Current sensed resistor
2. Design Transformer			
$L_P=$	1.47	mH ($\pm$8%)	Inductance of primary side
N=	8.3	Turn ratio of primary and secondary	
$N_P=$	102	T	Turns of primary side
$N_S=$	12	T	Turns of secondary side
$N_A=$	44	T	Turns of auxiliary side
3. Select Diode and Primary Transistor			
Vdr=	49.1	V	Maximum reverse voltage of secondary diode
Vdar=	181.8	V	Maximum reverse voltage of auxiliary diode
Vdc_max=	520.9	V	Voltage stress of primary transistor
4. Select Feedback Resistor			
R6=	36.5	kΩ	Feedback resistor
R7=	9.1	kΩ	Feedback resistor