PIxEQX6741SxZDE

PIxEQX6741SxZDE Evaluation Board Rev.C User Guide

Mar. 23, 2009

Contents

Introduction

The PIxEQX6741SxZDE Evaluation Board has been designed to allow convenient testing of the operation and features of Pericom's PI3EQX6741STZDE, PI2EQX6741SLZDE, and PI3EQX6741STBZDE SATA ReDriver. This board is designed to work with readily available SATA and eSATA cables for easy connection to SATA3.0 HDD, SSD, OMD storage components and PC system hosts.

This board allows the PIxEQX6741SxZDE device to be powered in either +1.05V, or 3.3V with an on-board regulator provided or directly from external power.

This User Guide describes the setup, configuration and operation of PIxEQX6741xZDE Eval Board Rev.C. Figure1 provides a top view of PIxEQX6741SxZDE Eval Board Rev.C, and Figure2 is bottom view of the board.

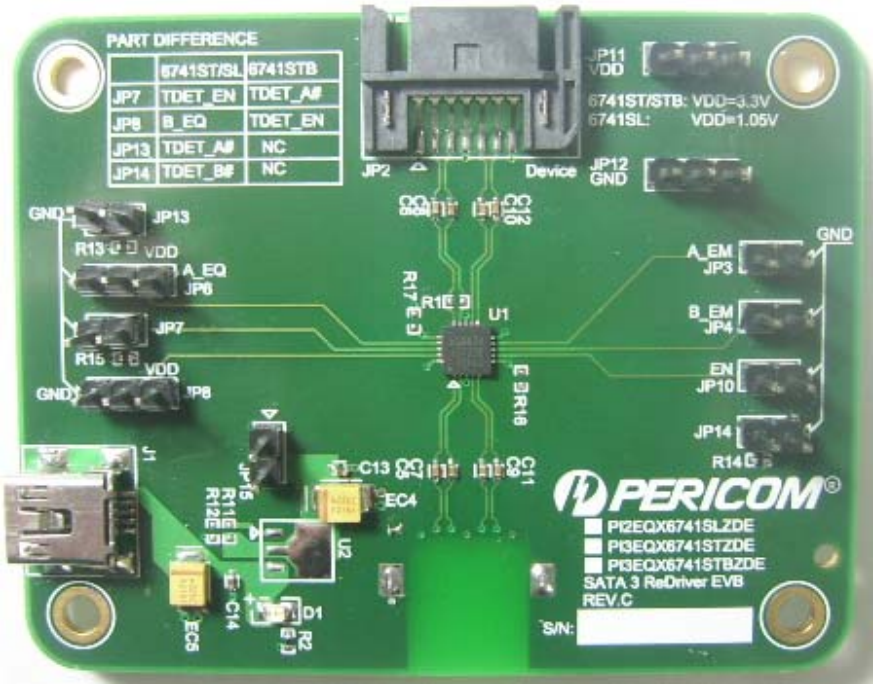


Figure1. Top view of PIxEQX6741SxZDE Eval board Rev.C

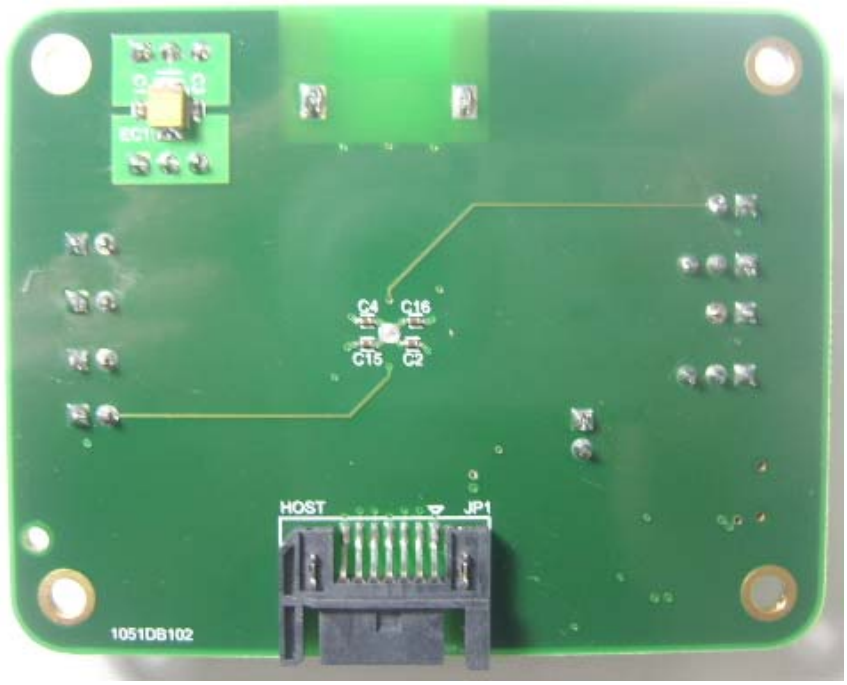


Figure2. Bottom view of PIxEQX6741SxZDE Eval board Rev.C

Board Operation

PIxEQX6741SxZDE is a 1-port (2-channel), bi-directional, signal SATA3.0 re-driver with termination detect feature to provide indication when the load is connected to HOST or Device. Figure3 shows the logical block diagram of PIxEQX6741SxZDE. Both channels of the PIxEQX6741SxZDE are fully independent in operation and configuration, except for the chip Enable function. Either SATA data connector, **J1** or **J2** can be connector to either the host controllers or target disk drive interchangeably. Channel configuration of output pre-emphasis, output swing and input equalization must be set appropriately to match the attached cable/trace length and type.

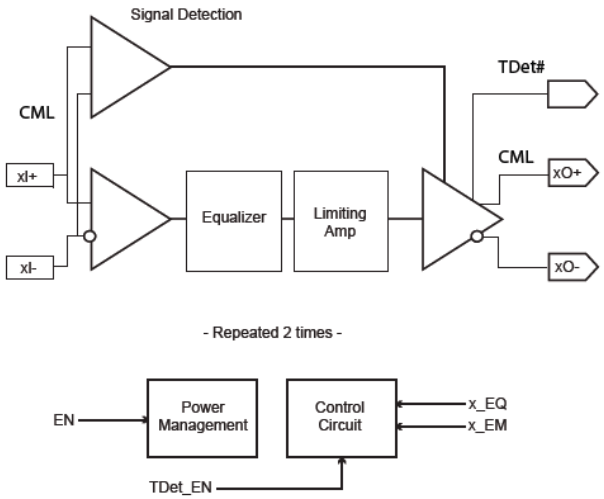


Figure3. Logical Block Diagram of PIxEQX6741SxZDE

Power Options

The PIxEQX6741SxZDE Evaluation Board provides the options for supplying +1.05V or +3.3V power to the ReDriver. Figure 4 circles the important connections.

1) Using the +5V power supplied by miniUSB connector (**J1**). The on-board LDO down-steps the voltage to +3.3V. When using this source, note that jumper **JP15** must be shorted (closed).

2) Using +1.05V or +3.3V power input directly by **JP11** power pin header and **JP12** ground pin header. When using this method, **JP15** must be open.

3) For PIxEQX6741SxZDE power supply, the evaluation board is shipped from the factory with +3.3V default from miniUSB port. Jumper JP15 must be shorted for normal operation.

Note:
1, PI3EQX6741STZDE and PI3EQX6741STB POWER SUPPLY is +3.3V. R16 and R17 should be OPEN.
2, PI2EQX6741SLZDE POWER SUPPLY is +1.05V, R16 and R17 MUST be populated with 0ohm resistor.

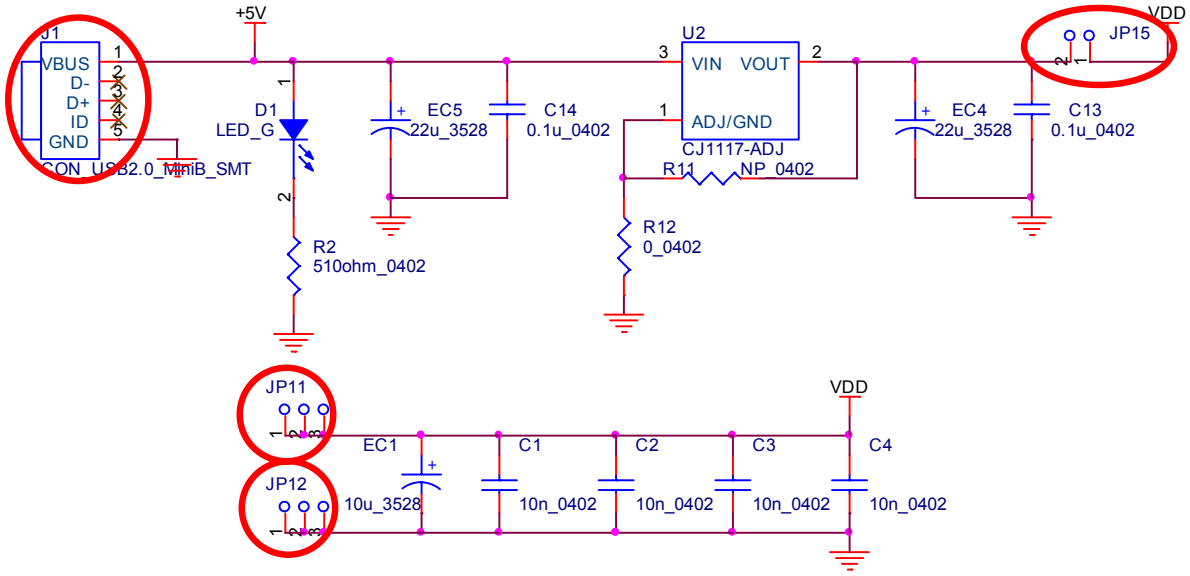


Figure4. Power supply of PIxEQX6741SxZDE

Device Configuration

The PIxEQX6741SxZDE SATA ReDriver supports emphasis and swing adjustment for optimum operation and signal margins. For the input equalizer, equalization is controlled via tri-level digital input pin.

PI3EQX6741STZDE and PI2EQX6741SLZDE have the same configuration at control pins, but PI3EQX6741STB has another configuration at control pins. Table1 shows the difference of control pins for them.

Table1. Control pins difference for PI3EQX6741ST/SL and PI3EQX6741STB

P/N	PIN3&13	PIN18	PIN19
PI3EQX6741STZDE PI2EQX6741SLZDE	TDet_A# TDet_B#	TDet_EN	B_EQ
PI3EQX6741STBZDE	NC	TDet_A#	TDet_EN

The location of configuration jumpers is shown in Figure 5. Configuration begins with EN pin as **JP10**, which must be open for normal operation. The EN pin of the PIxEQX6741SxZDE has an internal 200K pull-up resistor to define a high level default for normal operation.

When EN pin are shorted to GND, device operation is disabled. This is useful for checking PIxEQX6741SxZDE disabled-state power consumption.

1) Output Emphasis Configuration

Output signal emphasis can be controlled on PIN8&9. PIN8&9 has an internal 200k pull-up resistor to define a high level default once they're open.
The PIxEQX6741SxZDE Eval Board implements 2 jumpers (**JP3** and **JP4**) for adjusting output emphasis on each channel as detailed in Table 1 below.

Table2. Output Emphasis Settings on PIxEQX6741SxZDE Eval Board (x means Open, 0 means short)

JP3: A_EM JP4: B_EM	Output emphasis		Recommended Use
	PI3EQX6741STZDE PI2EQX6741SLZDE	PI3EQX6741STBZDE	
0 0	500mV at 3Gb/s 600mV at 6Gb/s	600mV	Default Factory Setting
x x	500mV+3.0dB pre-emphasis at 3.0Gb/s 600mV+1.5dB pre-emphasis at 6.0Gb/s	600mV+1.5dB pre-emphasis	For long trace or cable

2) Equalizer Configuration

A_EQ sets channel-A input equalization, while B_EQ sets channel-B equalization, as shown in Table 3. The equalization control inputs to the PI3EQX6741STZDE and PI2EQX6741SLZDE, A_EQ and B_EQ, have an internal 100K pull-up and 100K pull-down resistors for tri-level control by **JP6** and **JP8**. But PI3EQX6741STBZDE has ONLY A_EQ setting, so it is necessary to check which part is used and then refer to Table3 below for equalization selection.

Table3. EQ Settings on PIxEQX6741SxZDE Eval Board

<table>
<tr><th>P/N</th><th>JP6:
A_EQ</th><th>JP8:
B_EQ</th><th>Equalization Level</th><th>System Use</th></tr>
<tr><td>PI3EQX6741STZDE
PI2EQX6741SLZDE</td><td>Y</td><td>Y</td><td>
<table>
<tr><td rowspan="2">Resistor</td><td colspan="3">Input Equalization for Channel A&B</td></tr>
<tr><td>1.5Gb/s</td><td>3Gb/s</td><td>6Gb/s</td></tr>
<tr><td>Ch A: JP6=GND
Ch B: JP8=GND</td><td>1.0dB</td><td>2.5dB</td><td>3.0dB</td></tr>
<tr><td>Ch A: JP6=NP
Ch B: JP8=NP</td><td>2.5dB</td><td>5.0dB</td><td>6.0dB</td></tr>
<tr><td>Ch A: JP6=VDD
Ch B: JP8=VDD</td><td>4.0dB</td><td>7.5dB</td><td>9.0dB</td></tr>
</table>
</td><td rowspan="2">To GND:
Short trace<12inch
Default setting

NP:
Longer trace<24inch

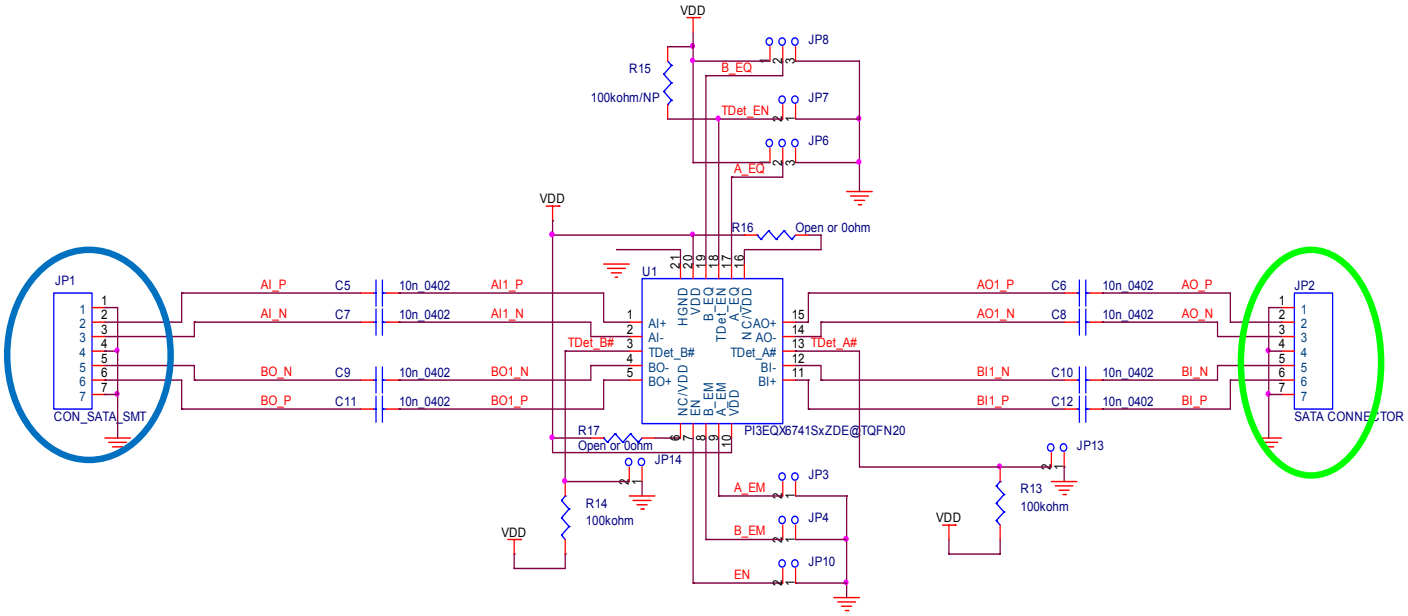
To VDD:
Longer trace<36inch</td></tr>
<tr><td>PI3EQX6741STBZDE</td><td>Y</td><td>N</td><td>
<table>
<tr><td rowspan="2">Resistor</td><td colspan="3">Input Equalization for Channel A</td></tr>
<tr><td>1.5Gb/s</td><td>3Gb/s</td><td>6Gb/s</td></tr>
<tr><td>Ch A: JP6=GND</td><td>1.0dB</td><td>2.5dB</td><td>3.0dB</td></tr>
<tr><td>Ch A: JP6=NP</td><td>2.5dB</td><td>5.0dB</td><td>6.0dB</td></tr>
<tr><td>Ch A: JP6=VDD</td><td>4.0dB</td><td>7.5dB</td><td>9.0dB</td></tr>
</table>
</td></tr>
</table>

3) Termination Detect Configuration

PIxEQX6741SxZDE has termination detect feature for power saving without HOST or Device. PI3EQX6741STZDE and PI2EQX6741SLZDE have TDet_A# and TDet_B# output indication via Enable pin-TDet_EN with internal 200k pull-up resistor. But PI3EQX6741STB has only TDet_A# output for Channel A. Table4 is termination detect configuration.

Table4. Termination Detect Settings for PIxEQX6741ST/SLZDE on Eval Board

P/N	TDet_EN	Termination Detect Output	Effective		System Use
PI3EQX6741STZDE PI2EQX6741SLZDE	JP7 at PIN18	TDet_A# at PIN13 TDet_B# at PIN3	**JP7=Open**	**Enable**	R15 should be open **RED** is default.
			JP7=Short	Disable	
PI3EQX6741STBZDE	JP8 at PIN19	TDet_A# at PIN18	**JP8=Open**	**Enable**	R15 should be 100kohm resistor, **RED** is default
			JP8=Short	Disable	



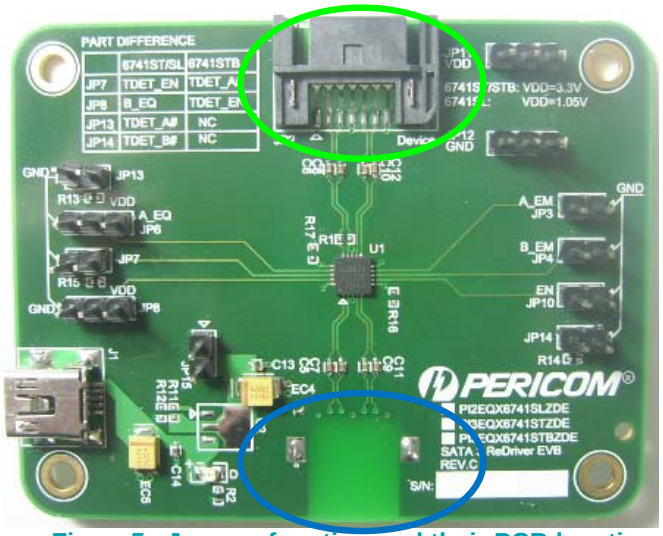


Figure5. Jumper function and their PCB location

System Connection

The diagrams below show some example system test setups with the PIxEQX6741SxZDE Eval Board.

Figure 6 shows the connection using a NB PC and eSATA Express Card. Note that many notebooks PCs already offer an eSATA port which can be used as the test signal source without the add-in card.

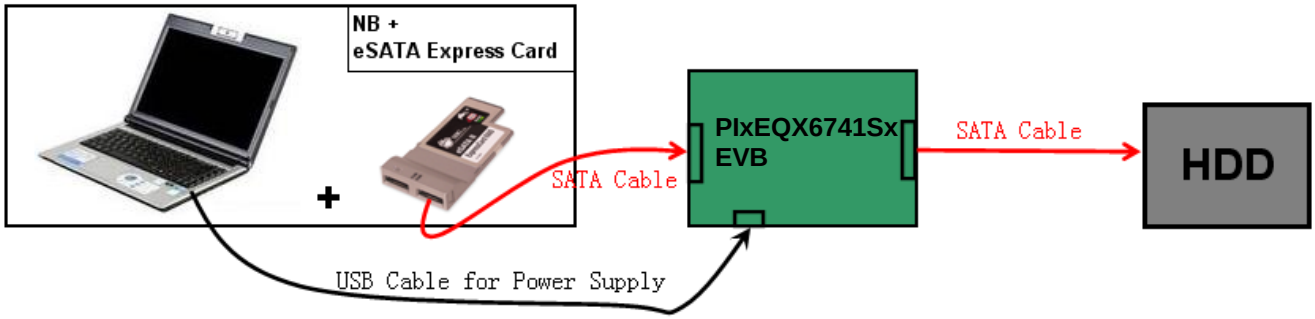


Figure 6. eHDD connection Test Setup using NB+eSATA Express Card with PIxEQX6741SxZDE Eval Board

Figure 7 shows the connection using Intel MB

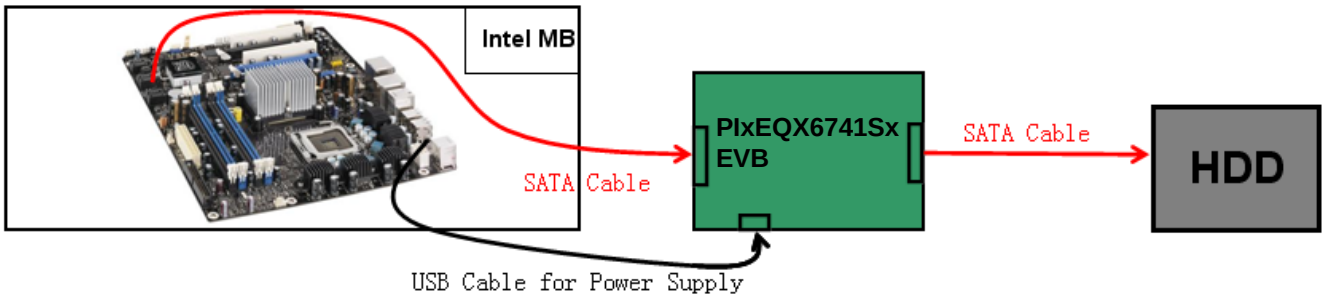


Figure 7. internal HDD connection Test Setup using Intel MB with PIxEQX6741SxZDE Eval Board

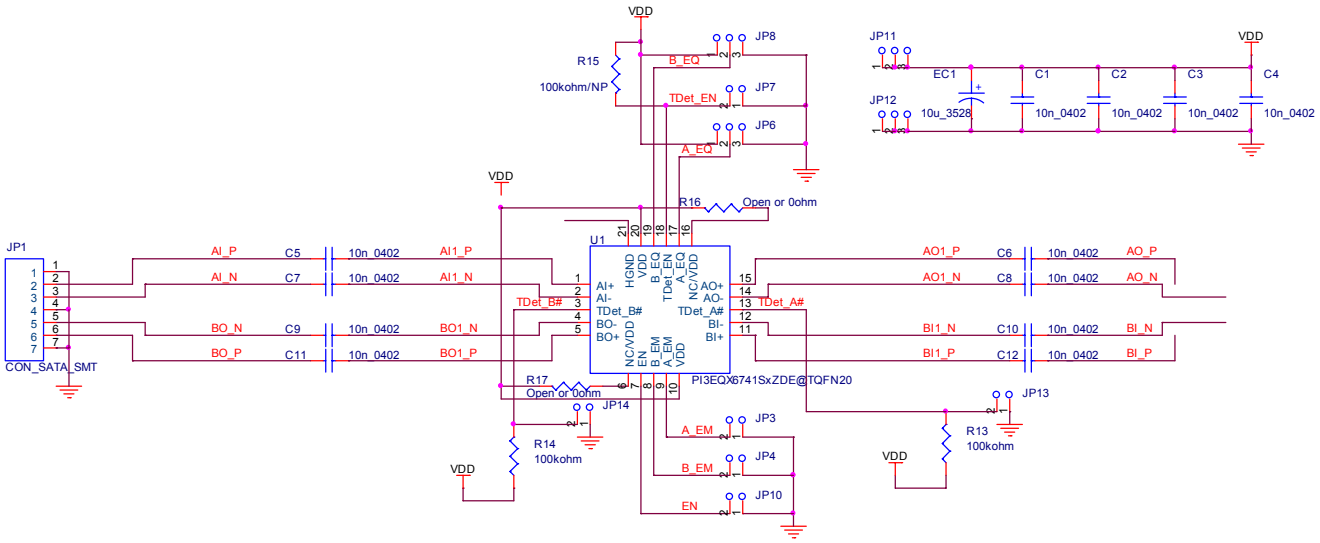
Power-on Sequence

It is recommended as good practice, that all system components be powered off while connections and configuration settings are made. There is no specific power-on sequence required when applying power to the PIxEQX6741SxZDE Eval Board. When connected to the system and powered by USB as shown above, then all devices will power-up together.

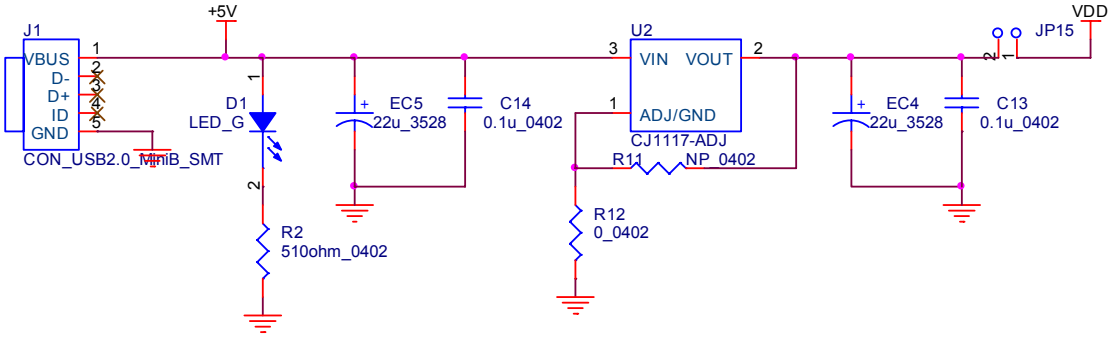
If the host PC and/or HDD are powered on, while the Eval Board is off, there will be no damage to the PIxEQX6741SxZDE under typical conditions. If the Eval Board is then powered on, the system will generally detect the SATA HDD as a hot-plug event, and the HDD will begin to operate properly. Note that some PC systems offer BIOS control over hot plug events, and if the HDD is not recognized, this BIOS setting is the most likely cause and should be changed. When connecting to the system as shown above, all devices will power on together and avoid this BIOS issue.

Board Design Information

- **PCB Schematic**



VDD: +3.3V for PI3EQX6741ST/STBZDE
+1.05V for PI2EQX6741SLZDE



- **PCB Layout Reference**
  a. Stack Up:

Layer #	Plane	Material type	mil
	Solder Mask		0.4
Layer 1	Signal		1.9
	Prepreg	Prepreg 1080 Prepreg 2116	7.3
Layer 2	Gnd		1.2
	Core		44
Layer 3	Power		1.2
	Prepreg	Prepreg 2116 Prepreg 1080	7.3
Layer 4	Signal		1.9
	Solder Mask		0.4

  b. Isolation Spacing = 30 mil
  c. Width & Spacing (W/S) of 100Ω Differential Trace = 10 / 9 mil

- **PCB BOM List**

Reference	Description	Package	Qty
U2	3.3V Regulator	SOT89	1
U1	PI3EQX6741STZDE or PI3EQX6741STBZDE or PI2EQX6741SLZDE	TQFN20-ZD	1
D1	LED	0805	1
JP1,JP2	SATA L-type connector	L-type	2
J1	miniUSB connector	B-type	1
JP3,JP4,JP7,JP10,JP13, JP14,JP15	2PIN HEADER	2.54mm	7
JP6,JP8,JP11,JP12	3PIN HEADER	2.54mm	4
C1,C2,C3,C4,C5,C6,C7,C8, C9,C10,C11,C12	Ceramic Capacitor, 10nF	0402	12
C13,C14	Ceramic Capacitor, 0.1uF	0402	2
EC1	Tan cap, 10u	3528	1
EC4,EC5	Tan cap, 22u	3528	2
R2	Chip Resistor, 510ohm	0402	1
R13,R14, R15	Chip Resistor, 100Kohm	0402	3
R12	Chip Resistor, 0ohm	0402	1

History

Version 1.0	Original Version	Mar. 23, 2011