Quiet FCT Logic Advantages

Replacement for ABT Logic

Introduction

With logic applications requiring faster clock speeds, which result in faster edge rates, the need for fast bus logic has become apparent. The problem is that the general result of a fast edge is excessive overshoot and undershoot that leads to ringing. Pericom's new Quiet Series devices are described in this brief. A quiet part is a part that has minimal overshoot, undershoot, ringback and ground bounce which means low noise.

The PI74FCT162QXXX series is a family of Quiet Double Density (16-bit wide) logic devices. This family not only offers almost noiseless operation, but also includes a bus hold feature. The following brief describes noise, bus hold operation, typical applications and a comparison to the competition.

What is Noise?

The Quiet Series was designed for light capacitance load applications of ~<70pF. For instance clock buffering, and low bank count memory are ideal uses for this product line. Figure 1 shows several sources of noise that should be averted to ensure proper operation. Most noise problems are a direct result of improper drive or termination. The Quiet Series has series resistance (shown in Figure 3) that, when added to the active pullup/pulldown, is about 40Ω. Fast edges cause overshoot and undershoot which are virtually eliminated by this technique.

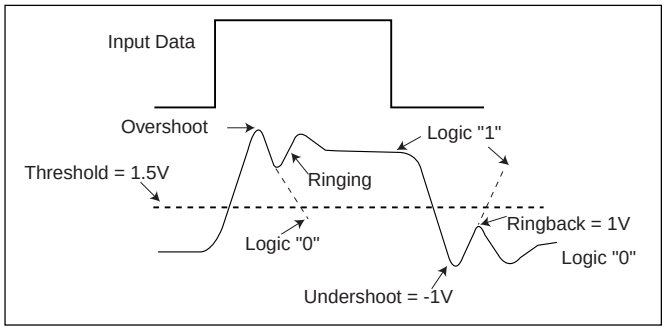

Figure 1. Typical Noise Waveform

Figure 2 exhibits another form of noise called ground bounce. By switching all bits simultaneously (B1 - B15) and checking one output (B16),who's input is grounded, one can measure ground bounce. Current, which is injected into the ground plane, is directly proportional to inductance L and di/dt. Ground bounce is a form of noise and directly relates to undershoot and ringback. Trace length is critical because trace capacitance (and inductance) change with trace length. Figure 3 shows a 60Ω trace impedance and 20pF per foot trace capacitance. The loaded impedance is 40Ω. Since

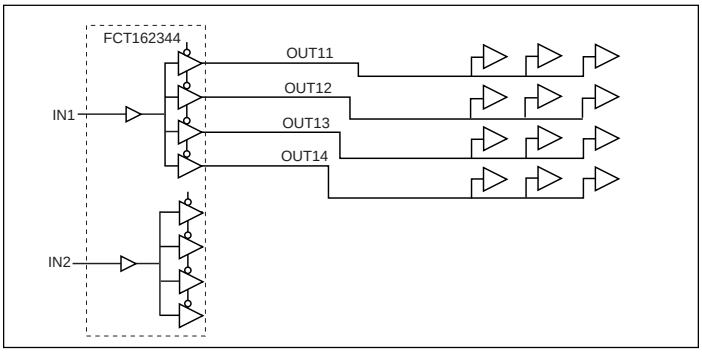

Figure 2. Ground Bounce Description

the output impedance of the PI74FCT162Q244/245 is typically 40Ω, there should be minimal refection because the loaded trace is matched to the driver output Z. Of course, as trace lengths change and the characteristic trace impedance changes, the loaded Z will change. Figure 3 shows this calculation. C_D is the load capacitance and C is the intrinsic line capacitance. R1 and R2 indicate the pullup and pulldown channel resistance.

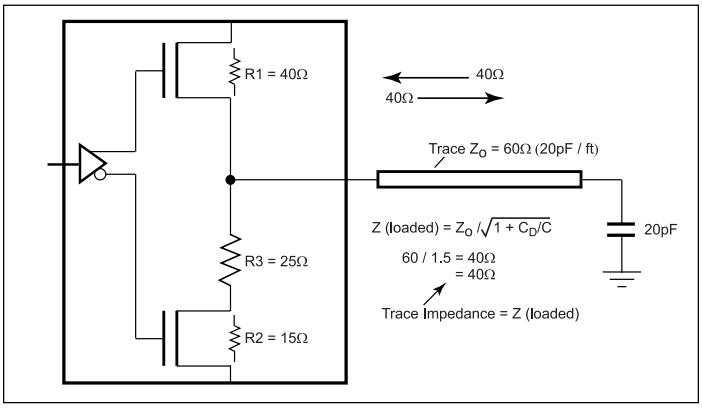

Figure 3. Description of Matched Line Impedance

Bus Hold Operation

Bus hold basically is a circuit that holds the last known state. Floating inputs do not need pullup/down resistors. All Quiet series devices have this feature. The bus hold sustaining current or hold current or hold current is 100µA.The effective bus hold capacitance is 8pF. It should be noted that *if floating inputs are left unterminated, oscillations may occur resulting in damage to devices not having the bus hold feature.*

Figure 5 shows the time it takes to acquire and hold data. The bus hold circuit consists of 2 inverters with propagation delays of 300ps each. The typical hold time is 600ps with a max of 1ns.

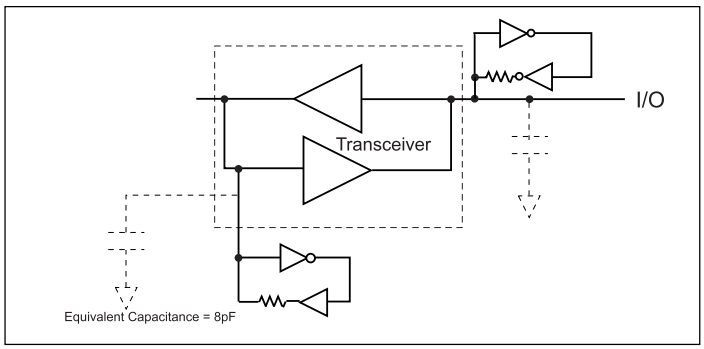

Figure 4. Bus Hold

Quiet Series Competition Comparison

Figures 6,7 and 8 depict waveforms (V_{CC} = 5V and C_L = 20pF) under light load conditions proving Pericom's PI74FCT162Q244/245 shows much less noise than the competition's "B" part and similar noise performance to the competition's "A" logic device. All products have the bus hold feature. Pericom compared its Q series to the competition in Table 1. ***Pericom's Q Series sub micron CMOS parts exhibit about 30% less power consumption compared to ABT's BiCMOS parts.***

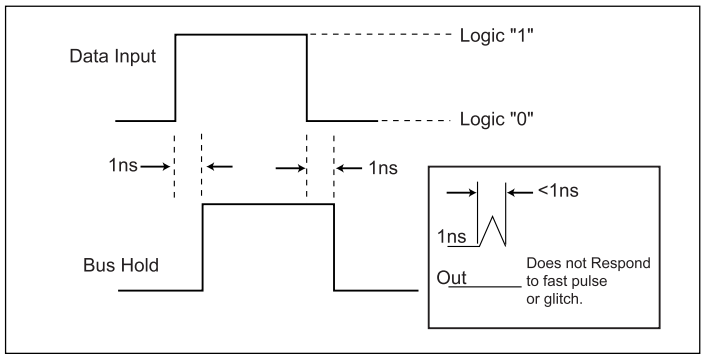

Figure 5. Quiet Series Comparison to Competition

Typical Application Hints

The Q Series parts are especially useful for PCI bus interface because this bus doesn't tolerate noisy logic. When buffering DRAM or SDRAM, and memory size is relatively low, it is very important to have a buffer with low overshoot and undershoot. Logic that doesn't have noise compensation will cause unwanted transition because of ringing and ringback (see Figure 1). Chip sets do not have enough drive for even light load (20pF to 50pF) applications. So quiet buffering is extremely important.

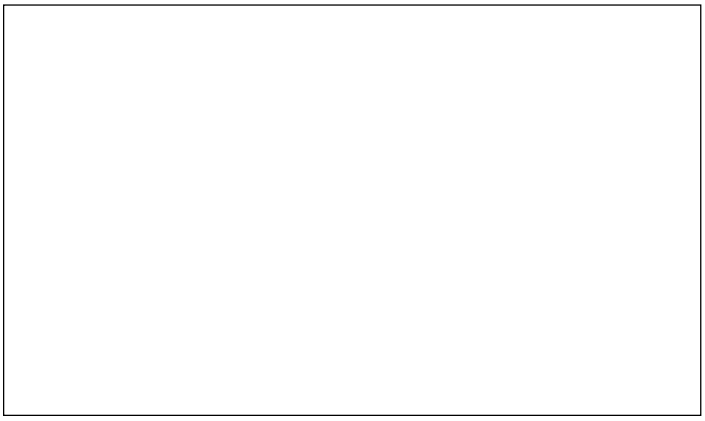

Figure 6. PI7FCT162Q244/245CTV

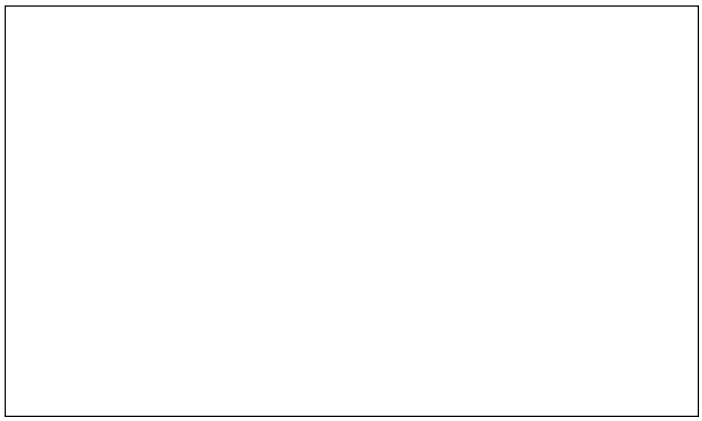

Figure 7. Competition A 74ABT162244/245DL

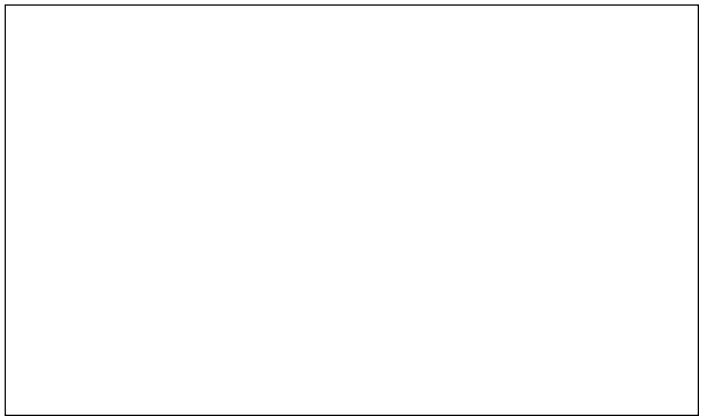

Figure 8. Competition B 74FCT162H244/245EPV

Table 1. Competitive Comparison (All Bits Switching Simultaneously)

Parameter/Part	**PERICOM** PI74FCT162Q244/245	**Competition A** 74ABT162244/245	**Competition B** 74FCT162H244/245E
Undershoot	0V	-0.2V	-1.5V
Ringback	0V	0V	0.7V
Ground Bounce	0.1V	0.1V	0.5V
I_{CC}, C_L = 20pF, f = 20MHz	90mA	110mA	90mA
I_{CC}, C_L = 20pF, f = 30MHz	140mA	160mA	140mA
I_{CC}, C_L = 20pF, f = 40MHz	170mA	220mA	170mA
I_{CC}, C_L = 20pF, f = 50MHz	230mA	310mA	230mA