Design Guides of PC133/100 Registered SDRAM Module

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Description

The "PC133 SDRAM Registered DIMM Design Specification, Rev. 1.0, May 1999," specifies the standard design of PC133 Registered SDRAM DIMM modules. The timings are very tight. To meet the specification, many PC133 DIMMs use a reference layout design, which is based on, or originated from, the Intel layout for PC100 SDRAM DIMM. By using a reference layout design, the challenge of designing a PC133 DIMM is greatly simplified.

The PC133 DIMM modules, using the same reference layout, have the same circuit schematic, have the same trace length, and have the same signal loading. If the SDRAM chips meet the specification, then a good PC133 DIMM design depends on only two key components – an address register and a PLL.

A Registered 168-pin DIMM is shown in Figure 1. There are 2 or 3 register chips for buffering the address/control signals from the DIMM connector. Only one PLL part is used to generate 9 or 10 copies of the reference input clock CK0 from the connector.

Figure 2 shows the address/control signal path on a DIMM module. These signals are clocked in at one of the register parts, then drives 9 or 18 SDRAMs. To drive 36 SDRAM chips, one address signal may have two outputs from register device. This path is most critical, because of signal loading. An AC analysis indicates that there is no timing margin for this path
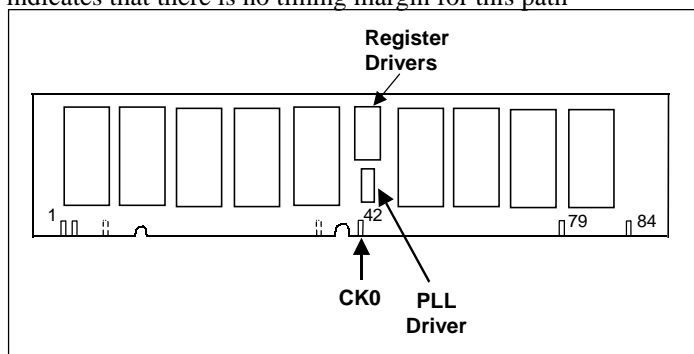

Figure 1. Registered 168-pin SDRAM DIMM

Address Register

The register is used to buffer the address/control signals. Each address/control signal drives up to 9 SDRAM loads for light load/non-stacked DIMM applications, or 18 SDRAM loads for heavy load/stacked DIMM applications. Table 1 lists the number of register parts used in each DIMM configuration defined in the PC133 Specification.

Table 1. Register Parts in Each DIMM Configuration

DIMM Configuration Raw Card Version	Total Number of SDRAMs	Pericom Register Part Number	Quantity of Register Parts per DIMM
A (Planar)	9	PI74ALVC 162835F/162834F	2
B (Planar)	18	PI74ALVC 162835F/162834F	3
B (Stacked)	36	PI74AVC 16835/16834	
C (Stacked)	36	PI74AVC 16835/16834	
D (Stacked)	36	PI74AVC 16835/16834	

Note: The pinouts of 16835 and 16834 are identical, except that the LE pin is high-active for 16835 and is low-active for 16834.
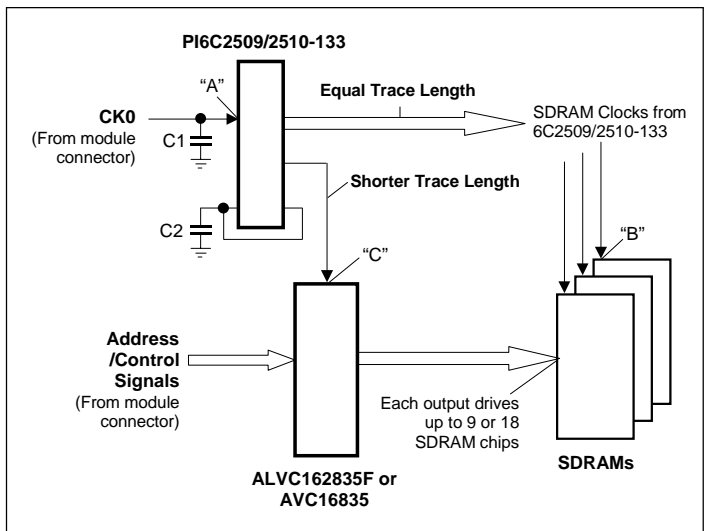

Figure 2. Address/Control Signal Critical Path on a DIMM Module

Figure 3 shows that the clock signal for the clock input pins at point "C" of the registers is adjusted to a negative value, -450 ps, relative to the reference clock CK0, at point "A", to gain timing margin. This is accomplished by shortening the trace length from a PLL output to the register's clock pin in the reference layout design.
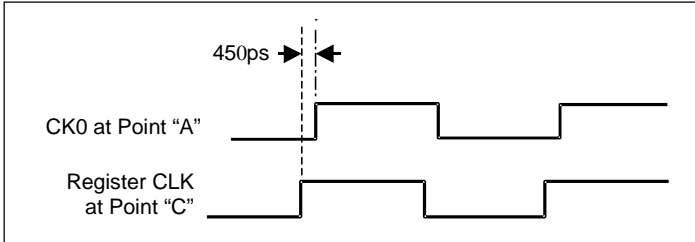

Figure 3. Register CLK at Point "C" leads CK0 at Point "A" in Figure 2

Pericom is very pleased that its ALVC 162835F/162834F parts have met all PC133 DIMM worst case simulation for *planar* Raw Cards applications (Raw Card A and Raw Card B planar configurations in Table 1).

Pericom's AVC16835/16834 parts are designed for heavy-load applications (Raw Cards B, C, and D stacked configurations). Each clock output has sufficient speed to drive up to 18 SDRAM loads.

PLL

The PLL device is used to buffer the clock signal and generate 9 or 10 clock signals from one clock input signal, as shown in Figure 4. Figure 5 shows the data signal path.
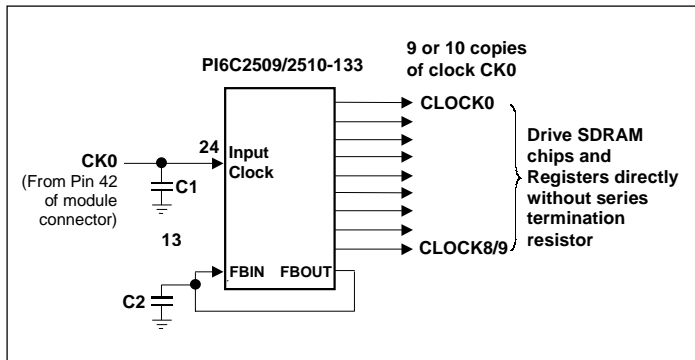

Figure 4. Block Diagram of PI6C2509/2510-133

To meet AC timing specs at the data signal critical path, the key feature of this PLL device aligns the clock signals at the SDRAM chips with the Reference Clock Input signal at the DIMM connector. If this requirement is not met, the data signal propagation time is then increased.

The clock signals at all SDRAM chips (Point "B") must align with the Reference Clock Input signal (Point "A"), as illustrated in Figure 6. If this is not aligned, the C2 capacitor value may be adjusted to accomplish the alignment. The PC133 DIMM specification specifies the C2 value.
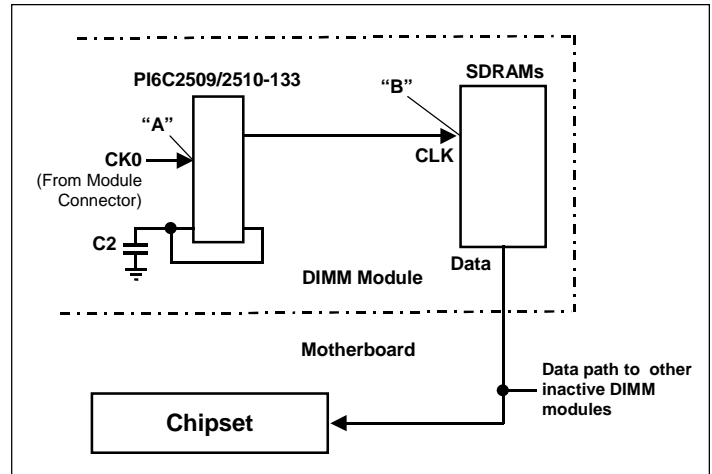

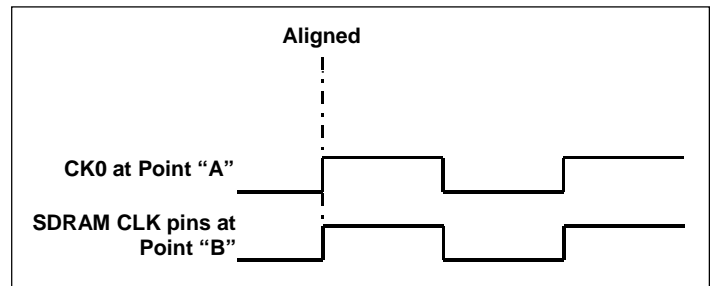Figure 5. Clock Connection from PI6C2509/2510-133 to SDRAM and Data Signal Path

Figure 6. The clock signals at all SDRAM Clock pins are aligned with CK0 at Point "A" in Figure 5.

For the PC133 reference layout design, Pericom 6C2509-133 and 6C2510-133 will align the clock signals at the SDRAM pins with the Reference Clock input signal CK0, as required by the PC133 Registered SDRAM DIMM specification.

Spread Spectrum Issue

Spread Spectrum Clocking (SSC) is a frequency modulation technique for EMI reduction. In the latest motherboards, the master clock generator chip does not maintain a constant frequency. SSC modulates the clock frequency/period at a predetermined modulation frequency of about 33 kHz. The modulation profile is also predetermined. As a result, the EMI from a motherboard is much reduced for meeting FCC requirement.

The reference input clock of an SDRAM DIMM is provided by the motherboard's master clock generator chip. As the clock frequency is constantly changing as a result of modulation, the frequency of the reference input clock of the DIMM PLL chip is constantly changing. For this reason, there is a new requirement on the DIMM PLL chip. In other words, the outputs of the DIMM PLL chip must "track" the reference input clock of the PLL chip. For example, when the reference input clock frequency is increasing, the output

clock frequency must be immediately increasing in approximately the same amount. Without this new feature, the output clocks could be randomly skewed, as compared with the reference input clock. Many of the old PLL clock buffer chips in the market do not have this feature at 133 MHz operation.

Pericom's 6C2509-133 and 6C2510-133 have this new feature, to ensure correct operation on the SSC motherboards.

Verifying using the PC133 Platform with
Spread Spectrum and Windows NT.

- Windows NT is more stringent than Windows 98 for testing DIMM modules.

- Enable Spread Spectrum and test DIMM module thoroughly.

The clock generator of new PC133 platforms provides clock signals with spread spectrum to CPU and SDRAM DIMM modules, for EMI reduction.

The spread spectrum feature is typically enabled by I²C programming after power up.

Summary
The PC133 Registered DIMM design is very challenging . However, the design can be greatly simplified by using a reference PC133 DIMM layout design and the PC133 spec compliant address register and PLL devices, such as the PC133 address register and PLL devices from Pericom , as shown below in Figure 7.
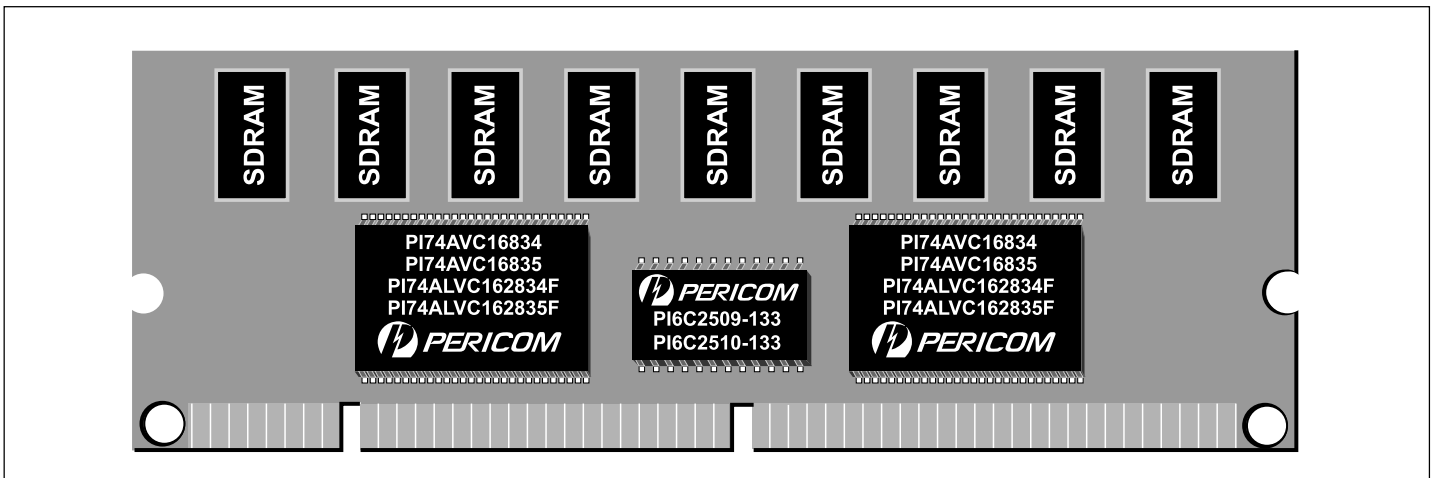

Figure 7. List of Pericom PC133 Address Registers and PLL Devices

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