AN1182

DGD2388M Application Note

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The DGD2388M is a highly integrated three-phase gate driver IC used to drive N-Channel MOSFETs or IGBTs. Below (Figure 1) is an example application of using the DGD2388M with IGBTs to make three half-bridge circuits used to drive a three-phase motor; typical motor applications are AC Induction motors, PMSMs, and BLDC motors. In this discussion, the important parameters needed to design in the DGD2388M are discussed; main sections are bootstrap resistor, diode, and capacitor selection, gate driver component selection, and decoupling capacitor value.

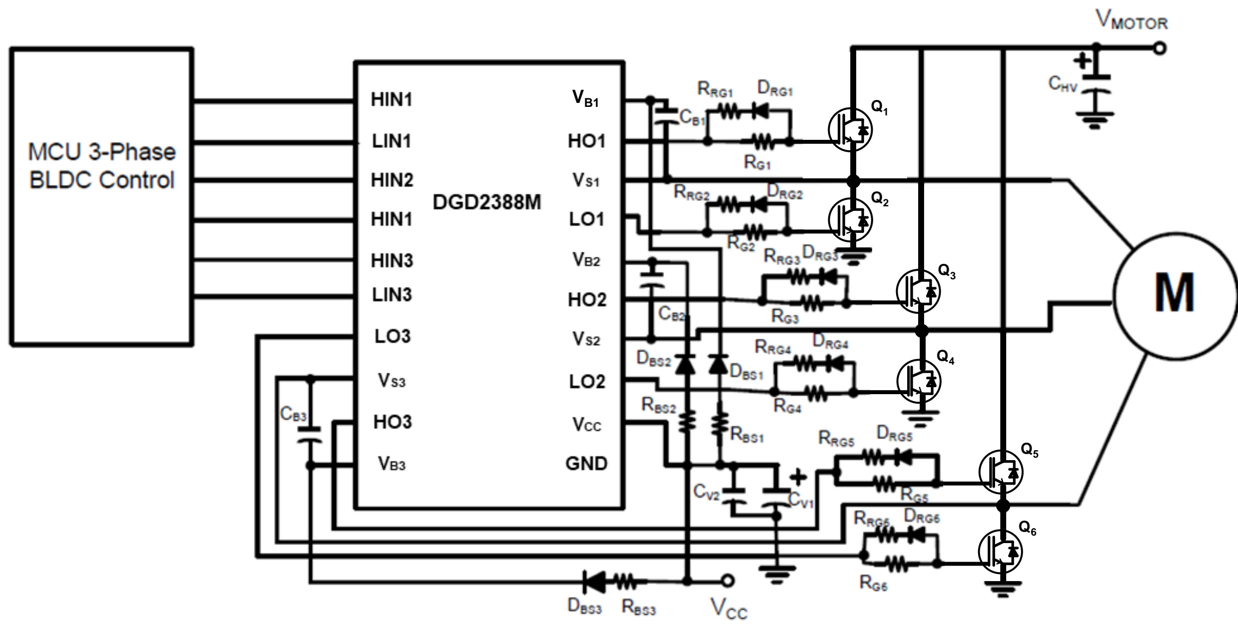

Figure 1. Application example of DGD2388M

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Bootstrap Component Selection

Bootstrap Resistor

Considering Figure 1, when the Low-Side IGBT (Q2, Q4, or Q6) turns on, V_S pulls to GND and the bootstrap capacitor (C_{B1}, C_{B2}, and C_{B3}) is charged. When the High-Side IGBT (Q1, Q3, and Q5) is turned on, V_S swings above V_{CC} and the charge on the bootstrap capacitor (C_B) provides current to drive the IC High-Side gate driver. The first charge of C_B from V_{CC} through the bootstrap resistor (R_{BS1}, R_{BS2}, and R_{BS3}) and bootstrap diode (D_{BS1}, D_{BS2}, and D_{BS3}) occurs when power is first applied, and Low-Side turns on the first time. At this time, the charge current is the largest, as typically C_B is not discharged fully at each cycle.

A bootstrap resistor (R_{BS}) is included in the bootstrap circuit to limit the inrush current that charges C_B when V_S pulls below V_{CC}; this inrush current is largest with the first charge. Limiting inrush current is desirable to limit noise spike on V_S and COM, potentially causing shoot-through. The amplitude and length of time of the inrush current is determined mostly by the component value of R_{BS} and C_B as well as V_{CC} level. The aim in resistor selection for the application is to slow down the inrush current but have minimal effect on the R_C time constant of charging C_B.

Typically, values for R_{BS} are 3Ω to 10Ω, enough to dampen the inrush current but have little effect on the V_{BS} turn on. Below are some scope shots illustrating the effect of different R_{BS} values.

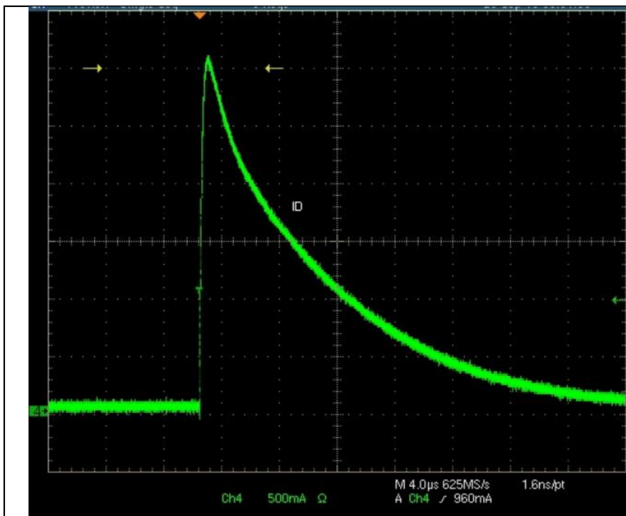

Figure 2. Bootstrap inrush current with R_{BS} = 3Ω, C_B = 2.2µF

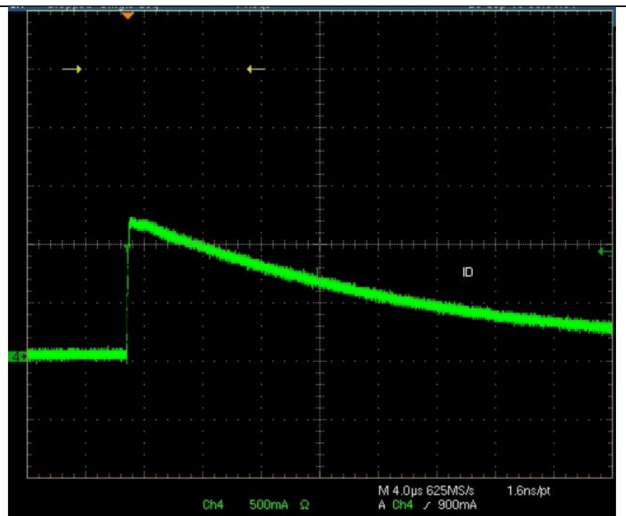

Figure 3. Bootstrap inrush current with R_{BS} = 10Ω, C_B = 2.2µF

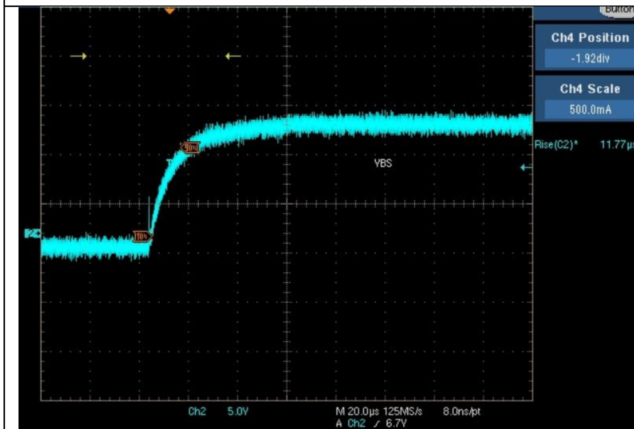

Figure 4. V_{BS} rise time (11.8µs) with C_B = 2.2µF and R_{BS}=3Ω resistor

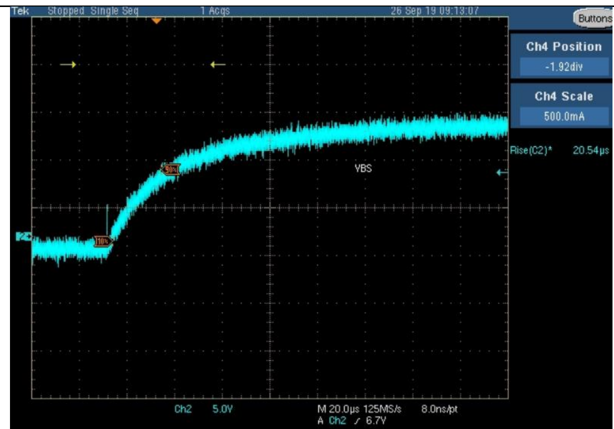

Figure 5. V_{BS} rise time (20.5µs) with C_B=2.2µF and R_{BS}=10Ω resistor

Bootstrap Diode

The chosen bootstrap diode (D_{BS}) should be rated higher than the maximum rail voltage since the diode must be able to block the full rail voltage and any spikes seen at the VS node. The diode's current rating is simply the product of total charge (Q_T) required by the HVIC and the switching frequency. An ultrafast recovery diode is recommended to minimize any delay of charging the bootstrap capacitor C_B. A 1A ultrafast recovery diode is typical for DGD2388M applications.

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Bootstrap Capacitor

The initial step in determining the value of the bootstrap capacitor is to determine the minimum voltage drop (ΔV_{BS}) that can be guaranteed when the High-Side device is turned on. In other words, the minimum gate-source voltage (V_{GSmin}) must be greater than the UVLO of the High-Side circuit, specifically V_{BSUV-} level. Therefore, if V_{GSmin} is the minimum gate-source voltage such that:
$V_{GSmin} > V_{BSUV-}$

Then:
$\Delta V_{BS} = V_{CC} - V_F - V_{GSmin} - V_X$

Where:

- V_{CC} is the supply voltage to the DGD2388M
- V_F is the voltage drop across the bootstrap diode (D_{BS})
- V_X is the voltage drop across the MOSFET or IGBT

V_X is calculated as the current seen across Low-Side MOSFET multiplied by its RDSON and is simply $V_{CE\text{-}ON}$ at the specify output current if an IGBT were used instead.

In addition to the voltage drops across these components, other factors that cause V_{BS} to drop are leakages, charge required to turn on the power devices, and duration of the High-Side on time. The total charge (Q_T) required by the gate driver then equals:

$Q_T = Q_G + Q_{LS} + [I_{LK_N}] * T_{HON}$

Where:

Q_G = Gate charge of power device
Q_{LS} = Level shift charge required per cycle
T_{HON} = High-Side on time
I_{LK_N} = Sum of all leakages that include:

- I_{GSS}/I_{GES}: Gate-source leakage of the power device
- I_{LK_DB}: Bootstrap diode leakage
- I_{LK_IC}: Offset supply leakage of HVIC
- I_{QBS}: Quiescent current for High-Side supply
- I_{LK_CBS}: Bootstrap capacitor leakage

Bootstrap capacitor leakage (I_{LK_CBS}) only applies to electrolytic types. Therefore, it is best not to use electrolytic capacitor. Thus, bootstrap capacitor leakages will not be included in the calculations.

Q_{LS} is not listed in the datasheet; depending on the process technology, it could range anywhere from 3nC – 20nC for 500V to 1200V process respectively. Assuming a value of 10nC for Diode's 600V, this process should be sufficient with added margin.

From the basic equation, the minimum bootstrap capacitor can be calculated as:

$C_{Bmin} \geq Q_T / \Delta V_{BS}$

Example using IGBT

- Power device: IRGB4066
- HVIC = DGD2388M
- V_{CC} = 15V
- Iout = 40A
- T_{HON} = 50us
- $V_{CE\text{-}max}$ = ~2.0V
- Q_G = 225nC
- I_{GSS}/I_{GES} = 200nA
- I_{LK_DB} = 100uA
- I_{LK_IC} = 10uA
- I_{QBS} = 130uA

From equations above:
ΔV_{BS} = 15V - 3.0V - 4V- 2.0V = 6.0V

$Q_T = Q_G + Q_{LS} + (I_{LK_N} * T_{HON})$
= 225nC + 10nC + 12nC
= 247nC

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Thus, C_B min = 254nC/6V = 41.2nF

The bootstrap capacitor calculated in the above problem is the minimal value required to supply the needed charge. It is recommended that a margin of 2 – 3 times the calculated value be used. In addition, if the added margin is significantly small still such that it is lower than 0.47µF, the minimal value should be brought up to this value. Utilizing values lower than this could result in over-charging of the bootstrap capacitor especially during $-V_S$ transients. Typically for motor driver applications C_B = 1µF to 10µF are used; it is also recommended to use low ESR ceramic capacitors as close to the V_B and V_S pin as possible (see PCB layout suggestions section).

Gate Resistor Component Selection

The most crucial time in the gate drive is the turn on and turn-off of the MOSFET, and performing this function quickly, but with minimal noise and ringing is key. Too fast a rise/fall time can cause unnecessary ringing and poor EMI, and too slow a rise/fall time will increase switching losses in the MOSFET.

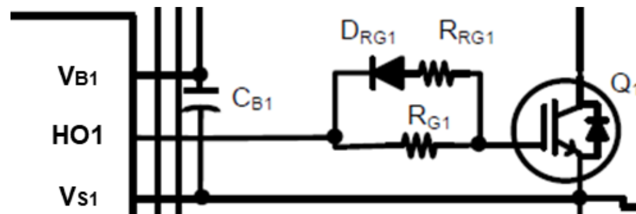

Figure 6. Phase1 gate drive components for DGD2388M

Considering the phase 1 gate driver components for DGD2388M in Figure 6, with the careful selection of R_{G1} and R_{RG1}, it is possible to selectively control the rise time and fall time of the gate drive. For turn on, all current will go from the IC through R_{G1} and charge the IGBT gate capacitor, hence increasing or decreasing R_{G1} will increase or decrease rise time in the application. With the addition of D_{RG1}, the fall time can be separately controlled as the turn off current flows from the MOSFET gate capacitor, through R_{RG1} and D_{RG1} to the driver in the IC to V_S. So, increasing or decreasing R_{RG1} will increase or decrease the fall time. Sometimes finer control is not needed and only R_{G1} is used.

Increasing turn on and turn off has the effect of limiting ringing and noise due to parasitic inductances, hence with a noisy environment, it may be necessary to increase the gate resistors. Gate component selection is a compromise of faster rise time with more ringing, and a poorer EMI but better efficiency, and a slower rise time with better EMI, better noise performance, but poorer efficiency. The exact value depends on the parameters of the application. Generally, for motors the switching speed is slower, and the application has more inherent noise, higher values are recommended, for example R_G = 20Ω - 100Ω.

Decoupling Capacitor Selection

For optimal operation, V_{CC} decoupling is crucial for all gate driver ICs including the DGD2388M; with poor decoupling, V_{CC} can drop when switching and for greater V_{CC} drop the IC can go into UVLO. In the configuration shown in Figure 1, two decoupling capacitors are recommended C_{V1} and C_{V2} (see Figure 7), both connected from V_{CC}-GND. C_{V1} can be a larger electrolytic, for example 47µF, 50V and does not need to be right next to the IC. But C_{V2} should be a low ESR ceramic capacitor placed close to the V_{CC} pin. This component provides stability when V_{CC} is quickly pulled down with load; typical values are 0.1µF to 1µF.

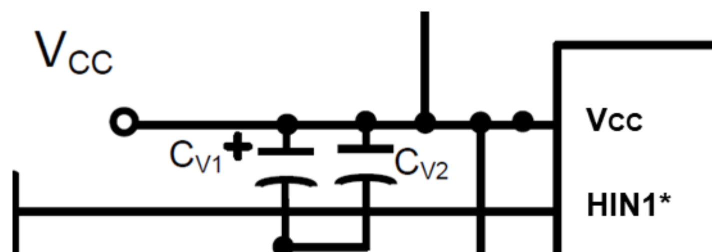

Figure 7. Decoupling capacitors on the DGD2388M

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Matching Gate Driver with MOSFET or IGBT

IC drive current and MOSFET/IGBT gate charge

Gate Driver ICs are defined by their output drive current, its ability to source current to the gate of the MOSFET/IGBT at turn on and to sink current from the gate of the MOSFET/IGBT at turn off. For the DGD2388M the drive current is IO+=420mA typical and IO-=750mA typical.

For a given MOSFET/IGBT, with the known drive current of the DGD2388M, you can calculate how long it will take to turn on/off the MOSFET/IGBT with the equation:

$t = Q_g / I$

Q_g = total charge of the MOSFET/IGBT as provided by the datasheet
I = sink/source capability of the gate driver IC
t = calculated rise/fall time with the given charge and drive current

For example, with Diodes Incorporated's (Diodes) DGTD65T15H2TF, 650V IGBT, Q_g = 61nC; and with the DGD2388M IO+/IO-, tr = 145ns and tf = 81ns. These are estimates as the total charge given in the datasheet may not be the same conditions in the application. Also, an addition of a gate resistor will increase the tr and tf.

MOSFET/IGBT Input Capacitance Ratio

In the half-bridge circuit (see Figure 8), when the Low-Side turns on, V_S swings low at a rate of dV_S/dt. Depending on the dV_S/dt of the system, and a ratio of C_{ies}/C_{res} of the IGBT, there can be an inadvertent turning on the High-Side IGBT during this transition; if this occurs shoot through will happen, possibly damaging the IGBT and causing inefficiency. Often, this is the reason for short unexplained shoot through. If this is the case, another IGBT with larger C_{ies}/C_{res} should be chosen, or a capacitor (for example 1nF) can be added between the gate and emitter of the IGBTs.

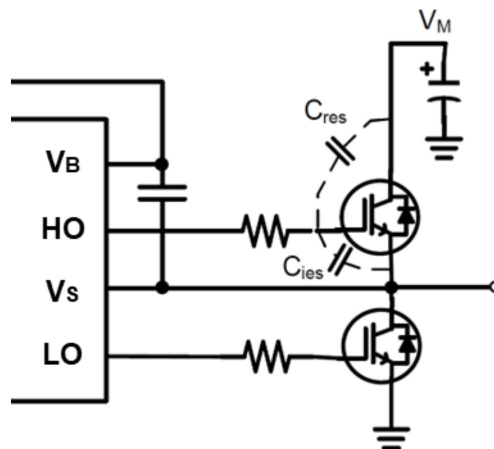

Figure 8. Half-bridge with High-Side IGBT equivalent capacitors

Minimum Pulse Requirement

The DGD2388M has a typical propagation delay of 120ns. With the prop delay of the DGD2388M, delay time from gate resistors, and rise/fall from the MOSFETs/IGBTs, for optimal operation, it is suggested to provide a minimum pulse width at the input to the IC from the MCU. As a rule of thumb, this minimum pulse should be 2x deadtime or 660ns.

PCB Layout Suggestions

Layout plays an important role in minimizing unwanted noise coupling, unpredicted glitches, and abnormal operation which can arise from poor layout. Figure 9 shows a single-phase half-bridge schematic with parasitic inductances in the high current path (L_{P1}, L_{P2}, L_{P3}, L_{P4}) which would be caused by inductance in the metal of the trace. Considering Figure 9, the length of the tracks in red should be minimized, and the bootstrap capacitor (C_B) and the decoupling capacitor (C_D) should be placed as close to the IC as possible as well as using low ESR ceramic capacitors. Finally, the gate resistors (R_{GH} and R_{GL}) and the sense resistor (R_S) should be surface mount devices. These suggestions will reduce the parasitics due to the PCB traces.

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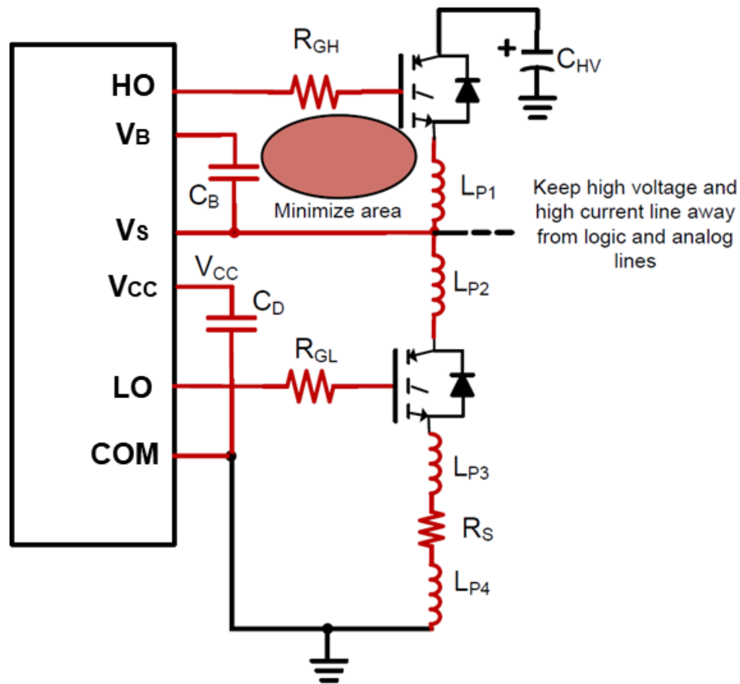

Figure 9. Layout suggestions for single phase of three-phase system

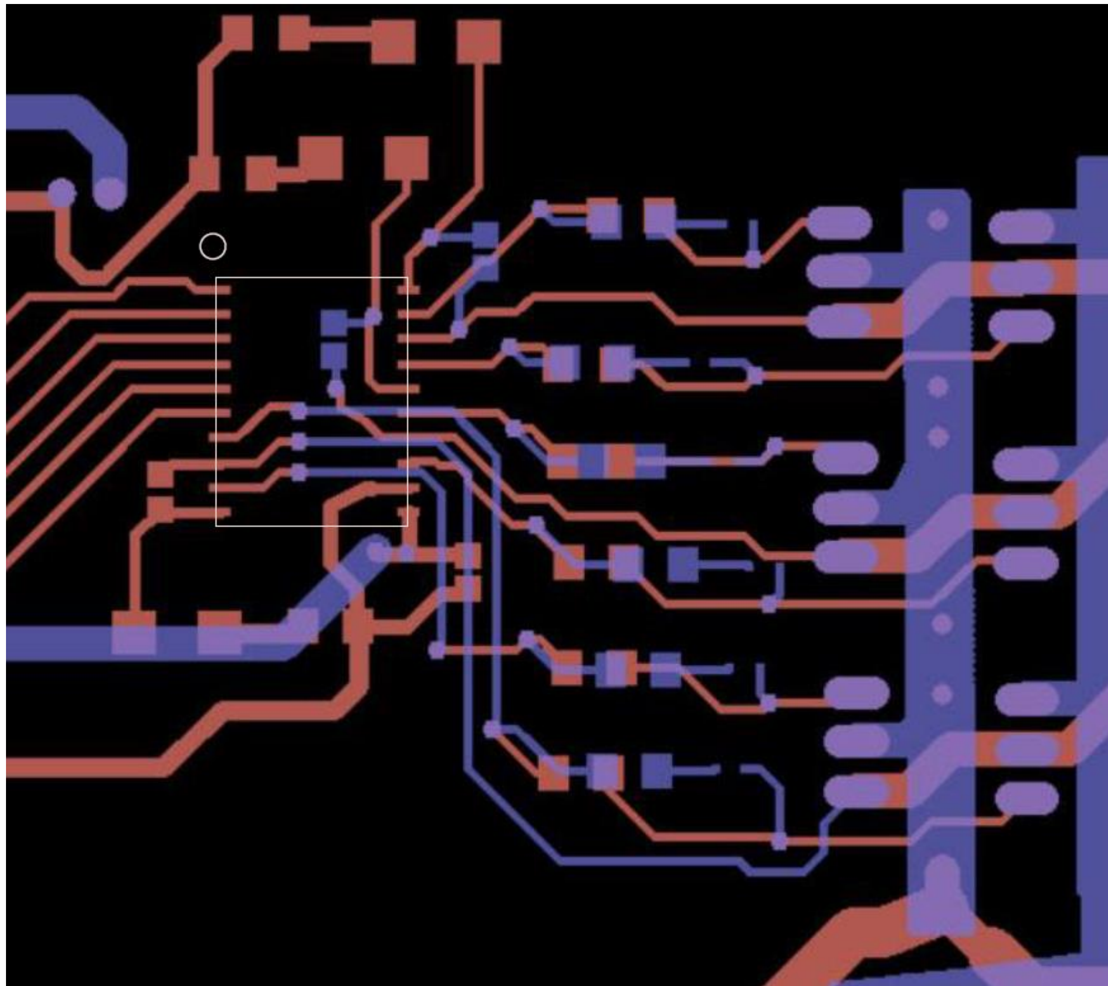

Figure 10. Layout of the schematic shown in Figure 1, DGD2388M in SOIC20, IGBTs in TO220 packages.

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