Replacing the PLX PCI6150 with the PI7C8150B

by Mohamad Tisani

1.0 Introduction

The PCI bus has been used for more than fifteen years and is still running strong. This interface is being developed in PCs, Servers, Notebooks, Datacom and Telecom Systems. With many different PCI devices and peripherals being placed in systems today, the need for PCI Bridges becomes essential.

Pericom Semiconductor Corp. has a broad selection of PCI to PCI bridges, including the PI7C8150 , PI7C8150 A, and the PI7C8150 B.
This application note discusses the differences between the Pericom Bridge PI7C8150 B and the PLX 6150.

2.0 Pin differences

1. The following are the pin differences for the PQFP package

Pin Number	Pericom PI7C8150B	PLX 6150/ HB4	Comments
51	VDD	Osc_Sel_L	8150B: Connect to VDD to work in async mode 6150:Connect Low to Work in async mode
54	VSS	Osc_In	8150B: Tie to Ground To work in async mode. 6150: Connect to the async clock for the secondary bus
103	VDD	EE_En_L	Tie High to disable the Serial EEPROM function. 8150B does not support the serial EPROM
106	MS1	Eject_En_L	Pull it high to work in asynchronous mode.
125	Cfg66/Scan_en/Clk_rate	Cfg66	Pull down: Sclkout are half the speed as the Async-clkin. If pulled high the same speed.
126	Msk_in/ Async_clkin	Msk_in	8150B: Asynchronous clock input to be used for the secondary bus. 6150: pull low to enable secondary output clocks
127	Reserved	Enum_L	Hot swap signal, NO connect is OK. 8150B does not support Hot swap
128	Reserved	LED	Hot swap signal, NO connect is OK. 8150B does not support Hot swap
151	VDD	Reserved	Connect to VDD
155	MS0	GPIO3_FN_L	Pull High for normal operation
158	VSS	EEPCLK	Connect to Ground.
160	VSS	EEPD	Connect to Ground.

2. The following are the pin differences for the BGA package

Ball Number	Pericom 8150 B	PLX 6150/HB4	Comments
K16	Cfg66/ Scan_en/ Clk_rate	Osc_sel_l	8150B: Pull down, Sclkout are half the speed as the Async-clkin. If pulled high the same speed. 6150:Connect Low to Work in async mode
K15	Msk_in/ Async-clkin	Osc_in	Asynchronous clock input to be used for the secondary bus.
C15	VDD	EE_EN_L	Tie High to disable the Serial EEPROM function. 8150B does not support the serial EPROM
R16	MS1	EJECT_EN_L	Pull high To work in asynchronous mode. 8150B does not support Hot swap
J14	Reserved	ENUM_L	Hot swap signal, NO connect is OK. 8150B does not support Hot swap
J16	Reserved	LED	Hot swap signal,

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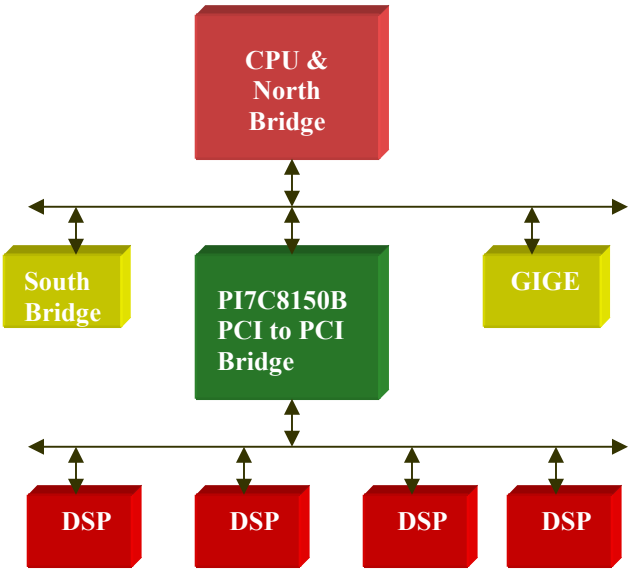
			NO connect is OK. 8150B does not support Hot swap
B14	MS0	GPIO3FN_L	Tie High to work in asynchronous mode
C14	VSS	EEPCLK	Connect to Ground. 8150B does not support the serial EPROM
D14	VSS	EEPD	Connect to Ground. 8150B does not support the serial EPROM

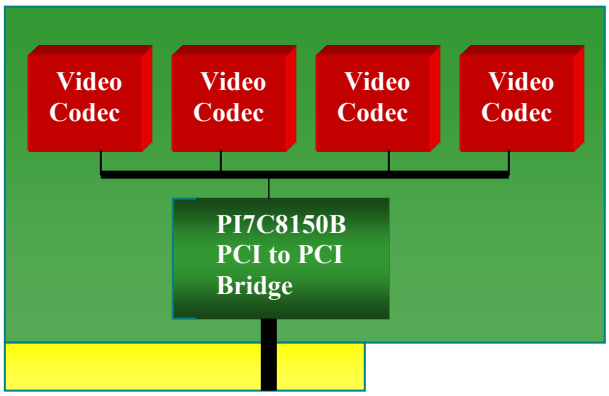
3.0 Applications

The PCI to PCI Bridge is used in the following applications:

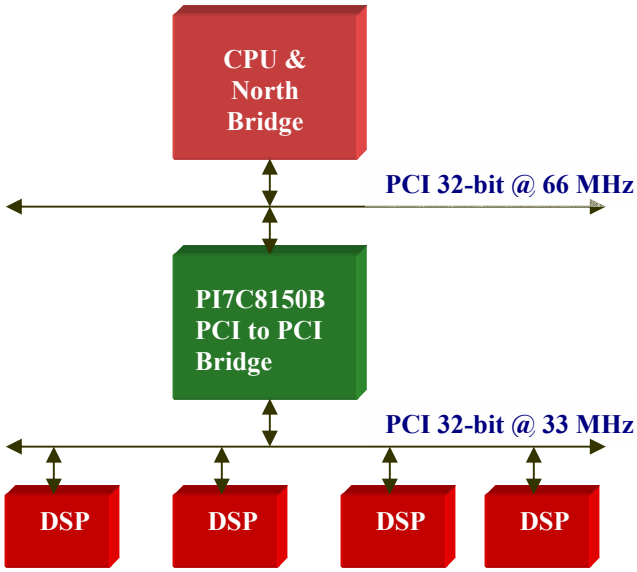
3.1 Bus Expansion. On the motherboard, in order to add more slots.



3.2 On the Add_ in cards if there is more then one PCI load.



3.3 Bus isolation in order to isolate the high-speed devices from the lower speed chips.



4.0 Unique features

Apart from pin differences the 8150B have many enhanced features:

4.1 Industrial Range

The chip is also offered in industrial range. This feature will enable the designer to place the chip in extreme temperature range as low as – 40 Celsius and as hot as + 85 degrees Celsius. If the chip is not used in this extreme environment, this feature will provide plenty of AC timing margin.

4.2 Optimum FIFO size

Pericom have experimented with many different number of write and read FIFO's. The Analysis was done on many different applications. Our Analysis indicated that we need the following FIFO size to achieve the best performance:

- 512 bytes delayed read transaction FIFO's for both the primary and the secondary sides.
- 256 bytes of posted write buffers for both the primary and the secondary sides.

The data indicated that bigger FIFO's are not necessarily better. You have to choose the right number in order to service both the write and the read transactions. This Architecture proved to be the optimum based on the performance report, which is also provided on the web site for your convenience.

4.3 Dynamic Prefetching

This is a unique feature that is integrated into the bridge. As you know in the PCI bus writes go fast, since most every device have a buffer where they immediately accepts the writes without adding many wait states. Read Transactions are more complex. Normally reads take much longer time. The bridge has to flush the write buffers and then request the read form the destination chip. The chip also can get one cache line or many cache lines. Usually the user does not know how many it needs since it depends on the chipset that is used and the application. The 8150B have a feature that automatically adjusts to the optimum number of cache line reads in order to match the requested reads. This will result in better performance and better utilization of the bus so that we do no waste the bus bandwidth and read extra transactions to discard them later. On the other hand we will not read less read transactions then needed so that we will starve the initiator that is requesting the read transactions.

5.0 Conclusion

The 8150 B have many superior features to the competition and it is also pin to pin compatible except for couple of pin differences. Please see the table provided above to ensure that the Asynchronous clock is connected to the proper pin. If you are not using the Serial EEPROM feature and the hot swap pins then the Pericom PI7C8150B can be dropped in into the 6150 Socket with couple of pin changes.
This chip is intended to be used in Asynchronous secondary bus operation. For synchronous operation, please use the 8150A chip.