Pericom PCI-to-PCI Bridge Intel/TI/PLX substitute

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Introduction

According to different chips and packages in the following list, this application brief provides the pin difference descriptions and the guidelines for device replacement. Each section is discussed accordingly.

- PI7C8140A, 128-pin PQFP
- PI7C8148A/B, 160-pin PBGA
- PI7C8150/A/B, 208-pin FQFP
- PI7C8150/A/B, 256-pin PBGA
- PI7C8152/A/B, 160-pin MQFP
- PI7C8154/A/B, 304-pin PBGA

PI7C8140A vs. PLX 6140, PQFP-128

Basically, Pericom PI7C8140A can make direct replacement with PLX 6140 (HB1) without making any change. The only point that needs to pay attention is the pin number 106. We will suggest remove the pull-up resistor used for PLX6140 at pin 106, and leave the pin opened for PI7C8140A when making device replacement.

The pin status of PI7C8140A and PLX6140 are described here for user's reference.

- For Pericom PI7C8140A, the pin 106 is defined as test mode I/O pin "SCAN_EN". During normal operation i.e. SCAN_TM# is pulled-up, the pin is set to output status "LOW".

- For PLX 6140, the pin 106 is defined as "S_IDEN" which must be pulled-up for proper operation.

PI7C8148A/B vs. PLX 6152, PBGA-160

Pericom PI7C8148A/B can make direct replacement with PLX 6152 (HB1) without making any change.

PI7C8150/A/B vs. Intel 21150, FQFP-208

Pericom PI7C8150/A/B can make direct replacement with Intel 21150 without making any change.

In addition to the same functions as 21150, 8150B can further provide asynchronous mode support**.** For synchronous operation (e.g. 8150/8150A and Intel 21150), both primary bus and secondary bus are running at the same clock rate. For asynchronous operation (7C8150B), primary bus and secondary bus can run at different clock rates. The alternative mode selection can be controlled by using the multiple function pins - MS0 & MS1.

Several pins are listed in the following table for user's information during device replacement.

Pin Number	PI7C8150/A/B	Intel 21150
106	MS1	VSS
125	CFG66 / SCAN_EN / *CLK_RATE	CFG66
126	MSK_IN / *ASYNC_CLKIN	MSK_IN
127	RESERVED	NC
128	RESERVED	NC
155	MS0	VDD

- MS0 and MS1 are used to select synchronous or asynchronous mode, their settings are correspondent to the following table:

MS1	MS0	Description
1	1	Asynchronous Mode – such as 8150B
0	1	Synchronous Mode - such as 8150/A and Intel 21150
X	0	Reserved

- CFG66 / SCAN_EN / *CLK_RATE:
  1. For "CFG66" (synchronous mode) - it is used to designate 33/66MHz operation. Tie the pin to "HIGH" for 66MHz operation or tie the pin to "LOW" for 33MHz operation.
  2. For "SCAN_EN" (synchronous mode), this pin also confirms full-scan is in shift/parallel operation and is valid only for test mode. For normal operation, the pin works in CFG66 synchronous mode.
  3. For "*CLK_RATE" (asynchronous mode), this pin is only supported by 8150B. It determines the S_CLKOUT frequency relation to ASYNC_CLK_IN.
     0: S_SCLKOUT is half the frequency of ASYNC_CLK_IN.
     1: S_CLKOUT is the same frequency as ASYNC_CLK_IN.

- MSK_IN / *ASYNC_CLKIN:
  1. For "MSK_IN" (synchronous mode), this pin is used to disable secondary clock outputs. This pin can be tied to "LOW" to enable all secondary clock outputs or tied to "HIGH" to drive all the secondary clock outputs high.
  2. For "*ASYNC_CLKIN" (asynchronous mode), this pin is only used by 8150B. The asynchronous clock for the secondary interface should be connected to this pin,

and S_CLKOUT [9:0] will be derived from ASYNC_CLKIN

- RESERVED is same as NC, i.e., not connected.

PI7C8150/A/B vs. TI 2050, FQFP-208

If user adopts TI 2050 to perform the same function as Intel 21150, Pericom 8150/A/B can replace 21150 directly. For TI2050 to act the same as 21150, the pin 155 "MS0" must be pulled to "HIGH". User can check this pin to judge the functional setting.

PI7C8150/A/B vs. PLX 6150, FQFP-208

If user adopts PLX6150 (HB4) to perform the same function as Intel 21150, Pericom 8150/A/B can replace 21150 directly.

Most of the 6150 pin definition and arrangement are same as Pericom 8150/A/B except EEPROM, Hot Swap and Clock Source selection pins. Following table describes the pin differences. And please refer to the Diagram A for design reference.

Pin Number	PI7C8150/A/B	PLX 6150 – HB4
51	VDD	OSC_SEL#
54	VSS	OSC_IN
103	VDD	EE_EN#
106	MS1	EJECT_EN#
125	CFG66 / SCAN_EN / CLK_RATE	CFG66
126	MSK_IN / ASYNC_CLKIN	MSK_IN
127	RESERVED	PIN_ENUM#
128	RESERVED	PIN_LED
151	VDD	RESERVED
155	MS0	GPIO3FN#
158	VSS	EEPCLK
160	VSS	EEPD

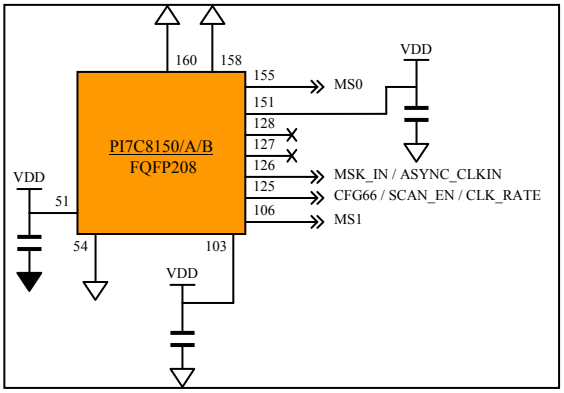

Diagram A

For settings of CFG66 / SCAN_EN / CLK_RATE, MSK_IN / ASYNC_CLKIN, and MS0 & MS1, please refers to the previous section "*PI7C8150/A/B vs. Intel 21150, FQFP-208*"

PI7C8150/A/B vs. Intel 21150, PBGA-256

Pericom PI7C8150/A/B can make direct replacement with Intel 21150 without making any change.

For additional 8150/A/B features such as CFG66 / SCAN_EN / CLK_RATE, MSK_IN / ASYNC_CLKIN, and MS0 & MS1, please refer to previous section "*PI7C8150/A/B vs. Intel 21150, FQFP-208*". The following table describes the pins with multiple functions.

Pin Number	PI7C8150/A/B	Intel 21150
B14	MS0	VDD
J14	RESERVED	NC
J16	RESERVED	NC
K15	MSK_IN / ASYNC_CLKIN	MSK_IN
K16	CFG66 / SCAN_EN / CLK_RATE	CFG66
R16	MS1	VSS

PI7C8150/A/B vs. PLX 6150, PBGA-256

If users system is bound with PLX 6150 (HB4) and just only need to run the same function as Intel 21150, Pericom 8150/A/B can replace directly.

Following table can provide the pin difference. And please refer Diagram B for your design note reference.

Pin Number	PI7C8150/A/B	PLX 6150 – HB4
B14	MS0	GPIO3FN#
C14	VSS	EEPCLK
C15	VDD	EE_EN#
D14	VSS	EEPD
J14	RESERVED	PIN_ENUM#
J16	RESERVED	PIN_LED#
K15	MSKIN / ASYNC_CLKIN	OSC_IN
K16	CFG66 / SCAN_EN / CLK_RATE	OSC_SEL#
R16	MS1	EJECT_EN#

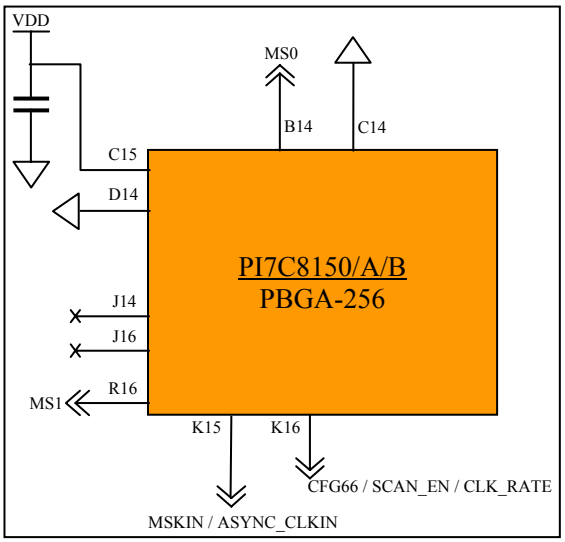

Diagram B

For setting of CFG66 / SCAN_EN / CLK_RATE, ASK_IN / ASYNC_CLKIN, and MS0 & MS1, please refers previous section - "*PI7C8150/A/B vs. Intel 21150, FQFP-208*"

PI7C8152/A/B vs. Intel 21152, MQFP-160

Pericom PI7C8152/A/B can make direct replacement with Intel 21152 PCI-to-PCI Bridge without making any change.

PI7C8152/A/B vs. TI 2250, MQFP-160

If users system is bound with TI 2250 and just only need to run the same function as Intel 21152, Pericom 8152/A/B can replace directly.

For TI 2250, its Intel compatible mode is depending on the pin 120 - MS0 must be pulled high.

PI7C8152/A/B vs. PLX 6152, MQFP-160

If users system is bound with PLX 6152 (HB1) and just only need to run the same function as Intel 21152, Pericom 8152/A/B can replace directly.

Following table can provide the pin difference. And please refer Diagram C for your design reference.

Pin Number	PI7C8152/A/B	PLX 6152 – HB1
5	S_LOCK_L	Reserved
49	S_CFN_L	Reserved
102	P_LOCK_L	Reserved
125	VDD	Reserved

- P_LOCK_L & S_LOCK_L: The primary and secondary bus lock signal. If no use, the pins can be unconnected. But it must be externally pulled-up.

- S_CFN_L: Secondary PCI central function enables. When tied low, S_CFN_L enables the secondary bus arbiter. When tied high, S_CFN_L disables the internal arbiter.

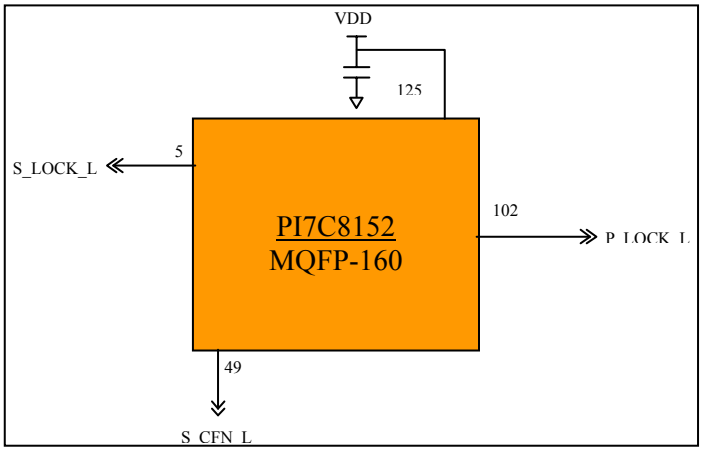

Diagram C

PI7C8154/A/B vs. Intel 21154, PBGA-304

Pericom PI7C8154/A/B can make direct replacement with Intel 21154 chip without making any change.

Following table is 8154/A/B pins of additional feature.

Pin Number	PI7C8154/A/B	Intel 21154
A22	VDD / * EEDATA	VDD
A23	VSS / * EECLK	VSS
B6	VDD / *NC	VDD
D11	PMEENA_L	VDD
V20	Reserved	VSS
Y18	Reserved	VDD
AA22	VSS / * NC	VSS
AB1	VDD / *ASYNC_SEL#	VDD
AB2	VSS / * ASYNC_CLKIN	VSS
AC22	VDD / * EE_EN#	VDD

- VDD / *EEDATA – For 8154, this pin is defined as power pin. For 8154A/B, this pin is used as serial data interface for EEPROM.

- VSS / *EECLK – For 8154, this pin is defined as ground pin. For 8154A/B, this pin is used as serial clock interface for EEPROM.
- VDD / *NC – For 8154/A, this pin is defined as power pin. For 8154B, this pin can be no connected.
- PMEENA_L is used to indicate the secondary devices are capable of asserting PME_L or not. For Intel compatible, this pin can directly tie to VDD.
- For pin V20, it must be tied to ground.
- For pin Y18, it must be tied to VDD.
- VSS / *NC – For 8154/A, this pin is defined as ground pin. For 8154B, this pin can be no connected.
- VDD / *ASYNC_SEL# - For 8154/A, this pin is defined as power pin. For 8154B, this pin is used as enables asynchronous mode for the bridge.
  0: Secondary bus clock outputs (S_CLKOUT [9:0]) will use the clock signal from ASYNC_CLKIN input instead of the P_CLK.
  1: Secondary bus clock outputs (S_CLKOUT [9:0]) will use the P_CLK input for synchronous operation.
- VSS / * ASYNC_CLKIN – For 8154/A, this pin is defined as ground pin. For 8154B, this pin is used as an external clock input in order to generate the secondary clock outputs (S_CLKOUT [9:0]) when enabled by ASYNC_SEL#.
- VDD / * EE_EN# – For 8154, this pin is defined as power pin. For 8154A/B, this pin is used as enable EEPROM interface when it is tied low.

PI7C8154/A/B vs. PLX 6154, PBGA-304

Pericom PI7C8154B can make direct replacement with PLX 6154 (HB2) chip without making any change.

Following table can provide the pin comparison. And please refer Diagram D for your design reference.

Pin Number	PI7C8154	PLX 6154 – HB2
A22	VDD / *EEDATA	EEPDATA
A23	VSS / *EECLK	EEPCLK
B6	VDD / *NC	NC
D11	PMEENA_L	VDD
V20	Reserved	VSS
Y18	Reserved	VDD
AA22	VSS / *NC	NC
AB1	VDD / *ASYNC_SEL#	OSCSEL#
AB2	VSS / *ASYNC_CLKIN	OSCIN
AC22	VDD / *EE_EN#	EE_EN#

For the above signals usage, please refer previous section – "*PI7C8154/A/B vs. Intel 21154, PBGA-304*"

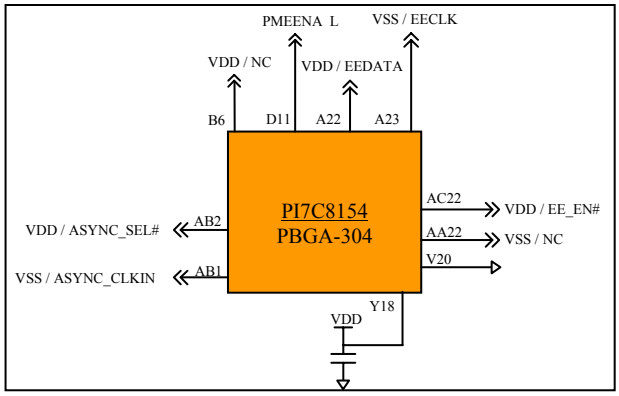

Diagram D