User Guide for PI7C8152 Reference Board

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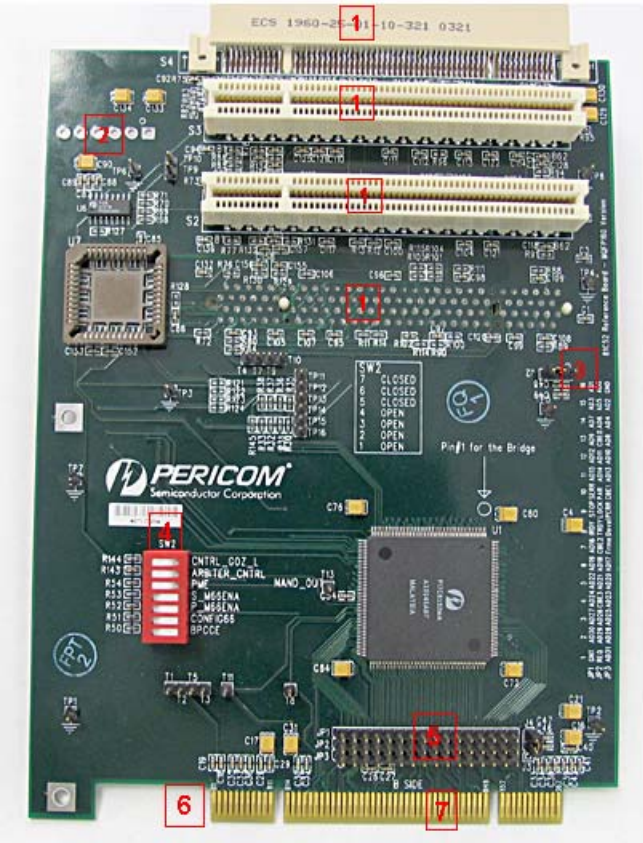
Introduction

The Pericom PI7C8152 bridge evaluation board demonstrates the bridge and allows testing of key features either before or during design / layout stages. The PI7C8152 Bridge complies with PCI Local Bus Specification Revision 2.2, as well as PCI Bridge Specification Revision 1.1.

Quick start (*photo of PI7C8152 reference board*)

The numbers on the photo correspond to the text explanation on the right:



1) Three standard and one straddle mount PCI connector.
2) Auxiliary power connector. (No need to connect external power in most applications). The host PCI bus can power all 4 secondary bus slots.
3) Secondary VIO Voltage Select to the slot can be set to either 3.3V or 5V. (Secondary VIO Voltage Select to the slot is set to 3.3V at J2 by default)
4) Switch to set bus speed and miscellaneous functions.
5) Headers for sampling signals on the primary PCI bus.
6) Pin 1 on the golden PCI-X edge connector faces left when looking down on the component (bridge IC socket).
7) Universal Edge Connector can be connected into a 3.3V slot or a 5V slot

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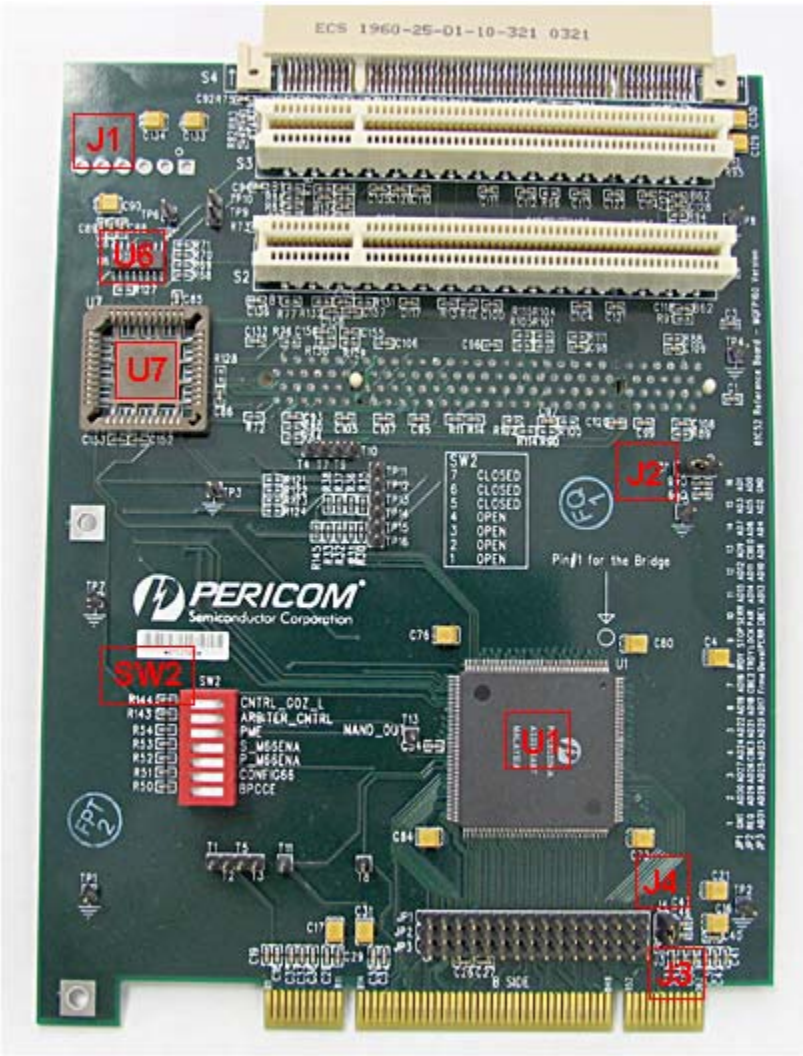
Components and Jumper Reference



U1 Pericom 7C8152 Bridge
U6 PI3B3257-W Mux/Demux bus switch
U7 Socket for optional external arbiter

SW2 Speed, options selection

J1 Auxiliary power connector, **not stuffed**
J2 Secondary bus VIO select
J3 +3.3V source, **not stuffed**
J4 Primary VIO follows motherboard

TABLES:

a) Right side of board has JP1, JP2 and JP3 list
b) **SW2 default stencil** list is ***replaced by this manual***

Switch Settings

Default and (*) important switch settings at a glance:
SW1 *there is no SW1.*

SW2	Signal	Default	Full Description
1	BPCCE	On	**"Off"** Enables bus/power clock control function (**BPCCE is high**) **"On"** Puts a low at this signal. (This influences turning off PCI clocks under ACPI power management.)
2	CFG66	Off	"**Off**" Bridge is 66Mhz capable. **"On"** Bridge is set to 33Mhz on **both** primary and secondary buses.
3	P_M66EN	On	"**Off**" Sets P_M66EN HIGH. Reference board can be used in 66MHz motherboard slot. **"On"** Reference board can be used in either 33MHz or 66MHz motherboard slot.
4	S_M66EN	Off	"**Off**" Sets Secondary bus is 66Mhz capable (S_M66EN is high) **"On"** Forces 33Mhz secondary bus even if primary bus is 66Mhz. (S_M66EN low)
5	PME#	Off	De-asserts PME# to motherboard, this switch **must** be **"Off**"
6	ARBCTRL	On	**"On"** Internal arbiter is selected. **"Off"** selects external arbiter but other changes needed also to activate external arbiter. See page 6.
7	CTRL_GOZ#	Off	Ties to pin 63 "SCAN_TM_L"

Jumper Settings

Jumper	Signal	Default	Full Description
J1	Not Connected	NC	**Auxiliary Power Connector**, this does not need to be connected to use the bridge.
J2	Secondary VIO Voltage Select to the slot	Pin 2-3	**"Pin 2-3"** Secondary VIO voltage select to the slot is set to 3.3V. **"Pin 1-2"** Secondary VIO voltage select to the slot is set to 5V.
J3	Not Used	NC	
J4	Primary VIO Voltage Select	Pin 1-2	The topmost pin at **J4** is **P_VIO** from the motherboard and the center pin goes to our bridge.

Before Powering the Board

a) Speed selection:

Using the switch **SW2, choose the speed setting for the secondary bus** based upon the input primary bus speed:

SW2	33/33	66/33 Secondary	66/66	Default
2-**2** CONFIG66	On	**Not supported**	Off	**Off**
2-**3** M66EN **primary**	On	**Not supported**	Off	**Off**
2-**4** M66EN **secondary**	On	**Not supported**	Off	**Off**

(**Note:** The secondary bus will have output clocks at the same frequency of the input primary clock regardless of M66EN status at either bus.)

b) Seat the board into a PCI slot on the main system board

Looking from the front of the motherboard, the small lip on our reference board points to the back of the motherboard, and the component side with the PI7C8152 bridge chip is on the left hand side. The motherboard PCI connector is adequate to powering the board with a few add-in cards.

c) Connect any PCI cards desired on the secondary PCI bus

For all PCI connectors on our reference board, when looking down onto the bridge IC, pin 1 is on the left side of the board. Notice that the external arbiter socket on the topside is closest to PCI connector pin1. This also applies to the top mounted "straddle" connector. The PCI slots are keyed for 3.3V or universal connector add-in cards; putting in any cards backwards will short 5V to GND through the PCI connector. Also each PCI connector has "A1", "B1", "A62", "B62" at the 4 corners of each slot, as a reminder where pin 1 is on each connector.

At this point, the Pericom PI7C8152 reference board is ready for you to use.

Primary Bus Test Points J1, J2, J3:

These allow a logic analyzer or oscilloscope to monitor signals on the path between the 7C8150 and the primary bus. There are 3 rows of 16 header pins, labeled J1, J2 and J3.

Test Point	1	2	3	4	5	6	7	8
JP1	GNT	AD30	AD27	AD24	AD22	AD19	AD16	IRDY
JP2	REQ	AD29	AD26	CBE3	AD21	AD18	CBE2	TRDY
JP3	AD31	AD28	AD25	AD23	AD20	AD17	FRAME	DEVSEL
Test Point	**9**	**10**	**11**	**12**	**13**	**14**	**15**	**16**
JP1	STOP	SERR	AD15	AD12	AD9	AD7	AD3	AD1
JP2	LOCK	PAR	AD14	AD11	CBE0	AD6	AD5	AD0
JP3	PERR	CBE1	AD13	AD10	AD8	AD4	AD2	IDSEL

(A copy of this table is present on the right hand side of the component side of the reference board.)
Note: Correction, **JP3-16** should be "**IDSEL**" not "*Ground*"

Test Points Description

These allow convenient sampling of signals by logic analyzer or oscilloscope:

T1 Primary TRST GPIO
T2 Primary TCK GPIO
T3 Primary TMS GPIO
T4 INTA#
T5 Primary TDO GPIO
T6 (not present)
T7 INTB#
T8 Primary **clock input**
T9 INTC#
T10 INTD#
T11 Primary **Reset#**
T12 (not present)
T13 SCAN_EN

TP1 GND
TP2 GND
TP3 GND
TP4 GND
TP5 GND
TP6 GND
TP7 GND
TP8 GND
TP9 GNT to top (4th) slot
TP10 GNT to 3rd slot

TP11 GNT to 2nd slot
TP12 GNT to 1st (bottom) slot
TP13 REQ to top (4th) slot
TP14 REQ to 3rd slot
TP15 REQ to 2nd slot
TP16 REQ to 1st (bottom) slot

OPTIONAL External Arbiter

For **internal** arbiter, **SW2 -6** is **ON** (closed)**.** This is the **default.**
For **external** arbiter, a **CPLD** need to be inserted in socket U5. For use in this mode, please contact Technical Support.

Asynchronous Clock Mode

This layout reference board does not have the external clock buffer and oscillator needed for asynchronous secondary bus clock mode.

Technical Support: http://www.pericom.com/support