PIxxxx
High Speed Layout Guideline

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1 Layout Design Guideline

As transmission data rate increases rapidly, any flaws and/or mis-matches on PCB layout are amplified in terms of signal integrity. Layout guideline for high-speed transmission is highlighted in this application note.

1.1 Power and GROUND

To provide a clean power supply for Pericom high-speed device, few recommendations are listed below:

- ✓ Power (VDD) and ground (GND) pins should be connected to corresponding power planes of the printed circuit board directly.
- ✓ The thickness of the PCB dielectric layer should be minimized such that the VDD and GND planes create low inductance paths.
- ✓ One low-ESR 0.1uF decoupling capacitor should be mounted at each VDD pin or should supply bypassing for at most two VDD pins. Smaller body size capacitors can facilitate component placement. The capacitor should be placed next to the VDD pin.
- ✓ One capacitor with capacitance in the range of 4.7uF to 10uF should be incorporated in the power supply decoupling design as well. It can be either tantalum or an ultra-low ESR ceramic.
- ✓ A ferrite bead for isolating the power supply for Pericom high-speed device from the power supplies for other parts on the printed circuit board should be implemented.

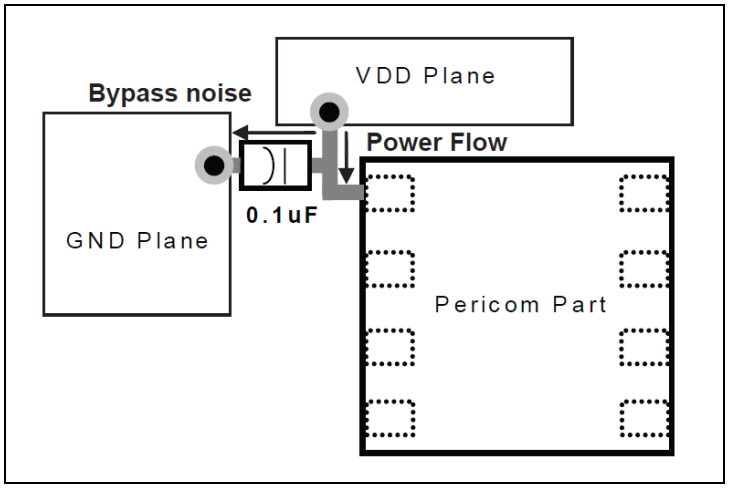

Figure 1: Decoupling Capacitor Placement Diagram

1.2 High-speed Signal Routing

Well-designed layout is essential to prevent signal reflection:

- ✓ Wider trace width of each differential pair is recommended in order to minimize the loss, especially for long routing. More consistent PCB impedance can be achieved by a PCB vendor if trace is wider.
- ✓ For minimal coupling, isolation spacing between two differential pairs should be maximized. At least 3 times the spacing of one differential pair is recommended.
- ✓ Differential signals should be routed away from noise sources and other switching signals on the printed circuit board.
- ✓ It is preferable to route differential signals on the same layer of the printed circuit board, particularly for the input traces of Pericom high-speed device in source application.

✓ Differential pair should maintain symmetrical routing whenever possible. The intra-pair skew should be less than 5 mils.

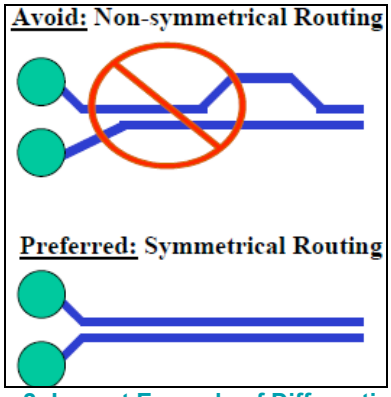

Figure 2: Layout Example of Differential Pair

✓ Stub creation should be avoided when placing shunt resistors on a differential pair.

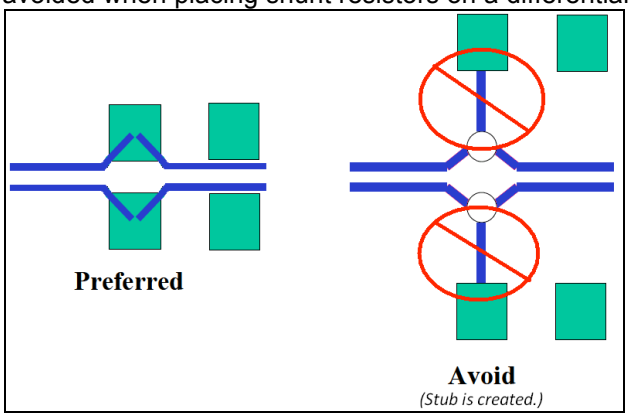

Figure 3: Shunt Resistor Placement

✓ To minimize signal loss and jitter, tight bend is not recommended. All angles should be larger than or equal to 135 degrees.

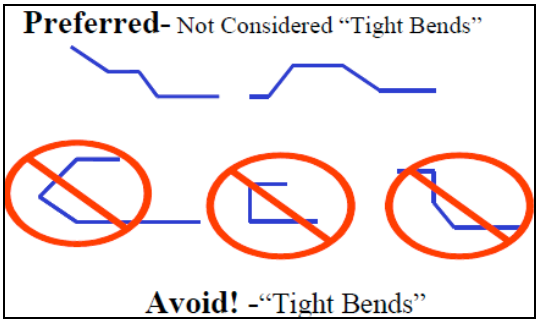

Figure 4: Acceptable Bends vs. Tight Bends

✓ AC coupling capacitor placement should be symmetrical.

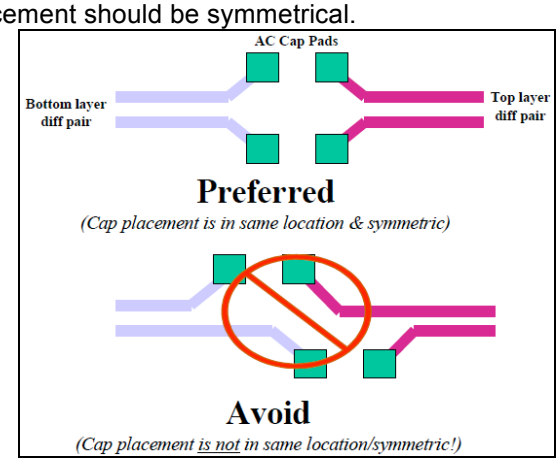

Figure 5: AC Capacitor Placement

✓ The use of vias should be avoided if possible. If using vias is a must, they should be used sparingly and must be placed symmetrically on a differential pair.

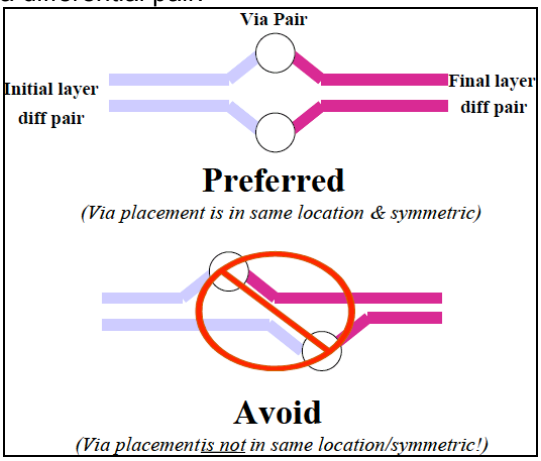

Figure 6: Via Placement

2 Related Reference

(1) PCI Express Board Design Guidelines Draft, Intel Corporation, June 2003
(2) USB3.0 Board Layout Guideline, NEC Electronics Corporation, 2009