AN1174

DGD0579U Application Note

The DIODES™ DGD0579U, High-side/Low-side gate driver with Integrated Bootstrap Diode is used to optimally drive the gate of MOSFETs. Below (Figure 1) is an example application using DGD0579U with MOSFETs to make three Half-bridge circuits used to drive a BLDC motor. The DGD0579U is also well-suited to low voltage power supplies due to its high-speed performance. In this document, the important parameters needed to design in the DGD0579U are discussed. Main sections are bootstrap capacitor selection, gate driver component selection, decoupling capacitor discussion, and PCB layout suggestions.

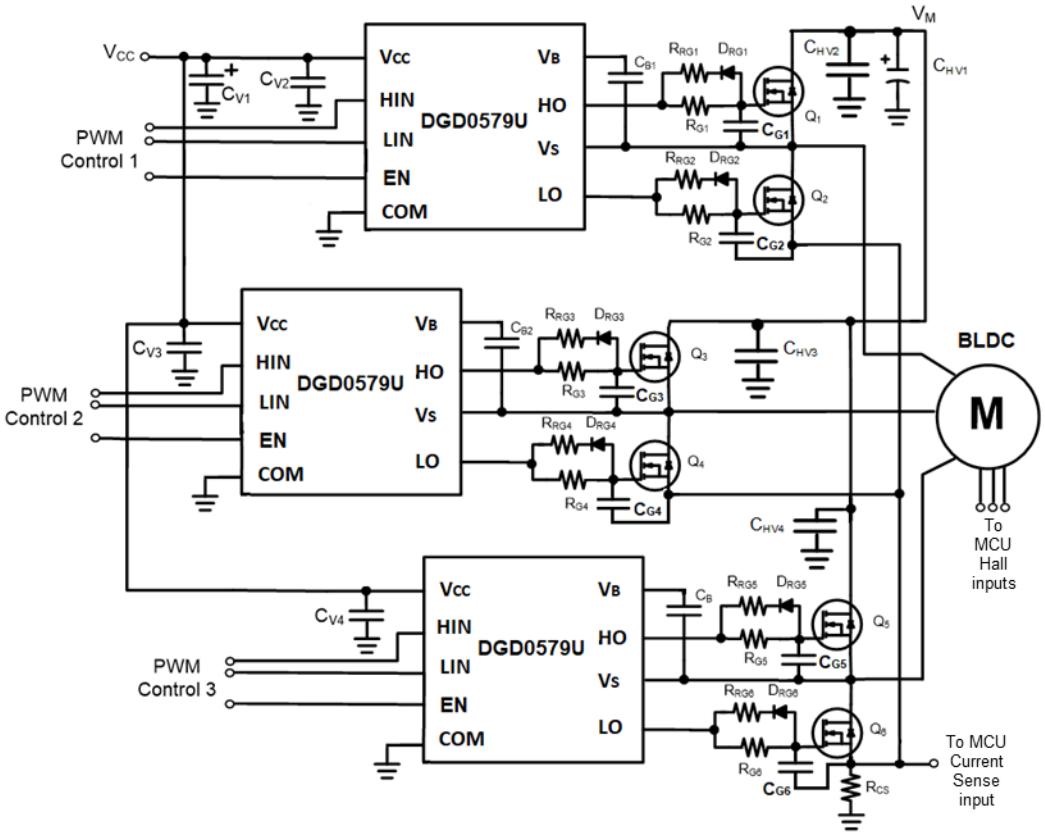

Figure 1. Three Phase Motor Driver application example of DGD0579U

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Bootstrap Component Selection

Considering Figure 1, when the low-side MOSFET (Q2, Q4, or Q6) turns on, Vs pulls to GND and the bootstrap capacitor (C_{B1}, C_{B2}, or C_{B3}) is charged. When the high-side MOSFET (Q1, Q3, or Q5) is turned on, V_S swings above Vcc and the charge on the bootstrap capacitor (C_B) provides current to drive the IC high-side gate driver. The charge of C_B is provided by Vcc through the integrated bootstrap resistor and bootstrap diode, and often the first charge of C_B is at power up will be the largest current through the bootstrap circuit as typically C_B is not fully discharged during each cycle of normal operation.

Bootstrap Capacitor

The initial step in determining the value of the bootstrap capacitor is to determine the minimum voltage drop (ΔV_{BS}) that can be guaranteed when the high-side device is turned on. In other words, the minimum gate-source voltage (V_{GS_min}) must be greater than the UVLO of the high-side circuit, specifically V_{BSUV-} level. Therefore, if V_{GS_min} is the minimum gate-source voltage such that:

$V_{GS\_min} > V_{BSUV-}$

Then:

$\Delta V_{BS} = Vcc - V_f - V_{GS\_min} - V_X$

Where:
- Vcc is the supply voltage to the DGD0579U
- V_f is the voltage drop across the bootstrap diode (D_{BS})
- V_X is the voltage drop across the MOSFET

V_X is calculated as the current seen across low-side MOSFET multiplied by its R_{DS_ON} and is simply V_{CE_ON} at the specific output current if an IGBT were used instead.

In addition to the voltage drops across these components, other factors that cause V_{BS} to drop are leakages, charge required to turn on the power devices, and duration of the high-side on time. The total charge (Q_T) required by the gate driver then equals:

$Q_T = Q_G + Q_{LS} + [I_{LK\_N}] * T_{H\_ON}$

Where:

Q_G = Gate charge of power device
Q_{LS} = Level shift charge required per cycle
T_{H_ON} = High-side on time
I_{LK_N} = Sum of all leakages that include:
- I_{GSS}/I_{GES}: Gate-source leakage of the power device
- I_{LK_DB}: Bootstrap diode leakage
- I_{LK_IC}: Offset supply leakage of Gate Driver
- I_{Q_BS}: Quiescent current for high-side supply
- I_{LK_CB}: Bootstrap capacitor leakage

Bootstrap capacitor leakage (I_{LK_CBS}) only applies to electrolytic types. Therefore, it is best not to use an electrolytic capacitor. Thus, bootstrap capacitor leakages will not be included in the calculations.

Q_{LS} is not listed in the datasheet; for the lower voltage process technology a Q_{LS} of 5nC will be a good approximation and provide a sufficient margin.

From the basic equation, then the minimum bootstrap capacitor is calculated as:

$C_{B\_min} \geq Q_T / \Delta V_{BS}$

Example using MOSFET, DMN6017SK3

Gate Driver = DGD0579U

Vcc = 12V
Q_G = 26nC
I_{GSS} = 100nA
T_{H_ON} = 5µs
R_{DSON} = 25mΩ max, 125˚C
Iout = 10A
I_{Q_BS} = 100µA

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I_{LK_IC} = 1µA
Q_{LS} = 5nC
V_F = 1.0V
I_{LK_DB} = 1µA
V_{GSmin} = 6.0V

From equations:

ΔV_{BS} = 12V- 1.0V-6.0V-(0.25V) = 4.75V

$Q_T = Q_G + Q_{LS} + (I_{LK\_N} * T_{H\_ON})$ where $I_{LK\_N} * T_{H\_ON} = 0.5nC$

= 26nC + 5nC + 0.5nC

= 31.5nC

Thus, C_{BS} min = 31.5nC/4.75V = 6.6nF

The bootstrap capacitor calculated in the above example is the minimal value required to supply the needed charge. It is recommended that a margin of 2-3 times the calculated value be used. Utilizing values lower than this could result in overcharging of the bootstrap capacitor especially during –VS transients.

Typically for high-speed applications like power supplies C_{BS} = 0.1µF to 1µF are used, and for low-speed applications like motor drives C_{BS} = 1µF to 2.2µF are used. It is recommended to use low ESR ceramic capacitors as close to the V_B and V_S pin as possible (see PCB layout suggestions section).

Integrated Bootstrap Diode

The DGD0579U has an integrated bootstrap diode to minimize the system BOM. The data below shows the performance of the integrated diode under DC conditions:

Forward Voltage of Bootstrap Diode	V_{F1}	—	0.6	0.75	V	I_F = 100µA
Forward Voltage of Bootstrap Diode	V_{F2}	—	1.4	1.75	V	I_F = 100mA

The current through the integrated diode is typically the largest during the first charge of C_B. The current waveform, as well as the time to charge C_B is determined by the size of C_B, see Figure 2 & 3.

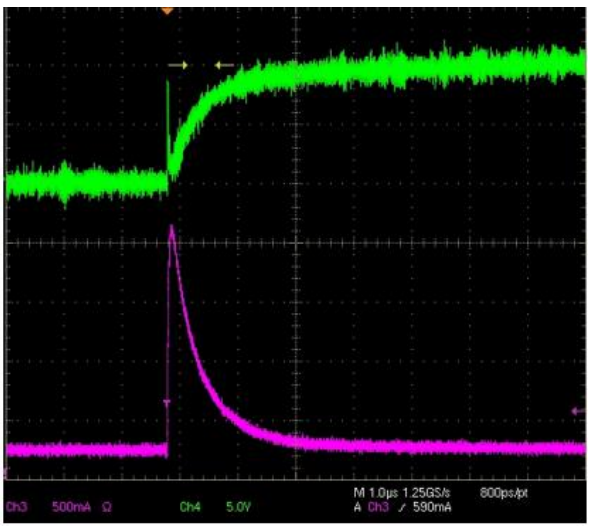

Figure 2. Bootstrap Peak inrush current (Ch3) and VBS (Ch4) with CBS=0.1µF

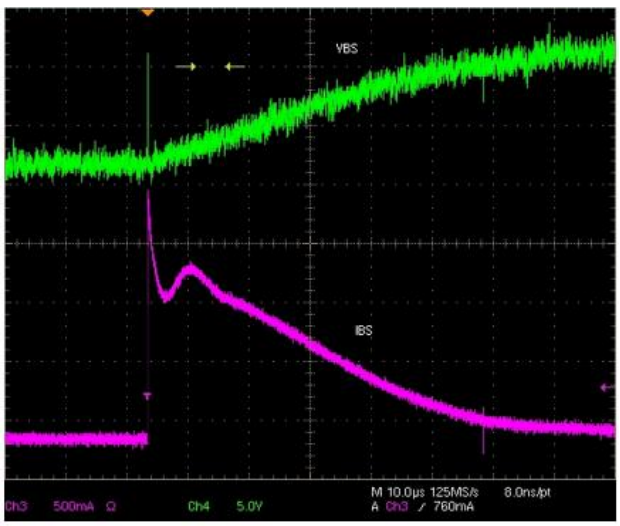

Figure 3. Bootstrap Peak inrush current (Ch3) and VBS (Ch4) with CBS=10µF

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Gate Component Selection

The most crucial time in the gate drive is the turn on and turn off of the MOSFET, and performing this function quickly, but with minimal noise and ringing is key. Too fast a rise/fall time can cause unnecessary ringing and poor EMI, and too slow a rise/fall time will increase switching losses in the MOSFET.

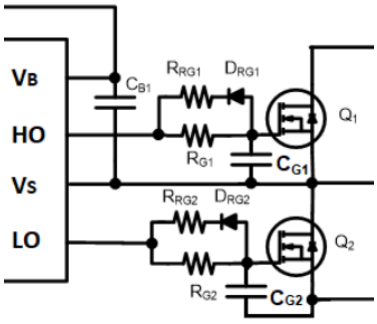

Figure 4. Gate Drive High-Side and Low-Side Components for DGD0579U

Considering the gate driver components for DGD0597U in Figure 4, with the careful selection of R_{Gn} and R_{RGn}, it is possible to selectively control the rise time and fall time of the gate drive to the MOSFET Qn. For turn on, all current will go from the IC through R_{G1} and charge the MOSFET gate capacitance, hence increasing or decreasing R_{Gn} will increase or decrease rise time in the application. With the addition of D_{RGn}, the fall time can be separately controlled as the turn off current flows from the MOSFET gate capacitor, through R_{RGn} and D_{RGn} to the driver in the IC to VS for high-side and COM for low-side. So, increasing or decreasing R_{RGn} will increase or decrease the fall time. Sometimes finer control is not needed and only R_{G1} and R_{G2} is used.

Increasing turn on and turn off has the effect of limiting ringing and noise due to parasitic inductances, hence with a noisy environment, it may be necessary to increase the gate resistors. Gate component selection is a compromise of faster rise time with more ringing, and a poorer EMI but better efficiency, and a slower rise time with better EMI, better noise performance but poorer efficiency. The exact value depends on the parameters of the application and system requirements. R_{Gn} values are typically between 10Ω and 50Ω, with the optimal value determined by MOSFET gate capacitance and the drive current of the Gate Driver. Gate resistor values are increased to decrease system noise, minimise ringing, and hence lower EMI. R_{RGn} values are typically between 5Ω and 20Ω, with the optimal value determined by MOSFET gate capacitance and the drive current of the Gate Driver. The sink current gate resistor can also be increased to decrease system noise, minimise ringing, and hence lower EMI.

To have equal switching times for high-side and low-side, it is recommended that the gate driver components for high-side and low-side are mirrored. For example $R_{RG1} = R_{RG2}$, $D_{RG1} = D_{RG2}$ and $R_{G1} = R_{G2}$.

The gate to source capacitors, C_{G1} and C_{G2}, are used to minimize unexpected shoot-through in the half-bridge. This shoot-through can decrease efficiency or even damage the MOSFETs; this phenomenon is discussed further on page 6.

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Decoupling Capacitor Selection

For optimal operation, Vcc decoupling is crucial for all gate driver ICs. With poor decoupling, larger Vcc transients will occur at the IC when switching, and for greater and longer Vcc drops the IC can go into UVLO.

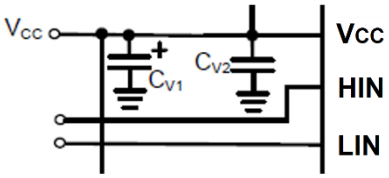

Figure 5. Suggested Vcc decoupling

As shown in Figure 5, two decoupling capacitors are recommended C_{V1} and C_{V2}. C_{V1} can be a larger electrolytic, for example 47µF (50V), and is used to dampen low frequency drains on supply: C_{V1} does not need to be right next to the IC, but C_{V2} is used to decouple faster edge changes to Vcc, and should be a low ESR ceramic capacitor placed close to the Vcc pin. This component provides stability when Vcc is quickly pulled down with load from the IC. Typical values for C_{V2} are 0.1µF to 1µF.

For applications with multiple gate driver ICs (for example BLDC motor drive with 3 x gate drivers as shown in Figure 1), one larger electrolytic (C_{V1}) can be used and the three low ESR ceramic caps (C_{V2}, C_{V3}, C_{V4}) should be used close to the Vcc pin (see Layout section also).

High-Voltage Decoupling Capacitors

Considering the performance of the whole half-bridge, it is important to have appropriate high-voltage decoupling capacitors (see C_{HV1}, C_{HV2} and C_{HV3} in Figure 1). For best stability (best high-frequency performance), C_{HV2} and C_{HV3} are small ceramic capacitors (say 1µF 450V) placed close to the drain of the MOSFETs at the half-bridge (less than 25mm); and C_{HV1} is the electrolytic bulk capacitor which is typically part of the on board power supply. If the small decoupling capacitors (C_{HV2} and C_{HV3}) are not used, then for optimal operation, the bulk capacitor (C_{HV1}) should be close to the drain of the MOSFETs (less than 25mm).

Input Resistors

The DGD0579U PWM inputs, HIN and LIN, are very high-impedance inputs with a pull-down resistor on both inputs to COM (see Figure. 6). The pull-down resistor on HIN and LIN has a value of approximately 1.5MΩ.

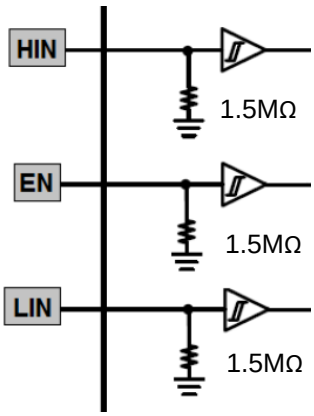

Figure 6. Input Logic for DGD0579U

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Matching Gate Driver with MOSFET or IGBT

IC drive current and MOSFET/IGBT gate charge

Gate Driver ICs are defined by their output drive current, and their ability to source current to the gate of the MOSFET/IGBT at turn on and to sink current from the gate of the MOSFET/IGBT at turn off. For the DGD0579U, the drive current is I_{O+}=1.5A typical and I_{O-}=2.5A typical.

For a given MOSFET/IGBT, with the known drive current of the DGD0579U, you can calculate how long it will take to turn on/off the MOSFET/IGBT with the equation:

t = Qg/I

Qg = total charge of the MOSFET/IGBT as provided by the datasheet
I = sink/source capability of the gate driver IC
t = calculated rise/fall time with the given charge and drive current

For example with the Diodes' DMN6017SK3, 65V 43A, Qg = 55nC; and with the DGD0579U I_{O+}=1.5A and I_{O-}=2.5A, the tr = 37ns and tf = 22ns. These are estimates as the total charge given in the datasheet may not be the same conditions in the application. Also, an addition of a gate resistor will increase the tr and tf.

Unexpected shoot-through with dV_{DS}/d_t

Unwanted MOSFET turn-on, caused by C_{GD} x dV_{DS}/d_t (see Figure 7) is often the cause of unexplained shoot-through in the half-bridge circuit. Depending on the ratio of C_{GS}/ C_{GD} , when the dV_{DS}/d_t across low-side MOSFET (Q2) occurs (i.e when high-side MOSFET turns on), there can be a voltage applied to the gate of the Q2 MOSFET, turning on Q2 and causing shoot-through. In effect, a gate bouncing occurs causing a ringing on the VS line and the power ground.

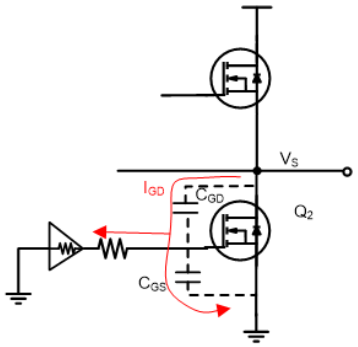

Figure 7. Unexpected shoot through with dV_{DS}/d_t

Considering Figure 7,

I_{GD} = C_{GD} x dV_{DS}/d_t

I_{GD} will flow towards the resistive load (and small inductance due to parasitics) of the gate driver and the C_{GS} of the MOSFET. Hence this unwanted condition may be minimized by looking at the Ciss/Cres in the MOSFET datasheet (Ciss/Cres gives an indication of C_{GS}/C_{GD}); having a Ciss/Cres as large as possible will minimize this phenomenon. Also an external capacitor can be added to the gate-source of the MOSFET (for example 1nF) which will increase C_{GS}/C_{GD}.

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Minimum Pulse Requirement

The DGD0579U has RC filters on the input lines to be more resilient in noisy environments. With a rising edge at the input to the gate driver, followed by the propagation delay of the IC, delay from gate resistor, and rise time of the MOSFET, the half-bridge will then turn on producing bus voltage at the output. This MOSFET turn on produces significant system noise. For optimal operation, it is suggested to provide a minimum pulse width at the input to the IC from the MCU to ensure the turn off occurs after this event. As a rule of thumb, this minimum pulse should be 2 x propagation delay for high-side/low-side gate drivers; hence for the DGD0579U, the minimum pulse recommended at the logic inputs is 140ns.

During typical operation, the DGD0579U will respond to an input greater than 40ns (approximate value from the RC input filter response). Hence, for an input pulse greater than 40ns approximately the IC will follow the pulse as expected; and for an input pulse less than 40ns, there will be no response from the IC.

PCB layout suggestions

Layout plays an important role in minimizing unwanted noise coupling, unpredicted glitches, and abnormal operation which can arise from a poor layout of the associated components. Figure 8 shows a schematic with parasitic inductances in the high-current path (L_{P1}, L_{P2}, L_{P3}, L_{P4}), which would be caused by inductance in the metal of the trace. Considering Figure 8, the length of the tracks in red should be minimized, and the bootstrap capacitor (C_B) and the decoupling capacitor (C_D) should be placed as close to the IC as possible in addition to using low ESR ceramic capacitors. And finally, the gate resistors (R_{GH} and R_{GL}) and the sense resistor (R_S) should be surface mount devices. These suggestions will reduce the parasitics due to the PCB traces.

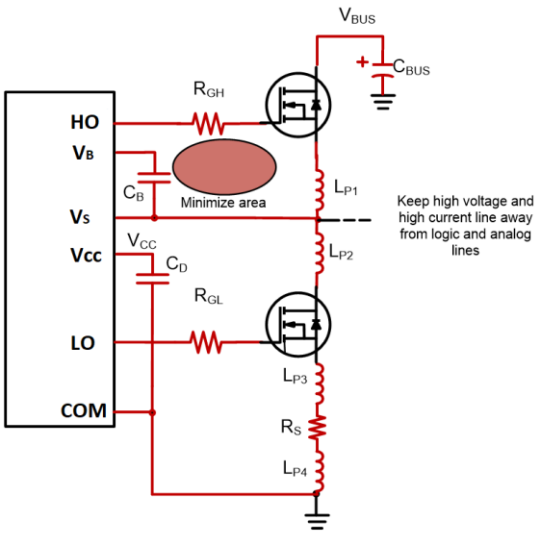

Figure 8. Layout suggestions for DGD0579U in a half-bridge, lines in red should be as short as possible

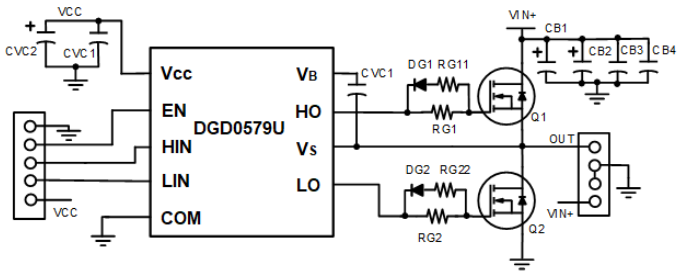

Figure 9. Schematic for layout example in Figure 10

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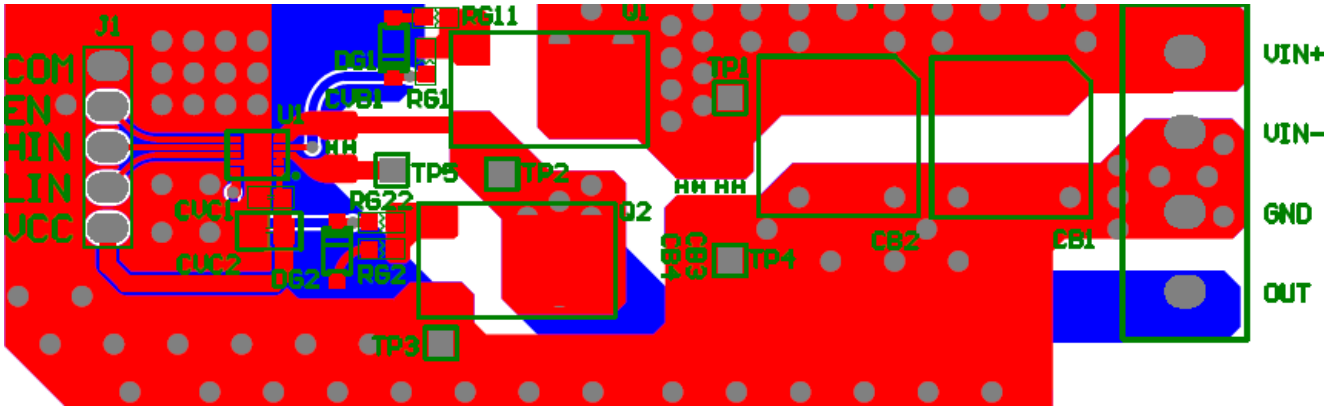

Fig 10. Layout of the schematic shown in Figure 9, DGD0579U in DFN3030-10

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