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Synchronous MOSFETs selection for Flyback converters

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Introduction

A Synchronous rectifier is an essential building block in the secondary side of the Flyback converter for designing efficient power supplies with high power density as motivated by emerging Energy standards. The ZXGD3101 controller when used with an appropriate MOSFET offers a higher efficiency than either a schottky diode or an ultra-fast Silicon rectifier.

However, choosing the optimum Synchronous MOSFET can be difficult if reliant on an experimental trial-and-error method. Instead a straightforward design flow chart can be used to deal with the many device characteristics and controller trade-offs. This design note presents a design procedure that will help to select the best MOSFET for the ZXGD3101 Synchronous rectification controller.

This design note should be used in conjunction with the spreadsheet of ZXGD3101 MOSFET selection tool.

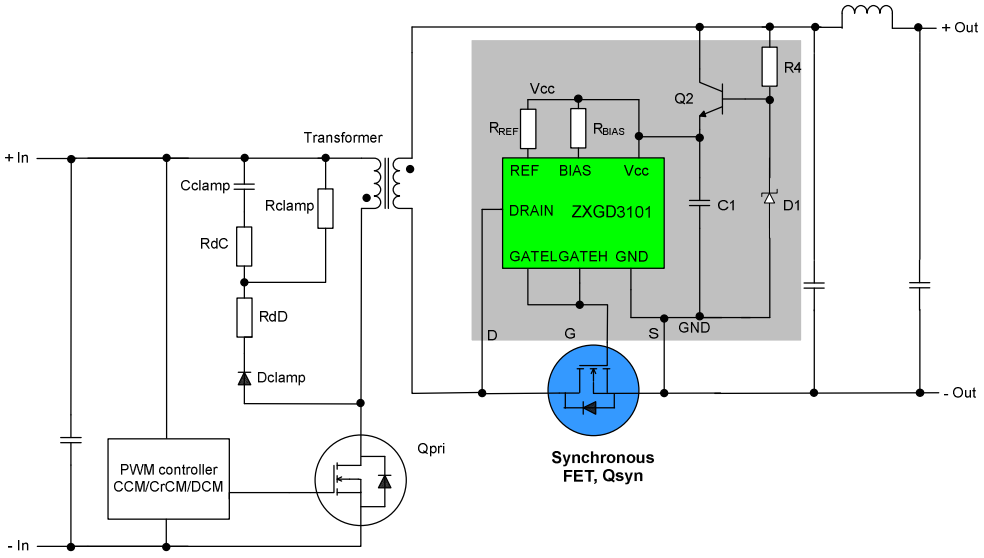


Figure 1 – Flyback converter with Synchronous rectification

Detailed design procedure

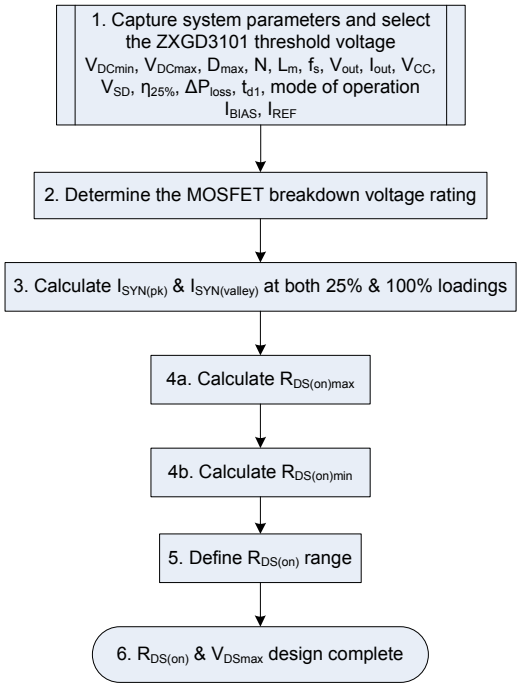


Figure 2 – Design flow chart for Synchronous MOSFET selection

A design methodology is presented below using the circuit diagram of Figure 1 as a reference. Figure 2 illustrates the design flow chart and the detailed procedure is as follows,

Step 1: Capture system parameters and select the ZXGD3101's threshold voltage

The design process starts with collecting the critical design parameters for the Flyback power supply as defined below.

Table 1 - Nomenclature

Symbol of system parameter	Definition
V_{DCmin}	Minimum rectified input voltage across +In and -In
V_{DCmax}	Maximum rectified input voltage across +In and -In
D_{max}	Maximum duty cycle of the primary switch at V_{DCmin} ($0.4 \le D_{max} \le 0.5$)
f_S	Switching frequency of the converter at V_{DCmin}
L_m	Primary magnetizing inductance of the power transformer
N	Primary-to-secondary turn ratio of the power transformer
V_{out}	Output voltage at +Out
I_{out}	Output current flowing from +Out to the load
t_{d1}	Turn on propagation delay time of ZXGD3101 controller
η	Power conversion efficiency
DCM	Discontinuous Conduction Mode
CrCM	Critical Conduction Mode
CCM	Continuous Conduction Mode

Generally, a synchronous rectifier is optimized for high full load efficiency. It is also important to maintain a reasonably high efficiency at low load, particularly for a product which has to meet energy efficiency standards such as Energy Star® V2.0. This design procedure addresses the need to optimize the efficiency at 25% loading to comply with efficiency standard. $\eta_{25\%}$ is the estimation of the power conversion efficiency at 25%. If no reference data is available, set $\eta_{25\%}$=0.8 for low voltage output applications (<6V) and $\eta_{25\%}$=0.83 for high voltage output applications (≥6V) as the initial assumptions.

The duty cycle of the primary side switch at 25% loading is,

$$D_{25\%load} = \frac{\sqrt{2 \times L_m \times f_s \times V_{out} \times I_{out}}}{\sqrt{\eta_{25\%}} \times V_{DCmin}}$$

The duty cycle is used later in the analysis to determine the peak Drain current at a partial load condition.

However, the maximum duty cycle is found at the minimum input voltage and full load as,

$$D_{max} = \frac{\sqrt{2 \times L_m \times f_s \times V_{out} \times I_{out}}}{\sqrt{\eta} \times V_{DCmin}} \quad \text{for DCM}$$

$$D_{max} = \frac{N \times V_{out}}{V_{DCmin} + N \times V_{out}} \quad \text{for CrCM/CCM}$$

where η should be set at 0.84 and 0.87 with a synchronous rectifier for V_{out}<6V and V_{out}≥6V respectively if no reference data is available.

Figure 3 shows the recommended I_{REF} and I_{BIAS} combinations for different operation modes, namely Continuous Conduction Mode (CCM) and Discontinuous Conduction Mode (DCM). The turn-off threshold voltage of the controller should be set at '-20mV' for CCM so that the MOSFET can be gated off sooner to minimize the possibility of simultaneous conduction of MOSFETs. The '-20mV' threshold value is set by selecting an appropriate resistor pair to source 5mA and 3mA into the BIAS and REF pins respectively, as shown in Figure 3. For example if the V_{CC} supply voltage to the controller is chosen to be 10V, resistors R_{BIAS} of 1.8kΩ and R_{REF} of 3kΩ should be used to achieve the desired threshold voltage.

An alternative turn-off threshold is '-10mV' which is only recommended for both DCM and CrCM where a higher secondary peak Drain current circulates, in order to ensure the sustained enhancement of a low resistance MOSFET. Again, this threshold is developed based on the combination for R_{BIAS} of 1.8kΩ and R_{REF} of 3.9kΩ to source 5mA and 2.4mA into the BIAS and REF pins respectively, as shown in Figure 3.

It is worth noting that a greater I_{BIAS} is required to achieve shorter turn on propagation delay and gate rise times while a greater I_{REF} speeds up the turn-off switching. However, if these two currents are getting too high, both no load and light load efficiencies will be degraded. Moreover, with reference to Figure 5, if either I_{BIAS} is getting too high or I_{REF} is getting too low, the zero point detected offset will become slightly positive to allow current flow in the reverse direction which could actively discharge the output capacitor in DCM or cause shoot through in CCM. Consequently, I_{BIAS} of 5mA has been compromised for all the operation modes.

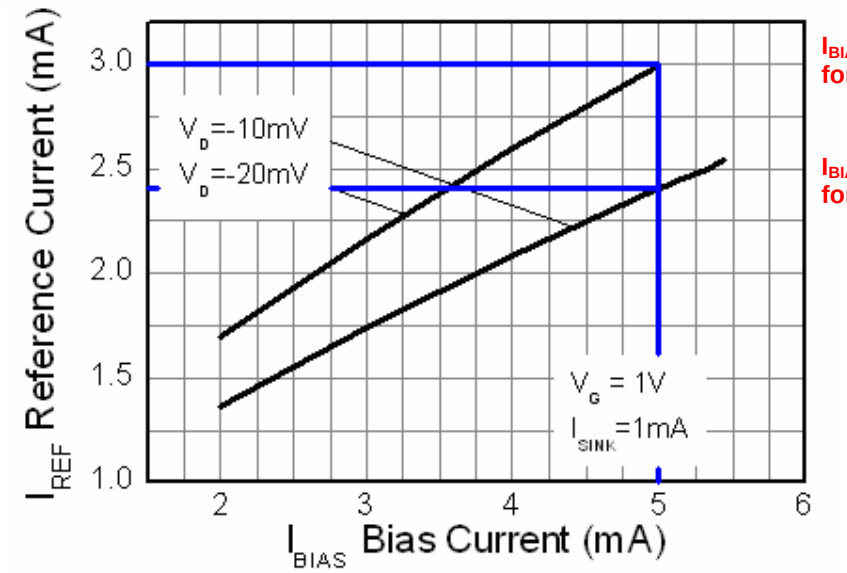


Figure 3 – Optimal I_{BIAS} and I_{REF} combinations at two turn off threshold voltages (-10mV & -20mV)

Step 2: Determine the MOSFET breakdown voltage rating

The MOSFET maximum reverse voltage with a safety design margin is determined as follows, where the margin is typically 20%~40%. 30% is taken generally,

$$V_{DSmax} = 1.3 \times \left[V_{out} + \frac{V_{DCmax} \times V_{out} \times (1 - D_{max})}{V_{DCmin} \times D_{max}} \right]$$

Step 3: Calculate $I_{SYN(pk)}$ and $I_{SYN(valley)}$ at 25% and 100% loadings

This section determines the magnitude of the current flowing through the Synchronous rectifier to establish the MOSFET's on-resistance requirement. However, as the input voltage and load condition vary, the converter's operation mode can switch between CCM and DCM, and the current magnitude changes as well.

Once the operation mode is determined, its respective maximum peak Drain current of the Synchronous MOSFET $I_{SYN(pk)}$ (see Figure 4) is obtained as,

$$I_{SYN(pk)} = \frac{2 \times N \times V_{out} \times I_{out}}{\eta \times V_{DCmin} \times D_{max}} \quad \text{for DCM}$$

$$I_{SYN(pk)} = \frac{2 \times I_{out}}{1 - D_{max}} \quad \text{for CrCM}$$

$$I_{SYN(pk)} = \frac{I_{out}}{1 - D_{max}} + \frac{V_{out} \times \left(\frac{1 - D_{max}}{f_s} \right)}{\frac{2L_m}{N^2}} \quad \text{for CCM}$$

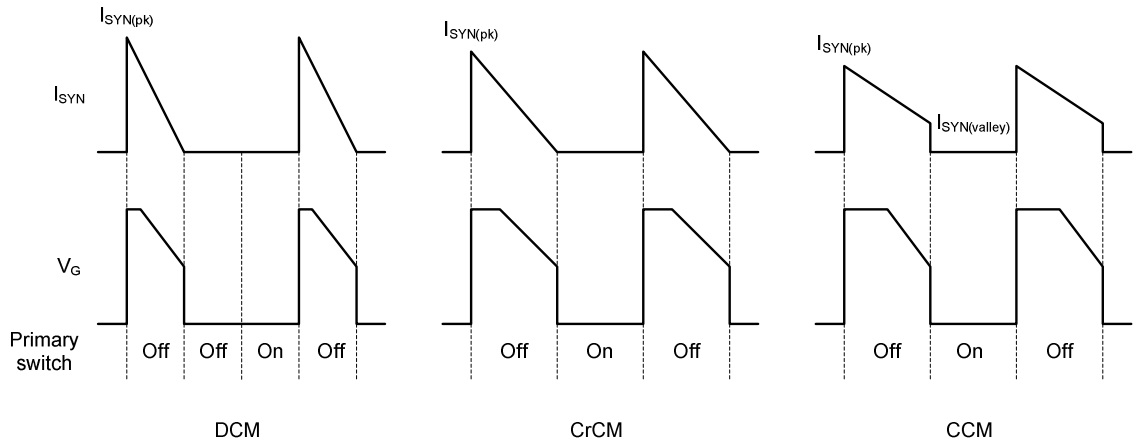


Figure 4 – MOSFET Drain current and mode of operation

And the valley Drain current of the MOSFET in Figure 4 is,

$$I_{SYN(valley)} = 0 \qquad \text{for DCM/CrCM}$$

$$I_{SYN(valley)} = \frac{I_{out}}{1-D_{max}} - \frac{V_{out} \times \left(\frac{1-D_{max}}{f_s}\right)}{\frac{2L_m}{N^2}} \qquad \text{for CCM}$$

When the output current drops from full load to 25% load that is 0.8A; the converter transverses from CrCM to DCM, and the Drain current peak decreases as,

$$I_{SYN(pk)@25\%load} = \frac{2 \times N \times V_{out} \times I_{out} \times 0.25}{\eta \times V_{DCmin} \times D_{25\%load}}$$

Step 4a: Calculate the maximum MOSFET on-resistance rating

The Synchronous rectifier will be required to achieve a power loss reduction of ΔP_{loss}, where ΔP_{loss} is typically greater than 50%. The typical forward voltage drop V_F of a 150V diode at elevated temperature of 100℃ is around 800mV.

For a given power loss reduction ΔP_{loss} dissipated in the secondary side switch, the required MOSFET on-state resistance at full load has to be,

$$R_{DS(on)@Tj=100℃} \le \frac{\frac{(100-\Delta P_{loss})}{100} \times I_{out} \times V_F - I_{SYN(pk)} \times V_{SD} \times t_{d1} \times f_s}{\left[I_{SYN(pk)} - \frac{N \times V_{DCmin} \times D_{max} \times t_{d1}}{L_m \times (1-D_{max})}\right]^2 \times \left[\frac{\left(\frac{L_m \times I_{SYN(pk)}}{N^2 \times V_{out}} - t_{d1}\right) \times f_s}{3}\right]} \qquad \text{for DCM}$$

$$R_{DS(on)@Tj=100℃} \le \frac{\frac{(100 - \Delta P_{loss})}{100} \times I_{out} \times V_F - I_{SYN(pk)} \times V_{SD} \times t_{d1} \times f_s}{\left(\frac{1 - D_{max} - t_{d1} \times f_s}{3}\right) \times \left\{\left[I_{SYN(pk)} - \frac{N \times V_{DCmin} \times D_{max} \times t_{d1}}{L_m \times (1 - D_{max})}\right]^2 + I_{SYN(valley)}^2 + \left[I_{SYN(pk)} - \frac{N \times V_{DCmin} \times D_{max} \times t_{d1}}{L_m \times (1 - D_{max})}\right] \times I_{SYN(valley)}\right\}} \quad \text{for CrCM/CCM}$$

The loss within the propagation delay time of the ZXGD3101, t_{d1}, associated with the forward voltage drop across the intrinsic body diode of the Synchronous MOSFET, V_{SD}, has been included in the above analysis.

The corresponding MOSFET on-state resistance at room temperature is deduced as,

$$R_{DS(on)@Tj=25℃} = \frac{1}{1.75} \times R_{DS(on)@Tj=100°C}$$

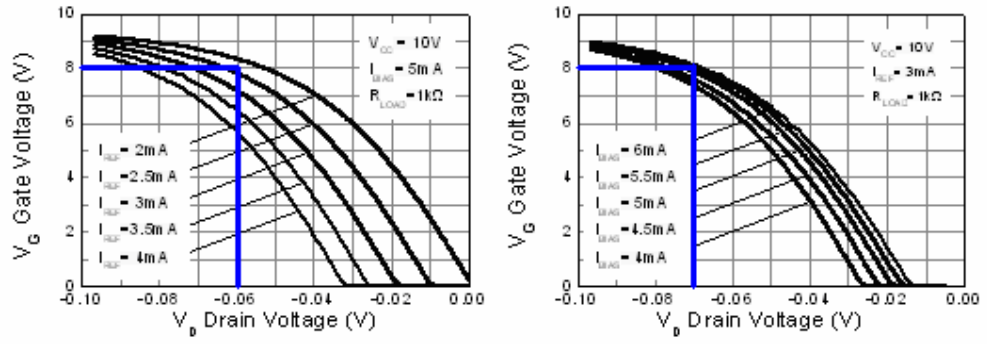
Step 4b: Calculate the minimum MOSFET on-resistance rating

The ZXGD3101 controller features a proportional Gate drive output which adjusts the magnitude of the Gate voltage as the Drain-Source voltage across the MOSFET varies as shown in Figure 5. This ensures that the Gate voltage will reach 8.5V when the MOSFET current was high to create the low resistance path at normal loading. The Gate enhancement then eases off gradually as the Drain voltage magnitude decreases, so that the Synchronous MOSFET can be turned off with reduced Gate charge at zero current crossing.

However, inadequate MOSFET enhancement could result at low load condition with the proportional Gate drive if a MOSFET with too low on-resistance is selected. This effect would be caused as the Drain current decreases at partial loading. The Drain-Source voltage drop, which is the current multiplied by the resistance of the MOSFET, might be insufficient to induce the controller to output a high enough Gate voltage. Therefore, the full capability of the MOSFET is not utilized and the additional resistive loss reduces the efficiency of the Synchronous rectifier.

In general, MOSFETs are fully enhanced beyond the Gate voltage of 8V. Using the V_D against V_G relationship in Figure 5, the minimum MOSFET resistance that can be used without compromising the power supply efficiency at 25% loading is determined from,

$$R_{DS(on)@Tj=25℃} \ge \frac{|V_D(V_G = 8V)|}{I_{SYN(pk)@25\%\,load}} = \begin{cases} \dfrac{0.06V}{I_{SYN(pk)@25\%\,load}} & \text{for DCM/CrCM} \\ \dfrac{0.07V}{I_{SYN(pk)@25\%\,load}} & \text{for CCM} \end{cases}$$



V_D=-0.06V for DCM/CrCM at -10mV

V_D=-0.07V for CCM at -20mV

Figure 5 – Minimum $|V_D|$ for full enhancement of Synchronous MOSFET with DCM/CrCM/CCM

Design example

The following example makes use of the design procedure to select the Synchronous MOSFET for an experimental Flyback converter with the parameters listed in Table 2. All the equations below are put into the spreadsheet in Figure 6 as a user-defined design tool.

Step 1: Capture the system parameters and select threshold voltage

Table 2 – System specification

System and ZXGD3101 controller parameters									
V_{DCmin}	V_{DCmax}	N	L_m	f_S	V_{out}	I_{out}	Operation mode	V_{CC}	t_{d1}
110V	375V	1:0.18	560µH	60kHz	19V	3.2A	CrCM	10V	525ns

The threshold voltage of the ZXGD3101 is selected to be '-10mV'. With the V_{CC} supply voltage to the controller fixed at 10V, a 1.8kΩ and 3.9kΩ resistor combination is used for R_{BIAS} and R_{REF} to set the desired threshold voltage. The Synchronous MOSFET is required to reduce the power loss by ΔP_{loss}=50% to facilitate a smaller heat sinking component. And the duty cycles at 25% and 100% loadings are,

$$D_{25\%load} = \frac{\sqrt{2\times 560\mu H\times 60kHz\times 19V\times 0.8}}{\sqrt{0.83}\times 110V} = 0.3189 \quad \text{assuming } \eta_{25\%}=0.83$$

$$D_{max} = \frac{5.6\times 19V}{110V + 5.6\times 19V} = 0.4917$$

Step 2: Determine the MOSFET breakdown voltage rating

$$V_{DSmax} = 1.3\times\left[19V + \frac{375V\times 19V\times(1-0.4917)}{110V\times 0.4917}\right] = 111.7V$$

Hence, a common 150V MOSFET is chosen.

Step 3: Calculate $I_{SYN(pk)}$ and $I_{SYN(valley)}$ at 25% and 100% loadings

$$I_{SYN(pk)} = \frac{2\times 3.2A}{1-0.4917} = 12.59A$$

$$I_{SYN(pk)@25\%load} = \frac{2\times 5.6\times 19V\times 0.8A}{0.83\times 110V\times 0.3189} = 5.847A$$

Step 4a: Calculate the maximum MOSFET on-resistance rating

From above, ΔP_{loss}=50% and the maximum allowable MOSFET resistance value is,

$$R_{DS(on)@Tj=25℃} \le \frac{1}{1.75}\times\frac{\frac{1}{2}\times 3.2A\times 0.8V - \frac{2\times 3.2A}{1-0.4917}\times 1.25V\times 525ns\times 60kHz}{\left[\frac{1}{1-0.4917}\times\left(2\times 3.2A - \frac{5.6\times 110V\times 0.4917\times 525ns}{560\mu H}\right)\right]^2\times\left(\frac{1-0.4917-525ns\times 60kHz}{3}\right)} = 19.47m\Omega$$

Step 4b: Calculate the minimum MOSFET on-resistance rating

$$R_{DS(on)@Tj=25℃} \ge \frac{0.06V}{5.847A} = 10.26m\Omega$$

Step 5: Define $R_{DS(on)}$ range

As a result, the $R_{DS(on)}$ range is established by combining the two constraints in Steps 4a & 4b as follows,

$$10.26m\Omega \le R_{DS(on)@Tj=25℃} \le 19.47m\Omega$$

In this example, a 150V, 79A, 16mΩ MOSFET–FDP2532 will satisfy the requirement.

	A	B	C	D	E	F
1					ZXGD3101/3 MOSFET selection tool issue 1	
2						
3					Used in conjunction with AN68	
4						
5		Input		Units	Description	
6		Enter converter variables				
7		V_{DCmin}	110	V	Minimum rectified input voltage	
8		V_{DCmax}	375	V	Maximum rectified input voltage	
9		f_s	60	kHz	Switching frequency of the converter at V_{DCmin} and full load	
10		V_{out}	19	V	Output voltage	
11		I_{out}	3.2	A	Output current	
12		$\eta_{25\%load}$	0.83		Expected efficiency at 25% load with ZXGD3101	
13		η	0.87		Expected efficiency at full load with ZXGD3101	
14		ΔP_{loss}	50	%	Desired power loss reduction in the rectifier (≈50%)	
15		Operation mode	CrCM		Operation mode at V_{DCmin} and full load	
16						
17		Enter ZXGD3101 variables		Units	Description	
18		t_{d1}	525	ns	Turn on propagation delay time	
19					ZXGD3101: 525ns; ZXGD3103: 150ns	
20						
21		Enter power transformer variables		Units	Description	
22		L_m	560	µH	Primary magnetizing inductance	
23		N	5.6		Primary-to-secondary turn ratio	
24						
25		Output		Units	Description	
26		Calculated parameters				
27		I_{BIAS}	5.0	mA	Current sourcing into the BIAS pin	
28		I_{REF}	2.4	mA	Current sourcing into the REF pin	
29		$D_{25\%LOAD}$	0.3189		Duty cycle at 25% load	
30		D_{max}	0.4917		Maximum duty cycle	
31		V_{DSmax}	111.8	V	Synchronous MOSFET maximum drain-source voltage	
32		I_{SYNCpk}	12.59	A	Synchronous MOSFET peak drain current	
33		$I_{SYNCvalley}$	0.000	A	Synchronous MOSFET valley drain current	
34		$I_{SYNCpk@25\%load}$	5.847	A	Synchronous MOSFET peak drain current at 25% load	
35		$R_{DS(on)max@Tj-125°C}$	34.08	mΩ	Maximum MOSFET on-resistance at elevated temperature	
36		$R_{DS(on)min@Tj-25°C}$	10.26	mΩ	Minimum MOSFET on-resistance at room temperature	
37						
38		Choose a MOSFET with the following parameters		Units	Description	
39		BV_{DS}	150.0	V	Breakdown voltage rating	
40		$R_{DS(on)@Tj-25°C}$	15	mΩ	On-resistance at V_{GS}=10V and room temperature	
41						
42		Configure ZXGD3101 with the following parameters		Units	Description	
43		V_{CC}	10.0	V	Supply voltage for ZXGD3101	
44		R_{BIAS}	1.9	kΩ	Bias resistance	
45		R_{REF}	3.3	kΩ	REF resistance	

Figure 6 – Spreadsheet for Synchronous MOSFET design

Conclusion

With the new energy saving standards launched out by the EPA, European Code of Conduct and the increasing adoption of the Energy Star V2.0 standard enforced for external power adaptor, the design of the power supply is no longer trivial but it can be a very tough challenge for many power supply designers using only the traditional Schottky technology. Combining both benefits of optimized MOSFET enhancement and fast turn off speed, the ZXGD3101 controller can be used by power supply designers as one of their tools to meet the emerging stringent efficiency requirements. This design procedure for the Synchronous MOSFET selection takes into consideration many critical system parameters, which aids the optimum selection of a low on-resistance MOSFET to be used with the ZXGD3101 controller reducing the need for experimentation. The procedure will be helpful to optimize the PSU performance for both full power and low load condition.

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