# Design Consideration with AP3039A

Prepared by Shanshan Yuan

System Engineering Dept.

## 1. Introduction

AP3039A is a current mode high voltage low-side N-channel MOSFET controller which is ideal for boost regulators. It contains all the features needed to implement single ended primary topology DC/DC converters.

The input voltage range of AP3039A is from 5V to 27V Its operation frequency is adjustable from 150kHz to 1MHz.

The AP3039A has UVLO (Under Voltage Lock Out) circuit. It uses two external resistors to set the UVLO voltage. The AP3039A also has an over output voltage protection to limit the output voltage. The OVP voltage can be set through external resistors. If the output voltage is higher than the OVP high threshold point, it will disable the driver, when the output voltage drops to the OVP low threshold point, it will enable the driver. It also features a soft start to reduce the inrush current when power on, the soft start time can be set through an external capacitor.

## 2. Functional Block Description

The pin configuration and the representative block diagram of the AP3039A are respectively shown in Figure 1 and Figure 2.

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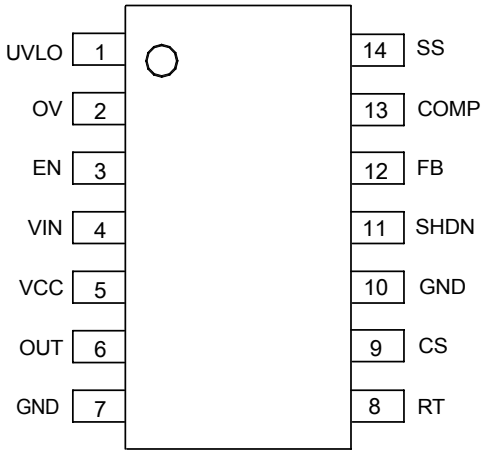


Figure 1. Pin Configuration of AP3039A (Top View)

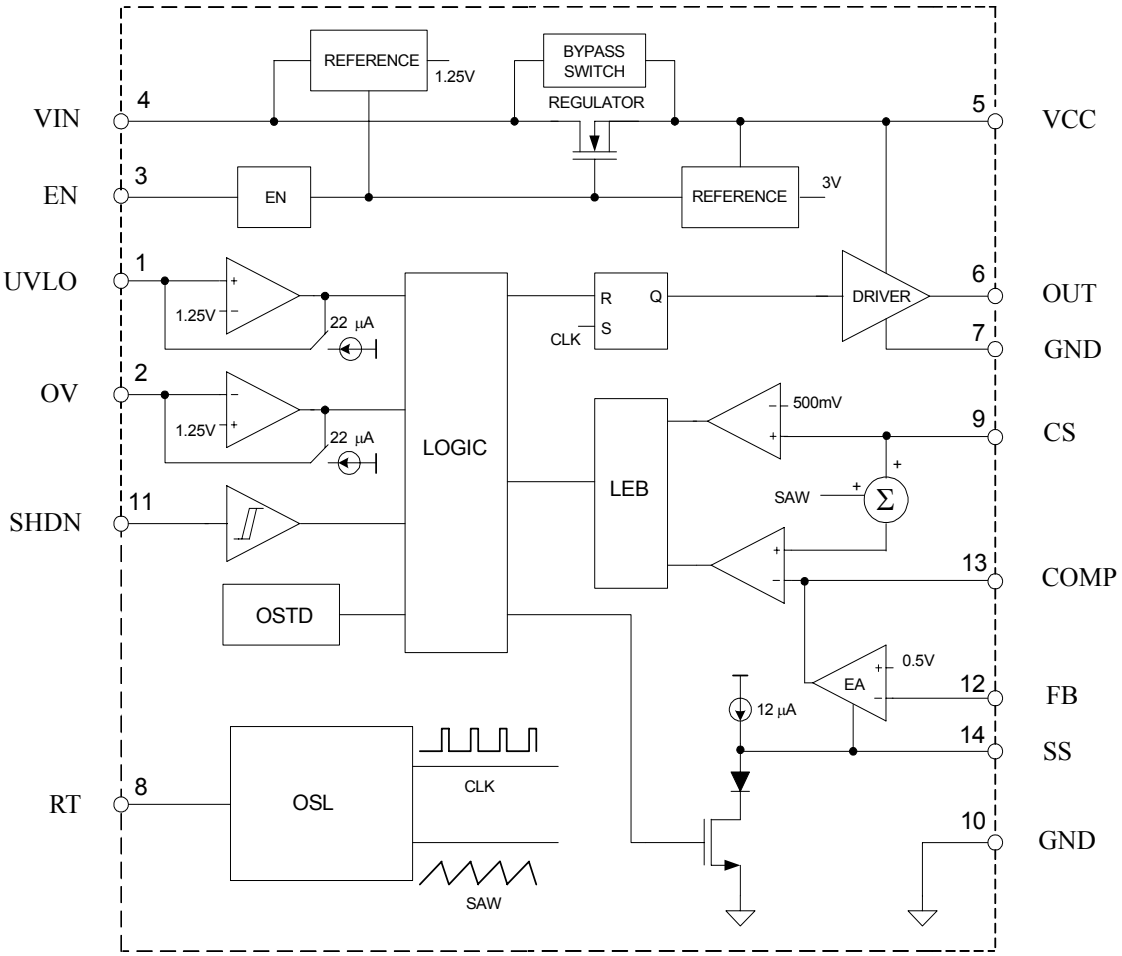


Figure 2. Functional Block Diagram of AP3039A

## 3. Operation

AP3039A is a boost DC-DC controller with adjustable operation frequency. Current mode control scheme provides excellent line and load regulation. Operation can be best understood by referring to the Figure 2.

At the start of each oscillator cycle, the SR latch is set and external power switch Q1 (refer to Figure 3) turns on. The switch current will increase linearly. The voltage on external sense resistor $R_{CS}$ (refer to Figure 3), which connected from CS pin to GND, is proportional to the switch current. This voltage is added to a stabilizing ramp and the result is fed into the non-inversion input of the PWM comparator. When this non-inversion input voltage exceeds inversion input voltage of PWM comparator, which is the output voltage level of the error amplifier EA, the SR latch is reset and the external power switch turns off.

It is clear that the voltage level at inversion input of PWM comparator sets the peak current level to keep the output in regulation. The output voltage level is the amplified signal of the voltage difference between feedback voltage and reference voltage of 0.5V. So, a constant output current can be provided by this operation mode.

## 4. Typical Application

In Figure 3, input capacitor $C_{IN}$, output capacitor $C_{OUT,}$ inductor L, switch Q1 and diode D1 build a typical boost converter. The output voltage is decided by R5, R6 and internal 0.5V reference. The output voltage accuracy is determined by the accuracy of R5 and R6, for which the precise resistors are preferred. (The external function will be introduced in Section 6 Application Hints)

$$V_{OUT}= \frac{0.5V}{R6} * (R5 + R6)$$

Figure 4 is the application of driving a single 1W or 3W LED lighting. In this application, the LED current is controlled by the feedback resistor R5. LEDs current accuracy is determined by regulator's feedback threshold accuracy and is independent of the LEDs' forward voltage variation. So the precise resistors are the better choices. The resistance of R5 is in inverse proportion to the LED current since the feedback reference is fixed at 0.5V. The relation of R5 and the LED current can be expressed as below:

$$R5= \frac{0.5V}{I_{LED}}$$

Figure 5 is the application circuit of backlight driver. The summation of LED current is determined by R5 and internal 0.5V reference same as the illustration in Figure 4.

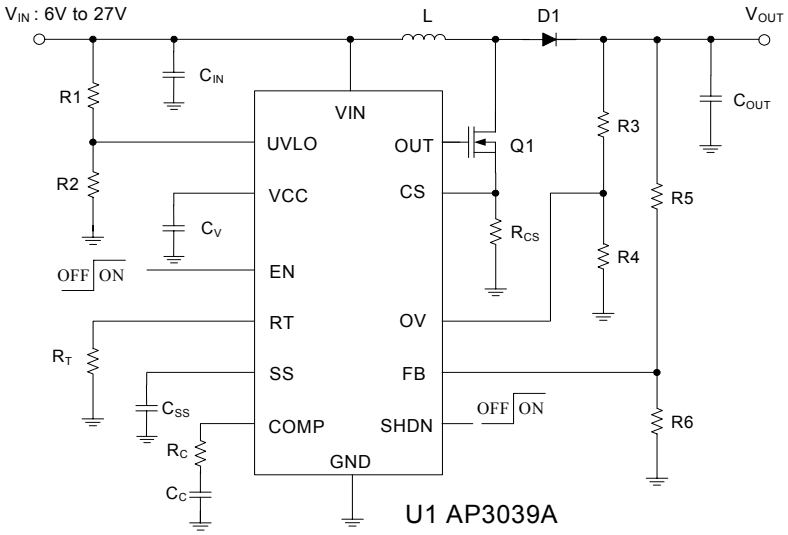


Figure 3. AP3039A Application Circuit

## 4. Typical Application (Continued)

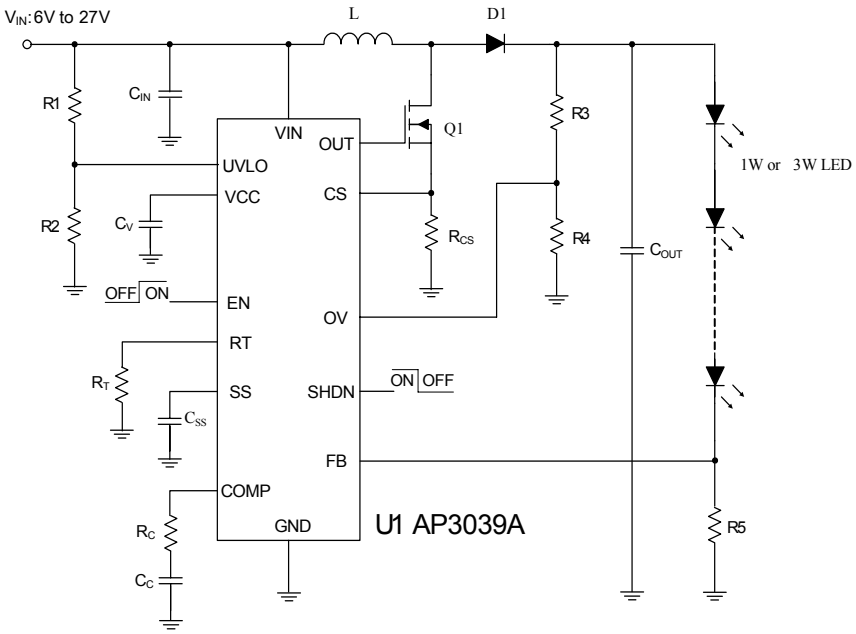


Figure 4. Application Circuit 2 of AP3039A (Driving Single 1W or 3W LED Lighting)

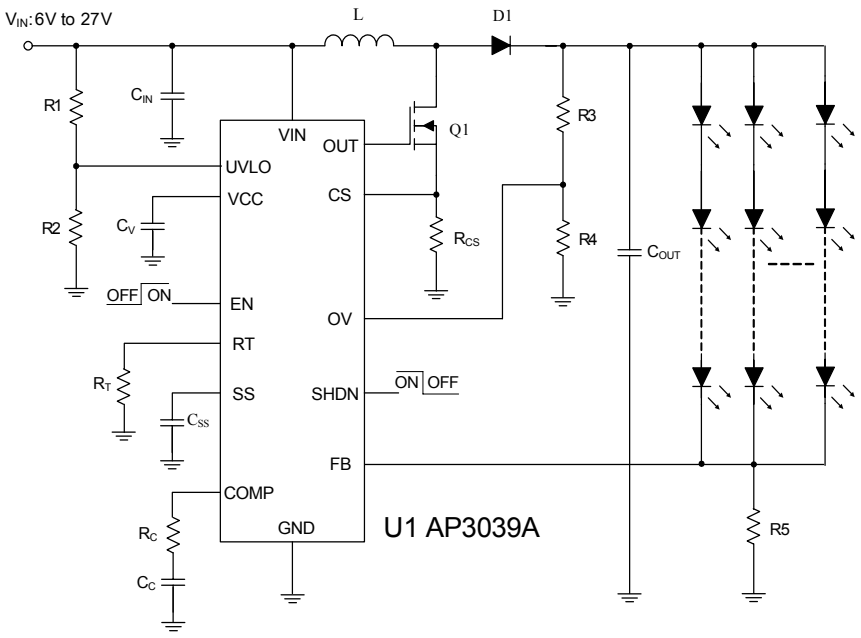


Figure 5. Application Circuit 3 of AP3039A (Backlight Driver)

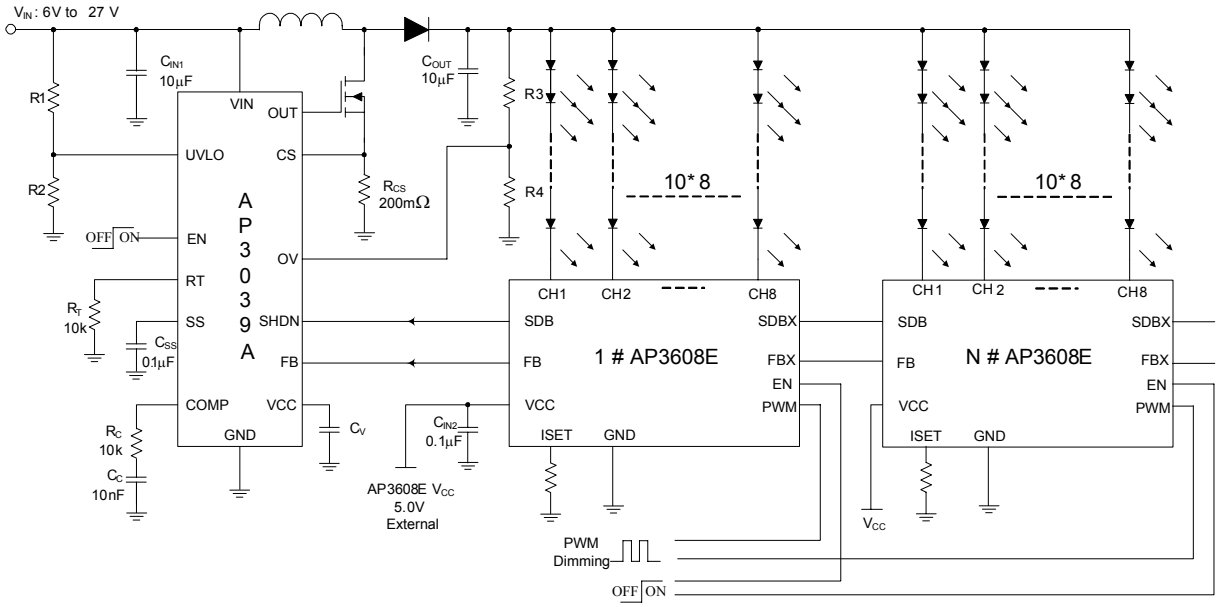


Figure 6. AP3039A + AP3608E (Eight Channels Current Sink) Application Circuit

Another application of AP3039A is introduced in Figure 6.

The application circuit in Figure 6 is AP3039A works with AP3608E to drive LED array. The AP3608E acts as an eight-channel constant current sink with current match to drive the LEDs.

The FB, FBX, SDB and SDBX pins of AP3608E are the interface terminals to coordinate with the AP3039A. The FB/FBX pin of AP3608E samples voltage of each channel, and outputs the lowest voltage of all the strings to AP3039A.

When there is a shutdown signal on EN pin of AP3608E or all LED channels are inactive, the SDB/SDBX pin of AP3608E outputs a low logic signal to turn off AP3039A.

If AP3608E is on PWM dimming mode, the SDB/SDBX pin of AP3608E outputs a signal to AP3039A, which is synchronous with PWM.

## 5. Components selection

### Inductor Selection

When choosing an inductor, the first step is to determine the operating mode: continuous conduction mode (CCM) or discontinuous conduction mode (DCM). When CCM mode is chosen, the ripple current and the peak current of the inductor can be minimized. If a small-size inductor is required, DCM mode can be chosen. In DCM mode, the inductor ripple current and peak current are higher than those in CCM.

When the value of inductor is less than $L_{CCM(MIN)}$, the system operates in DCM mode.

$$L_{CCM(MIN)} = \left(\frac{V_{IN}}{V_{OUT}}\right)^2 \left(\frac{V_{OUT} - V_{IN}}{I_{OUT} * f_{OSC}}\right) * \frac{\eta}{2}$$

The expected efficiency (η) is taken from an appropriate curve in datasheet.

**Current Resistor Selection**

An external resistor $R_{CS}$ is connected from CS pin to GND to detect switch current signal for current-mode boost converter. The current-limit threshold voltage VCS of AP3039A is fixed at 500mV. The required resistance of $R_{CS}$ is based on the peak inductor current at the end of the switch on-time, and can be calculated by the following equations:

$$R_{CS\_MAX} < \frac{VC_S}{\frac{\Delta I_L}{2} + I_{IN}}$$ in which,

$$\Delta I_L = \frac{(V_{OUT} - V_{IN}) * V_{IN}}{L * f_{OSC} * V_{OUT}}$$

$$P_{RCS} = I_{RMS-ON}{}^2 * R_{CS}$$ in which,

$$I_{RMS\_ON}{}^2 = \frac{V_{OUT} - V_{IN}}{V_{OUT}} * \left( I_{IN}{}^2 + \frac{\Delta I_L{}^2}{12} \right)$$

**Output Capacitor Selection**

The output capacitor of the boost converter is used for output filtering and keeping the loop stable. The ESR value is the most important parameter of the $C_{OUT}$, because it directly affects the system stability and the output ripple voltage.

The total output ripple can be calculated by the following the equations:

$$\Delta Vo = \Delta V_{O(CO)} + \Delta V_{O(ESR)}$$

$$\Delta V_{O(CO)} = \frac{I_{OUT}}{C_O} * \left( \frac{V_{OUT} - V_{IN}}{V_{OUT} * f_{OSC}} \right)$$

$$\Delta V_{O(ESR)} = I_{L-PEAK} * R_{ESR(CO)}$$

The small size and high temperature rating of ceramic capacitors is a good choice.

**Input Capacitor Selection**

The input capacitor ($C_{IN}$) of AP3039A filters the current peaks drawn from the input supply and reduces noise injection into the IC. A 10μF ceramic capacitor (or two 4.7μF ceramic capacitors in parallel) is recommended in the typical application.

**VCC Decoupling Capacitor Selection**

The VCC pin of AP3039A should be decoupled with a ceramic capacitor placed as close to the AP3039A as possible. This capacitor keeps VCC voltage steady when the system operates at a high frequency. The decoupling capacitor should adopt X5R or X7R ceramic capacitor because of their good thermal stability, and the capacitance of 0.47μF is recommended.

**Power MOSFET Selection**

When selecting the power MOSFET Q, some tradeoffs between cost, size, and efficiency should be made. The losses in the MOSFET can be calculated by:

$$P_{MOS} = P_{CONDUCTION} + P_G + P_{SW}$$

Where $P_{CONDUCTION}$ is conduction loss, $P_G$ is Gate charging loss, and $P_{SW}$ is switching loss.

$$P_{CONDUCTION} = K_{TH} * I_{RMS\_ON}{}^2 * R_{DSON}$$

Where $K_{TH}$ is the factor for the increase in on resistance of MOSFET due to heating. For an approximate analysis, the factor can be ignored and the maximum on resistance of the MOSFET can be used.

Gate charging loss, $P_G$, results from the current required to charge and discharge the Gate capacitance of the power MOSFET and is approximated as:

$$P_G = Qg * V_{CC} * f_{OSC}$$

Where Qg is the total Gate charge of the MOSFET. Power of VCC is applied by $V_{IN}$ and the MOSFET driving current flows through VCC regulator. The loss PVCC is estimated as:

$$P_{VCC} = (V_{IN} - V_{CC}) * Qg * f_{OSC}$$

So the total Gate charging loss is

$$P_{G\_TOTAL} = P_G + P_{VCC}$$

The total Gate charging loss occurs in IC but not in the MOSFET itself only actually.

Switching loss, $P_{SW}$, occurs in transition period as the MOSFET turns on and off. This loss is consisted of turn on loss and turn off loss.

$$P_{TURN\_ON} = \frac{1}{6}(I_{IN} - \frac{\Delta I_L}{2}) * V_{OUT} * t_r * f_{OSC}$$

$$P_{TURN\_OFF} = \frac{1}{6}(I_{IN} + \frac{\Delta I_L}{2}) * V_{OUT} * t_F * f_{OSC}$$

$$\Delta I_L = \frac{(V_{OUT} - V_{IN}) * V_{IN}}{L * f_{OSC} * V_{OUT}}$$

$$P_{SW} = P_{TURN\_ON} + P_{TURN\_OFF}$$

Where $t_R$ and $t_F$ are the rise and fall times of the MOSFET.

When MOSFET turns off, the $V_{DS}$ (the stress voltage on Drain to Source ) of MOSFET is $V_{OUT}$ plus the ringing. The MOSFET selected must be able to withstand $V_{OUT}$ plus any ringing from drain to Source, and $V_{CC}$ plus ringing from Gate to Source. The MOSFET with $V_{DS}$ =60V and $V_{GS}$> 10V is recommended.

**Diode Selection**

The boost converter requires a diode D to carry the inductor current during the MOSFET off time. Schottky diodes are recommended due to their fast recovery time and low forward. D should be rated to handle the maximum output voltage (plus switching node ringing) and the peak switch current. The conduction loss of diode is calculated by:

$$P_{DIODE} = I_{RMS\_OFF} * V_F \quad \text{in which,}$$

$$I_{RMS\_OFF} = \left[\frac{V_{IN}}{V_{OUT}} * \left(I_{IN}^{\ 2} + \frac{\Delta I_L^{\ 2}}{12}\right)\right]^{\frac{1}{2}}$$

the $V_F$ is the forward voltage of Schottky diode.

**$R_{COMP}$ and $C_{COMP}$ Selection**

AP3039A adopts current mode PWM control to improve transient response and achieve simple loop compensation circuit. The loop compensation parameters $R_{COMP}$ and $C_{COMP}$ in different operating frequency (as shown in Figure 4) are shown in table 1.

| Operating Frequency (kHz) | Compensation Parameter | |
|---|---|---|
| | $R_{COMP}$ (kΩ) | $C_{COMP}$ (nF) |
| 200 | 15 | 3.3 |
| 400 | 15 | 3.3 |
| 600 | 22 | 3.3 |
| 800 | 36 | 3.3 |
| 1000 | 51 | 2.2 |

Table 1. Compensation Selection

## 6. Application Hints

### Input Under-Voltage Detector

AP3039A contain an Under Voltage Lock Out (UVLO) circuit. Two resistors R1, R2 are connected from UVLO pin to ground and the VIN pin (refer to Figure 3.). The resistor divider must be designed such that the voltage on the UVLO pin is higher than 1.25V when VIN is in the desired operating range. If this under voltage threshold is not met., all functions of AP3039A are disabled and system remains in a low power standby state. UVLO hysteresis is accomplished through an internal 22μA current Source that is switched on or off into the impedance of the set-point divider. When the UVLO threshold is exceeded, the current Source is activated to instantly raise the voltage on the UVLO pin. When the UVLO pin voltage falls below the threshold the current Source is turned off, causing the voltage on the UVLO pin to fall. The formula for UVLO can be expresses as blow:

For Input Threshold Voltage

$$V_{IN\_THRESHOLD} = 1.25V * (\frac{(R1+R2)}{R2})$$

For Input Hysteresis Voltage

$$V_{IN\_HYSTERESIS} = 22\mu A * R1$$

### Over-Voltage Protection

AP3039A has an over voltage protection (OVP) circuit. The OV Pin is connected to the center tap of a resistive voltage-divider from the high voltage output to GND (refer to Figure 3.). When the loop is open or the output voltage becomes excessive in any case, result the voltage on OV pin exceeds 1.25V, all functions of AP3039A are disabled, and the output voltage will fall. OVP hysteresis is accomplished with

an internal 22μA current Source and the operation mode is the same as UVLO. The formula for OVP can be expresses as blow:

For OVP Voltage

$$V_{OVP} = 1.25V * (\frac{(R3 + R4)}{R4})$$

For OVP Hysteresis Voltage:

$$V_{OVP\_HYSTERESIS} = 22\mu A * R3$$

### Frequency Selection

An external resistor RT connected from RT pin to GND to set the operating frequency (refer to Figure 3). Operation frequency range is from 150kHz to 1MHz (as shown in Table 2). High frequency operation optimizes the regulator for the smallest component size, while low frequency operation can reduce the switch losses.

| $R_T$ (kΩ) | Operating Frequency (kHz) |
|---|---|
| 470 | 150 |
| 390 | 200 |
| 147 | 400 |
| 95 | 600 |
| 68 | 800 |
| 51 | 1000 |

Table 2. Frequency Selection

### Soft Start

The AP3039A has a soft start circuit to limit the inrush current during startup. The soft start feature allows the boost converter output to gradually reach the initial steady state output voltage, thereby reducing start-up stresses and current surges. The time of startup time is controlled by an internal 12μA current Source and an external soft start capacitor $C_{SS}$ which connected from SS pin to GND (refer to Figure 4). At power on, after the $V_{IN}$ UVLO threshold is reached, the internal 12μA current Source charges the external capacitor $C_{SS}$. The capacitor voltage will ramp up slowly and will limit COMP pin voltage and the switch current.

### VCC Pin Application Description

The AP3039A includes an internal low dropout linear regulator with the output pin VCC. This pin is used to power internal PWM controller, control logic and MOSFET driver. On the condition that $V_{IN} \geq 13.5V$, the regulator generates a 10V supply. If $6V \leq V_{IN} \leq 12.5V$, the $V_{CC}$ is equal to $V_{IN}$ minus drop voltage across bypass switch. When $V_{IN}$ is less than 6V, connect VCC to VIN.

## 7. PCB Layout Guideline

Boost converter performance can be seriously affected by poor layout. To produce an optimal solution for system, good layout and design of the PCB are as important as the component selection. The following PCB layout guideline should be considered:

1. There are two high-current loops in the solution. One is the high-current input loop, and the other is the high-current output loop. The high-current input loop goes from the positive terminal of the $C_{IN}$ to the inductor, to the MOSFET, then to the current-sense resistor, and to the $C_{IN}$' s negative terminal. The high-current output loop goes from the positive terminal of the $C_{IN}$1 to the inductor, to the diode, to the positive terminal of the $C_{OUT}$, reconnecting between the $C_{OUT}$ and the $C_{IN}$ ground terminals. Minimize the area of the two high-current loops to avoid excessive switching noise. The trace connected these two high-current loops must be short and thick.

2. Create two ground islands. One is called Power Ground Island (P Island), the other is called Analog Ground Island (A Island). The P Island consists of $C_{IN}$ and $C_{OUT}$ ground connections and negative terminal of the current-sense resistor $R_{CS}$. Maximizing the width of the P Island traces will improve efficiency and reduces output voltage ripple and noise spike. The A Island is the connection of the OV and UVLO detection-divider ground, $R_T$ resistor ground, $C_V$, $C_{SS}$, and $C_{COMP}$ ground and the device' s exposed backside pad. Connect the P Island and A Island directly to the exposed backside pad. Make no other connections between these separate ground planes.

3. Place the bypass capacitor $C_V$ as close to the device as possible. The ground connection of these capacitors should be connected directly to GND pins with a thick trace.