AN47
Getting more out of the ZXLD1350 - dimming techniques

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Introduction

The ZXLD1350 has a versatile adjust pin that can be used in many ways to adjust the brightness of the LED by controlling the current in the LED. This application note deals with some the ways in which dimming the LED can be achieved and discusses the merits of the techniques. These dimming methods discussed include PWM dimming both with a low and high frequency signals, DC voltage control and resistive dimming.

Low frequency dimming

Low frequency dimming is preferred for LED dimming since the LED instantaneous driving current is constant. The color temperature of the LED is preserved at all dimming levels. Another advantage of low frequency dimming is that the dimming level can down to 1%. Hence result in dimming range of 100:1.

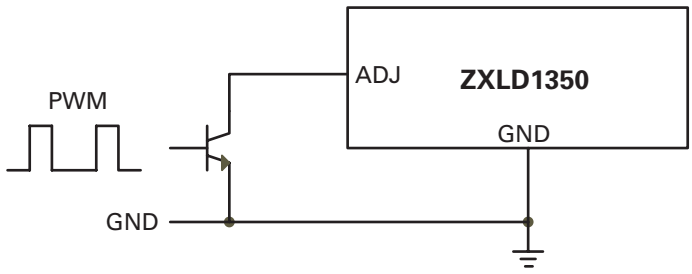
Choice of frequency

To avoid visible flicker the PWM signal must be greater than 100Hz. If you choose too high a frequency the internal low pass filter will start to integrate the PWM signal and produce a non linear response. Also the soft start function of the ADJ pin will cause a delay on the rising a falling edge of the PWM signal. This can give a non-linearity in the LED current which will have a greater affect as frequency increases.

An upper limit of 1kHz is suggested. The effect of audible noise in the inductor may need to be considered. This may happen in some inductors with loose windings and will be more noticeable at PWM frequencies of 1kHz than 100Hz.

If the PWM frequency is less than approximately 500Hz, the device will be gated 'on' and 'off' and the output will be discontinuous, with an average value of output current given by:

$$I_{OUT} \approx \frac{0.1\,D_{PWM}}{R_S} \quad [\text{for } 0<D_{WPM}<1]$$

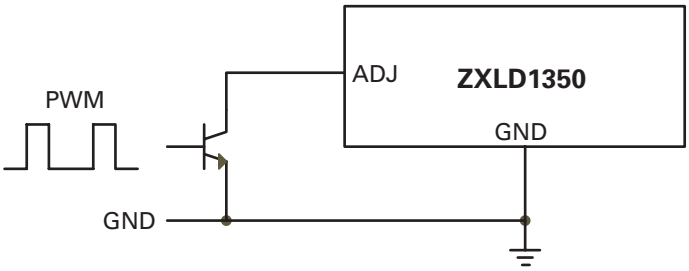


High frequency dimming

High frequency dimming is preferred if system required low radiated emission and in/output ripple. But dimming range is reduced to 5:1. The ZXLD1350 has an internal low pass filter which integrates the high frequency PWM signal to produce a DC dimming control.

If the PWM frequency is higher than approximately 10kHz and the duty cycle above the specified minimum value, the device will remain active and the output will be continuous, with a nominal output current given by:

$$I_{OUT} \approx \frac{0.1\,D_{PWM}}{R_S} \quad \text{[for } 0.16 < D_{PWM} < 1\text{]}$$



Input buffer transistor

For PWM dimming an input bipolar transistor with open collector output is recommended. This will ensure the 200mV input shutdown threshold is achieved.

It is possible to PWM directly without a buffer transistor. This must be done with caution. Doing this will overdrive the internal 1.25V reference. If a 2.5V input level is used at 100% PWM (DC) the output current into the LED will be 2X the normal current which may destroy the ZXLD1350. Overdriving with a 5V logic signal is very likely to damage the device as it exceeds the ADJ pin voltage rating.

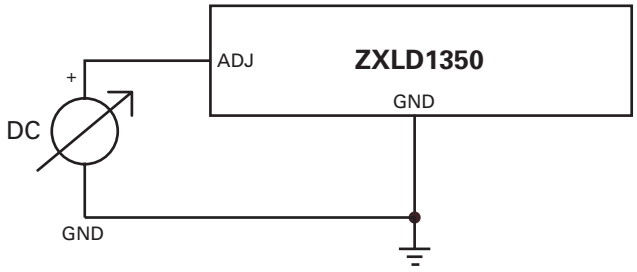
Soft start and decoupling capacitors

Any extra capacitor on the ADJ pin will affect the leading and falling edge of the PWM signal. Take this into account as the rise time will be increased by approximately 0.5ms/nF.

Compare this with a 100Hz PWM. 50% duty cycle T_{on} and T_{off} are 5ms at 1% duty cycle T_{on} is 0.1ms. 1nF on the ADJ pin will cause 0.5ms rise time which result in an error and limitation in dimming at low duty cycles.

DC voltage dimming

The ADJ pin can be overdriven by an external DC voltage (V_{ADJ}), as shown, in order to override the internal voltage reference and adjust the output current to a value above or below the nominal value.



The nominal output current is then given by:

$$I_{OUT} \approx \frac{0.08 \times V_{ADJ}}{R_S} \quad \text{[for 0.3< } V_{ADJ} \text{ <2.5V]}$$

Note that 100% brightness setting corresponds to $V_{ADJ} = V_{REF}$.

If V_{IN} is 2.5V max the R_{SENSE} should be increased by 2X R_S. This will slightly decrease the efficiency by 1 to 2% .

The input impedance of the ADJ pin is 200kΩ ±20%. This may be factor if the DC voltage with a relatively high output resistance.

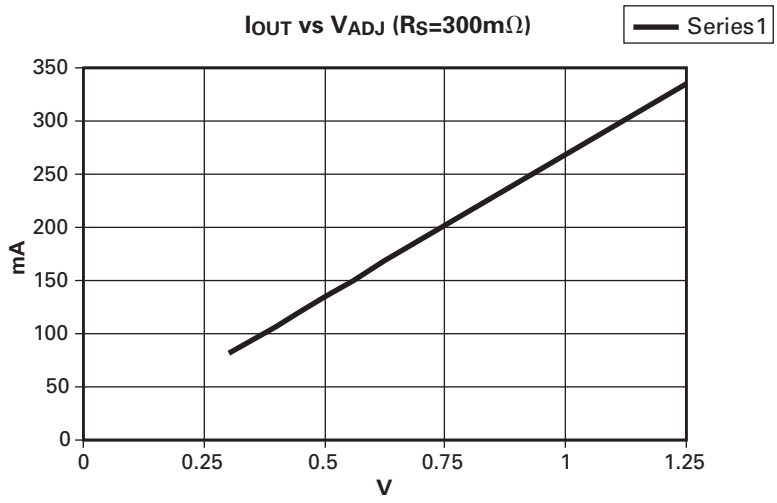


Figure 1 Typical output current versus ADJ voltage with R_S = 300mΩ

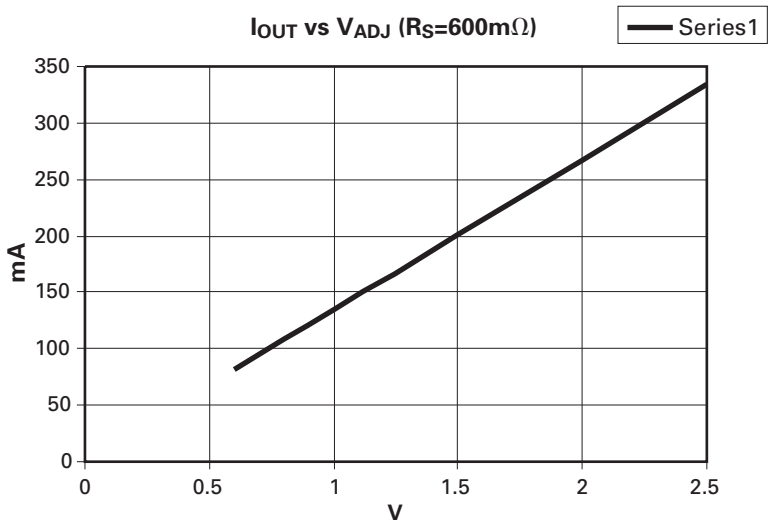


Figure 2 Typical output current versus ADJ voltage with R_S = 600mΩ

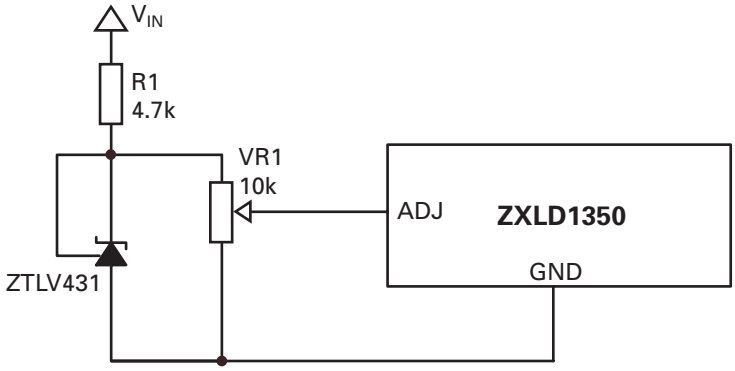


Figure 3 Typical circuit of DC voltage dimming

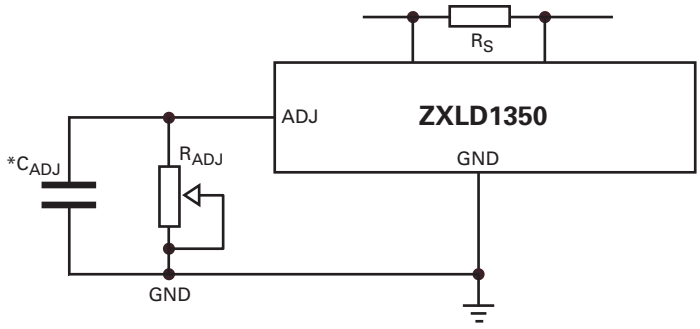
The ZTLV431 acts as a shunt regulator to generate an external 1.25V reference voltage. The reference voltage is applied to pot VR1 to provide dimming voltage of 0-1.25V.

Using an external regulator affects the accuracy of the current setting. If a 1% reference is used the LED current will be more accurate than using the internal reference.

Resistor dimming

By connecting a variable resistor between ADJ and GND, simple dimming can be achieved.

Capacitor C_{ADJ} is optional for better AC mains interference and HF noise rejection. Recommend value of C_{ADJ} is 0.22µF.



The current output can be determined using the equation:

$$I_{OUT} = \frac{(0.08/R_S) \times R_{ADJ}}{(R_{ADJ} + 200k)}$$

Note that continuous dimming is not possible with a resistor. At some point the shutdown threshold will be reached and the output current reduced to zero. This can occur below 300mV.

Note that a 1MΩ resistor will load the V_{REF} on the ADJ pin. The V_{REF} will now be divided down by the nominal 200k V_{REF} resistance and the 1M R_{ADJ}. The nominal voltage will now be approximately 1V. R_S will need to be adjusted to set the maximum current.

The +/20% tolerance of the input resistance should also be understood. See table below:

Table 1

R_{ADJ} kΩ	Rint nom. kΩ	Rint min. kΩ	Rint max. kΩ	V_{ADJ} nominal	% error from nominal Due to Rint min.	% error from nominal Due to Rint max.
1000	200	160	240	1.041	3.4%	-3.3%
500	200	160	240	0.892	6.1%	-5.7%
200	200	160	240	0.625	11.1%	-10.0%
100	200	160	240	0.416	15.4%	-13.3%

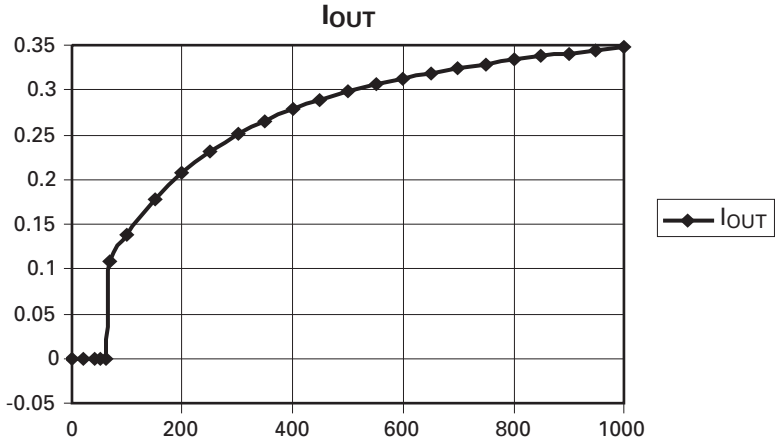


Figure 4 Typical output current against pot resistance

If linear pot is used, the output current change is not linear against shaft rotation.

In order to make the output current more linear, a log type pot is used.

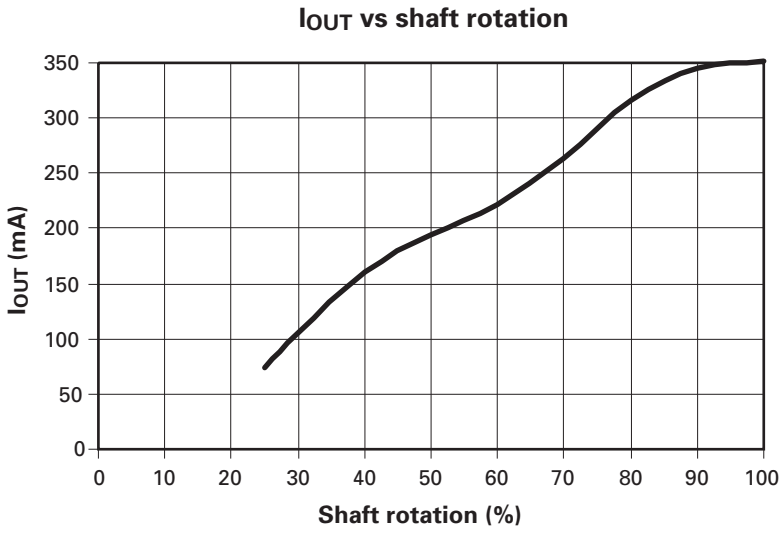


Figure 5 Output current against shaft rotation of log type pot

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