PIxEQX6741Sx
PIxEQX6741Sx SATA ReDriver Application Note

Introduction

PIxEQX6741Sx SATA ReDriver™ devices are developed to re-drive one full-lane of SAS/SATA signals up to 6Gbps. The devices' features include lower power consumption and high performance. Figure1 shows typical application examples.

PIxEQX6741Sx series devices support Termination Detect indication (TDet_A# or TDet_B#), which provides indication when load (HDD or Host) is connected. Also, HDD unplug condition feature can be used to control the device to go into power saving mode by the host.

Packaging: 20-contact TQFN (4x4mm)

Main Applications:
- Server
- Desktop
- Storage/Workstation

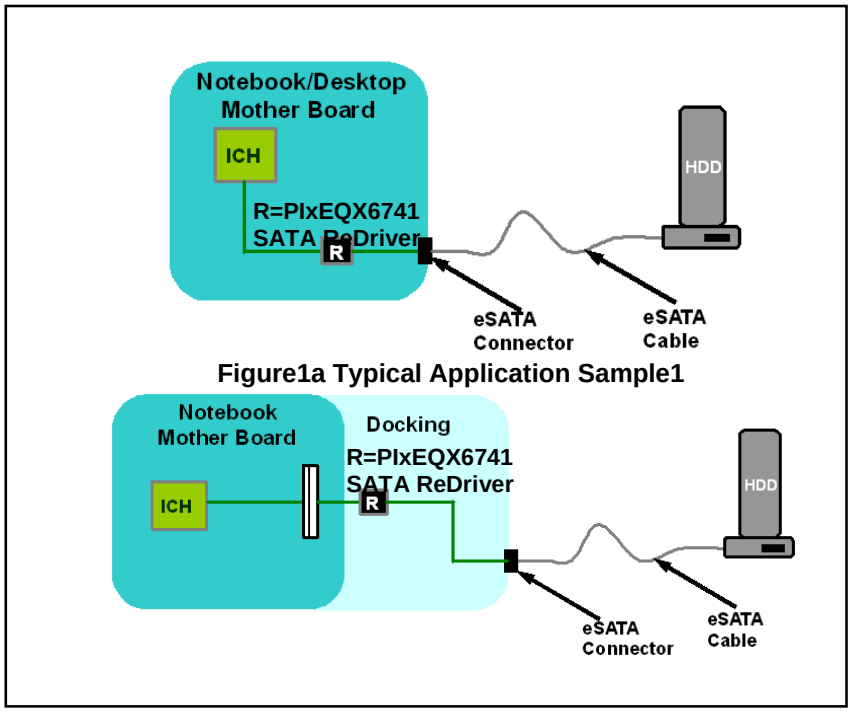


Figure 1: Examples of Typical Application

PIxEQX6741Sx Part Selection for Various Applications

PIxEQX6741Sx series devices include PI3EQX6741ST, PI3EQX6741STB and PI2EQX6741SL. These parts'

Applications	Standards	Recommended Device	Package
Low Power 1.05V VDD; NoteBook/Docking	SATA 1.5G, 3.0G, 6.0G	PI2EQX6741SL	TQFN-20
3.3V VDD; NoteBook/Docking Desktop Sever/Storage	SATA 1.5G, 3.0G, 6.0G SAS (G1-1.5g, G2-3.0g)	PI3EQX6741ST PI3EQX6741STB, compatible with TI-SN75LVCP412CD	TQFN-20

Table 1: Application Based Selection Table

PI2EQX6741SLZDE supports +1.05V power supply, and the other two parts support from +3.3V power supply.

Comparison of Feature (Part Number)	VDD (V)	Power consumption (mW)			Termination Detect	
		Max.	Slumber Mode	Standby	Y/N	Power Consumption(mW) When HDD is unplugged
PI2EQX6741SLZDE	1.05	104.5	15.4	1.1	√	5.5
PI3EQX6741S TZDE PI3EQX6741S TBZDE	3.3	342	50	3.6	√	18

Table 2: Power consumption at 1.2V and 2.5~3.3V Power Supply

External Components Requirement

PIxEQX6741SxZDE series devices require AC coupling capacitors for all redriver inputs and outputs. High-quality, low-ESR, X7R, 10nF, 0402-sized capacitors are recommended.

Layout Design Guide

Layout Considerations for Differential Pairs

- The trace length miss-matching shall be less than 5 mils for the "+" and "–" traces in the same pairs
- Use wider trace width, with 100ohm differential impedance, to minimize the loss for long routes
- Target differential Zo of 100ohm ±20%
- More pair-to-pair spacing for minimal crosstalk coupling, it is recommended to have >3X gap spacing between differential pairs.
- It is preferable to route differential lines exclusively on one layer of the board, particularly for the input traces
- The use of vias should be avoided if possible. If vias must be used, they should be used sparingly and must be placed symmetrically for each side of a given differential pair.
- Route the differential signals away from other signals and noise sources on the printed circuit board

PCB Layout Trace Routings

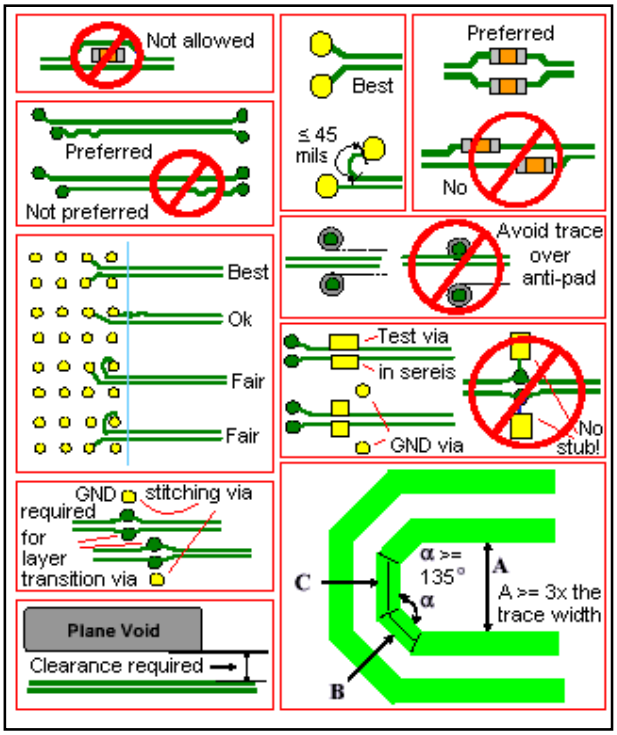


Figure 2: Layout Sample for Trace Routings

Power-Supply Bypass

Designers must pay attention and be careful with the details associated with high-speed design as well as providing a clean power supply; there are some approaches that are recommended.

- The supply (VDD) and ground (GND) pins should be connected to power planes routed on adjacent layers of the printed circuit board. The distance to plane should be <50mil.
- The layer thickness of the dielectric should be minimized so that the VDD and GND planes create a low inductance supply with distributed capacitance.
- Careful attention to supply bypassing through the proper use of bypass capacitors is required. A low-ESR 0.01uF bypass capacitor should be connected to each VDD pin such that the capacitor is placed as close as possible to PIxEQX6741SxZDE. Smaller body size capacitors can help facilitate proper component placement.
- The distance of capacitors to IC body should be <100mil.
- One capacitor with capacitance in the range of 1uF to 10uF should be incorporated in the power supply bypassing design as well. It is can be either tantalum or an ultra-low ESR ceramic.

Power Supply Sequencing

Proper power supply sequencing is recommended for all devices. Always apply GND and VDD before applying signals. especially if the signal is not current limited.

Caution: Do NOT exceed the absolute maximum ratings because stresses beyond the listed ratings can cause permanent damage to the device.

Equalization and Pre-emphasis Setting

Various Input Traces and Eye Tests with different EQ settings

Figure 3 shows the test setup for testing PIxEQX6741SxZDE in different EQ setting. "R" in the figure represents PIxEQX6741SxZDE.

Signal Source: PRBS2^7-1 pattern, Differential Voltage is 600mV, Pre-emphasis is 0dB

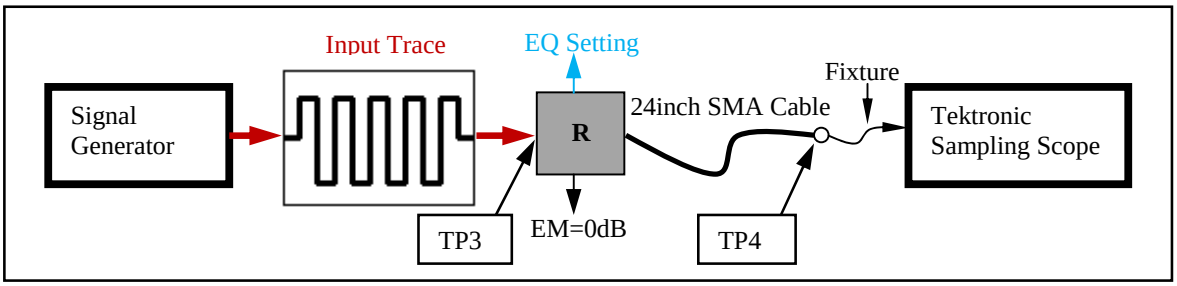


Figure 3: EQ Setting Test Setup for PIxEQX6741SxZDE

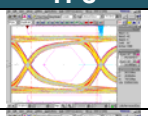
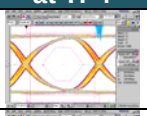
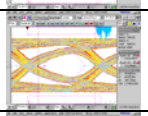
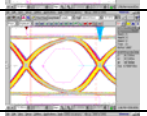
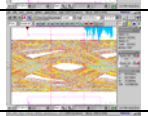
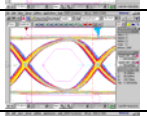
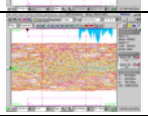
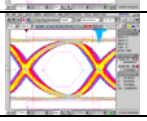
Input Trace Length	EQ Setting	Input Eye at TP3	Output Eye at TP4
6 inch FR4 Lab trace (-2dB loss at 3GHz)	3dB (A_EQ or B_EQ =Low)		
18 inch FR4 Lab trace (-6dB loss at 3GHz)	3dB (A_EQ or B_EQ =Low)		
30 inch FR4 Lab trace (-10dB at 3GHz)	6dB (A_EQ or B_EQ =Open)		
48 inch FR4 Lab trace (-16dB loss at 3GHz)	9dB (A_EQ or B_EQ =High)		

Table 3: Eye Diagram vs. Input FR4 trace and EQ Setting at 6Gb/s

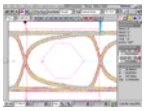
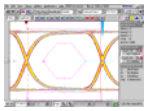
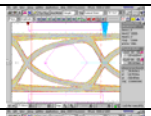
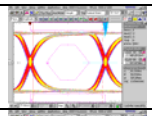
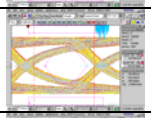
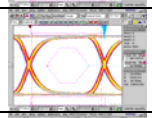
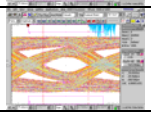
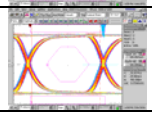
Input Trace Length	EQ Setting	Input Eye at TP3	Output Eye at TP4
6 inch FR4 Lab trace (-1.2dB loss at 1.5GHz)	2.5dB (A_EQ or B_EQ =Low)		
18 inch FR4 Lab trace (-3dB loss at 1.5GHz)	2.5dB (A_EQ or B_EQ =Low)		
30 inch FR4 Lab trace (-5dB loss at 1.5GHz)	5dB (A_EQ or B_EQ =Open)		
48 inch FR4 Lab trace (-9dB loss at 1.5GHz)	7.5dB (A_EQ or B_EQ =High)		

Table 4: Eye Diagram vs. Input FR4 trace and EQ Setting at 6Gb/s

Various Input Traces and Eye Tests with different Pre-emphasis settings

Figure 4 shows the test setup for testing PIxEQX6741SxZDE in different EM setting. “R” in the figure represents PIxEQX6741SxZDE.

Signal Source: PRBS2^7-1 pattern, Differential Voltage is 600mV, Pre-emphasis is 0dB

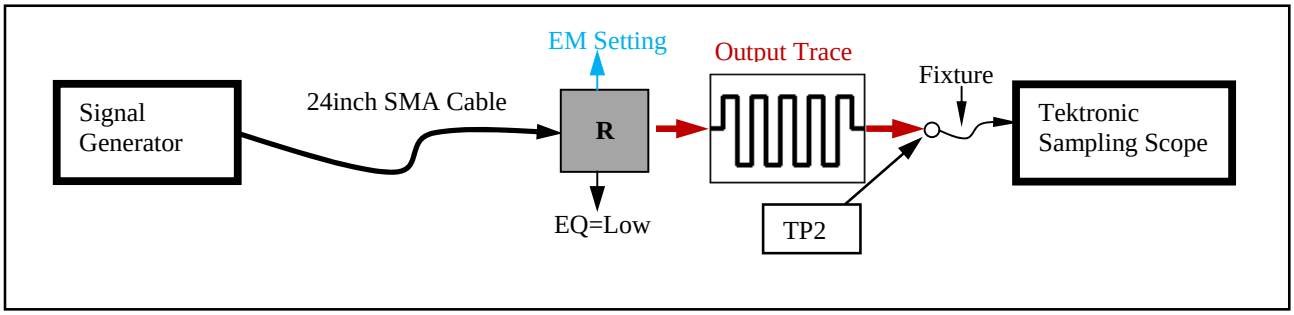


Figure 4: EM Setting Test Setup for PIxEQX6741SxZDE

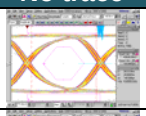
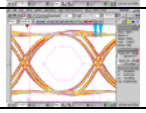
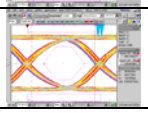
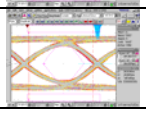
EM Setting	Eye Test at TP2 for Various Output Trace		
	No trace	6 inch FR4 Lab trace (-2dB loss at 3GHz)	12 inch FR4 Lab trace (-4dB loss at 3GHz)
EM=low			
EM=High			

Table 5: Eye Diagram vs. Output FR4 Trace and EM setting at 6Gb/s

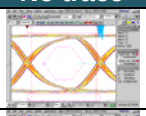
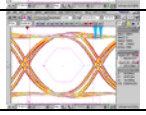
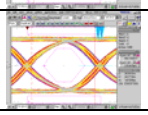
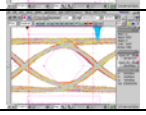
EM Setting	Eye Test at TP2 for Various Output Trace		
	No trace	6 inch FR4 Lab trace (-1.2dB loss at 1.5GHz)	12 inch FR4 Lab trace (-2.2dB loss at 1.5GHz)
EM=low			
EM=High			

Table 6: Eye Diagram vs. Output FR4 Trace and EM setting at 3Gb/s

Termination Detect Feature

Figure 5 shows the test setup for testing termination detect feature. “R” in the figure represents PIxEQX6741SxZDE.

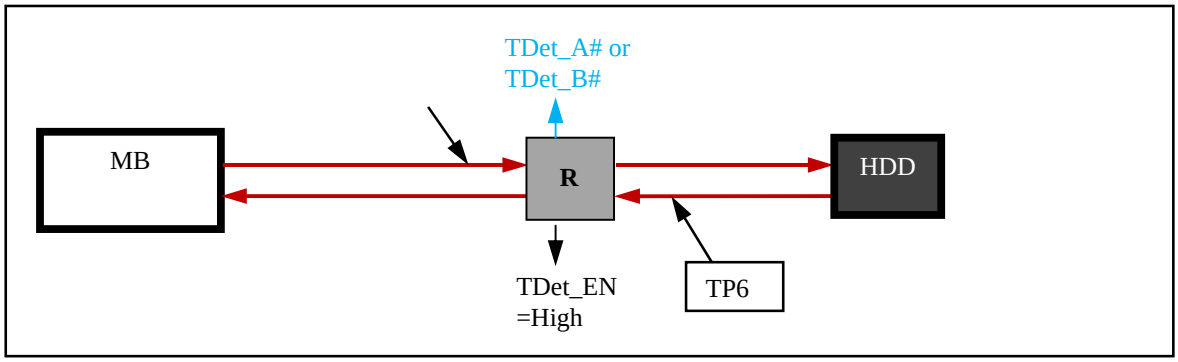


Figure 5: PIxEQX6741SxZDE test setup for Termination Detect Feature

Table7 shows the relationship between TDet_A#/TDet_B# and SATA signal at TP5/TP6 when HDD/HOST is plugged and unplugged at TDet_EN=HIGH

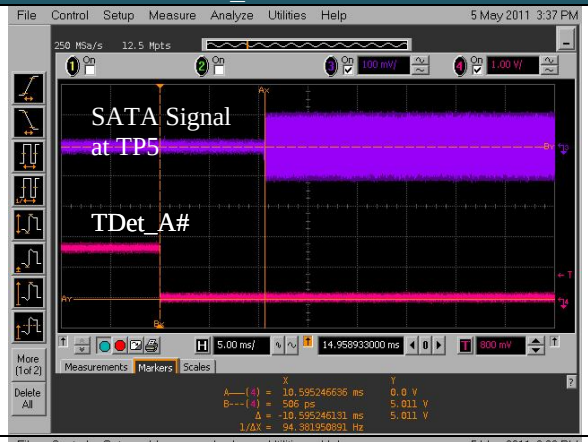
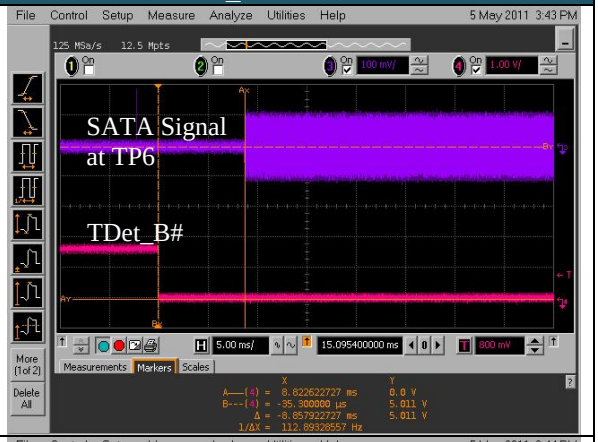
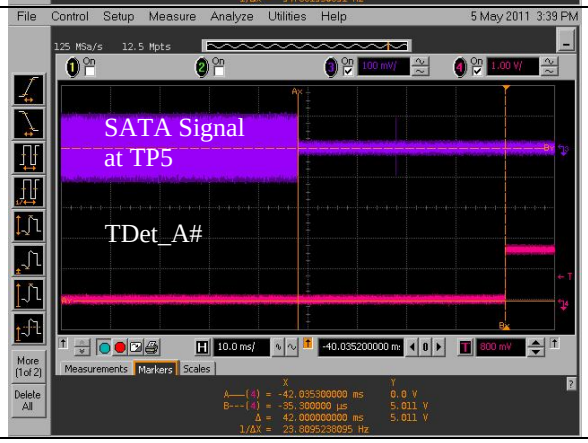
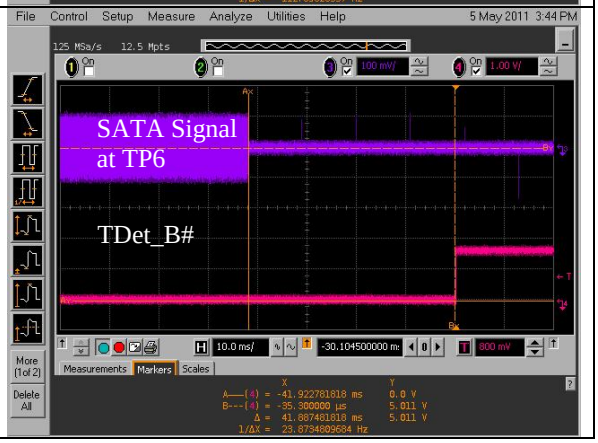
HDD/HOST	A/B_OS=2.7kohm	A/B_OS =2.0kohm
Plugged		
Unplugged		

Table 7: TDet_A#/TDet_B# and SATA signal at TP5/TP6

Typical Application Circuit

Figure 6a and 6b show typical application circuits of PI3EQX6701xZDE.

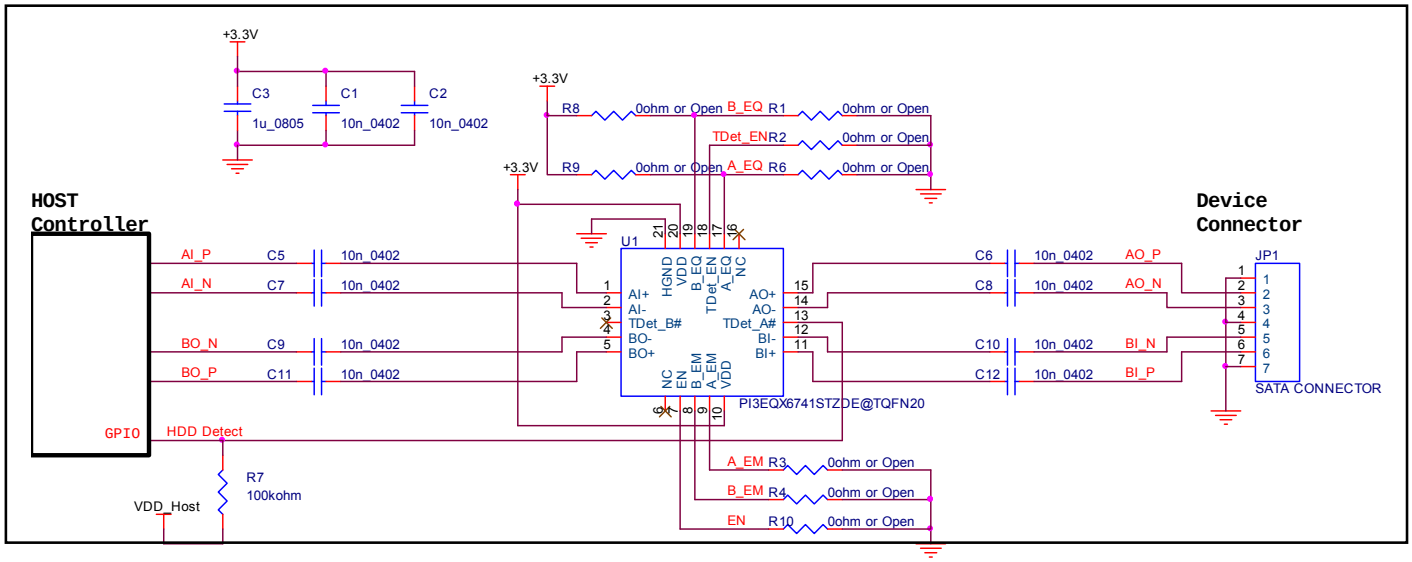


Figure 6: Typical Application Circuit of PI3EQX6741STZDE

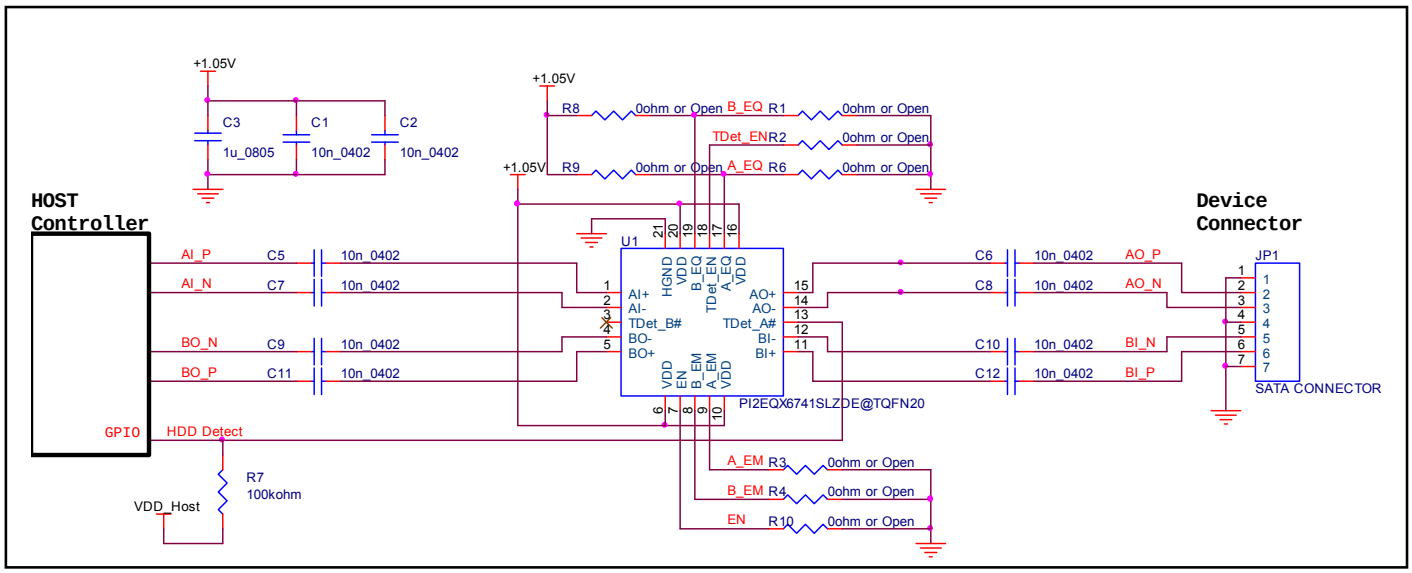


Figure 7: Typical Application Circuit of PI2EQX6741SLZDE

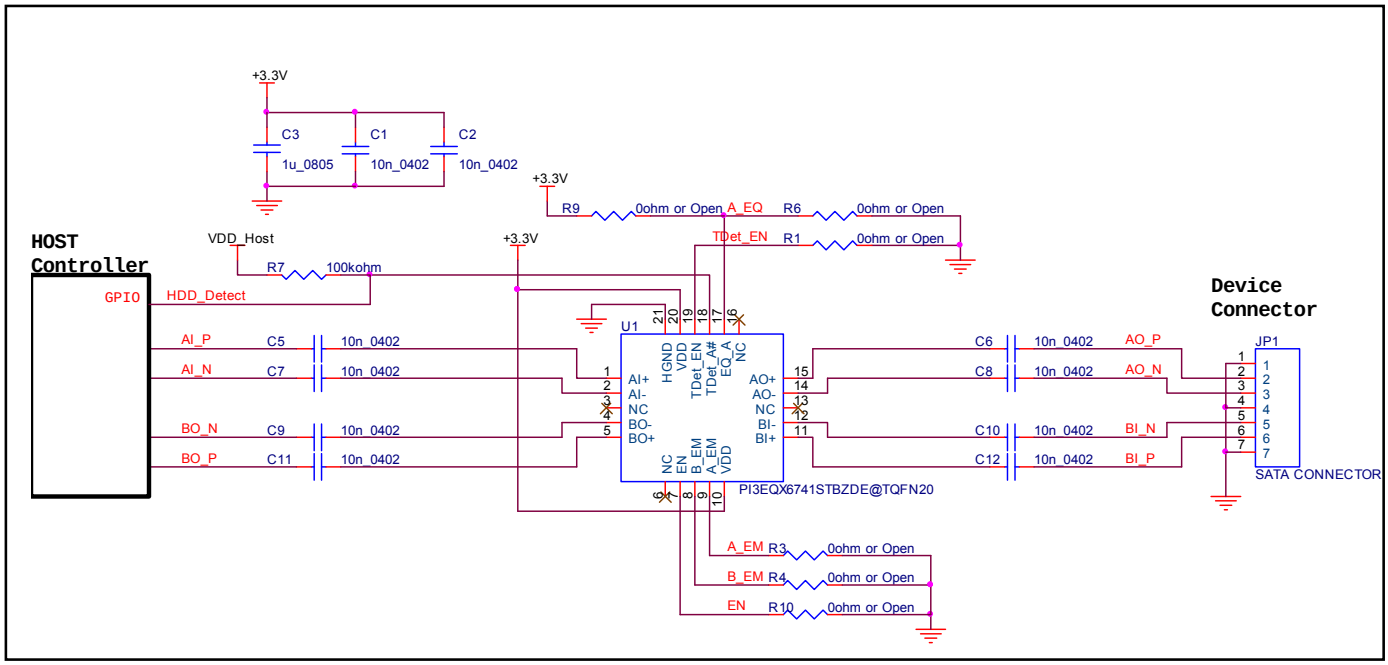


Figure 8: Typical Application Circuit of PI2EQX6741SLZDE

Sample PCB Layout

Figure 9 shows typical layout routing of PI3EQX6741STZDE.

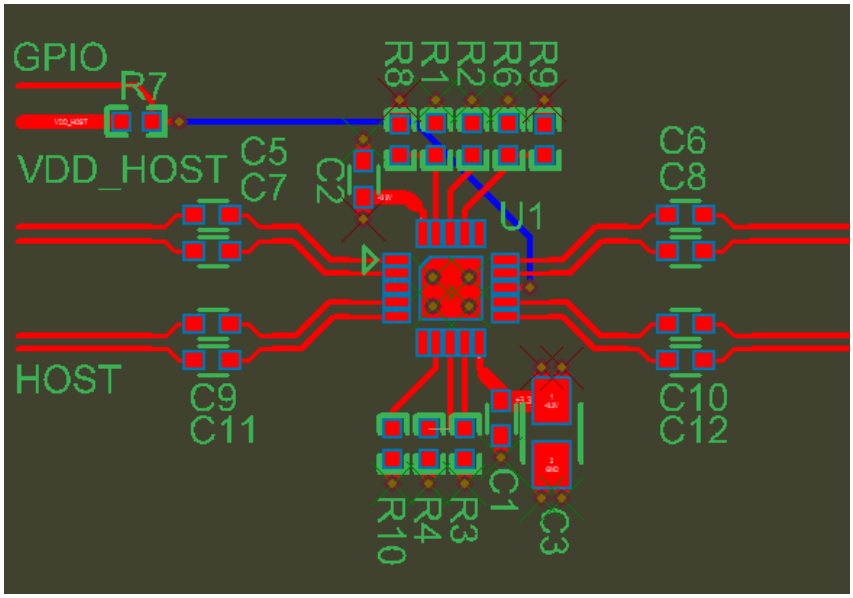


Figure 9: Typical Layout Routing of PI3EQX6741STZDE

Figure 10 shows typical layout routing of PI3EQX6741SLZDE.

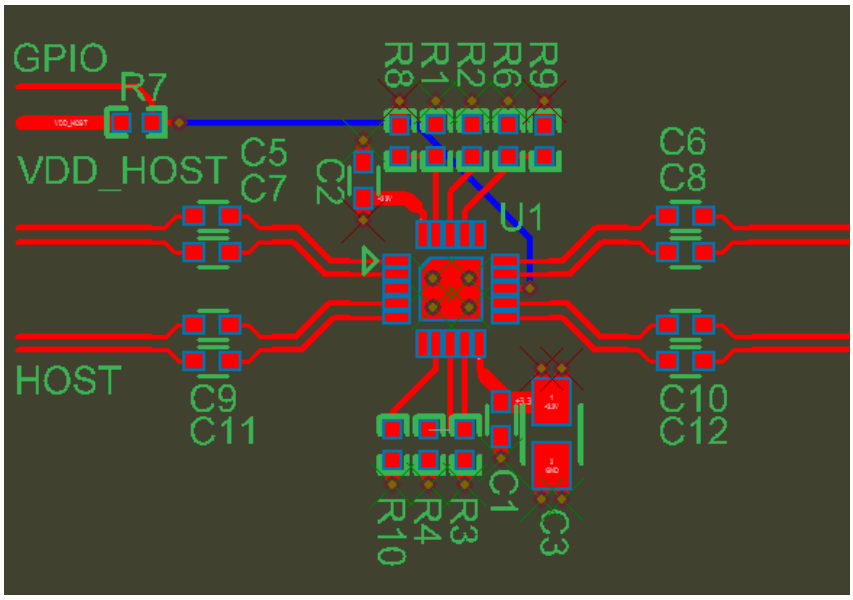


Figure 10: Typical Layout Routing of PI3EQX6741SLZDE

Figure 11 shows typical layout routing of PI3EQX6741STBZDE.

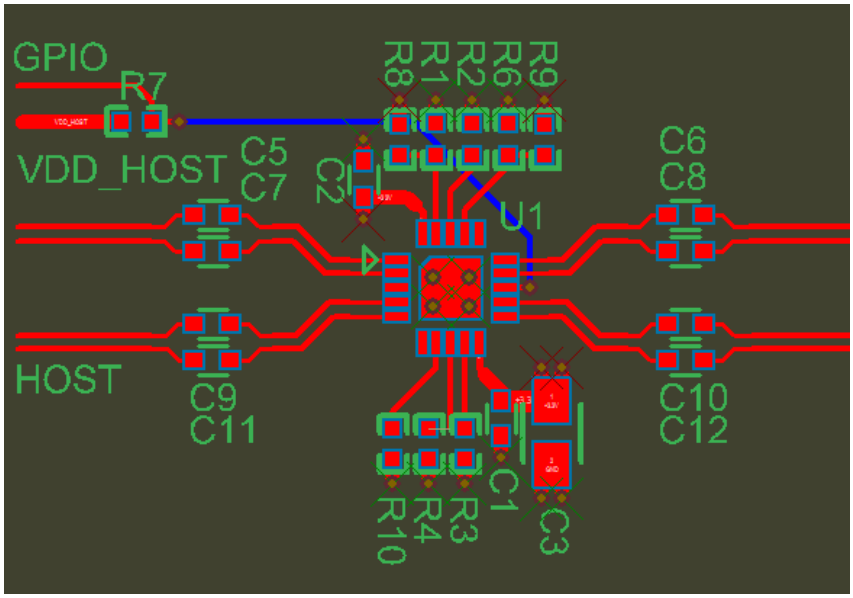


Figure 11: Typical Layout Routing of PI3EQX6741STBZDE