AN1191

DC-DC PCB Layout Design for EMC

Isaac Sibson and Naveed Chowdhury, Automotive Applications Engineers, Diodes Incorporated

Electromagnetic Compatibility (EMC) is an increasingly important topic as switching regulators and LED drivers become more and more widely used. EMC is something that occurs at a system level – not just the electronic components in question but how they are put together, most significantly on a Printed Circuit Board (PCB). In this application note we will look at some simple recommendations to try to achieve the best possible EMC performance. A well-designed PCB can mean that less additional components and countermeasures are required, saving system cost.

A DC-DC converter is a switching device and therefore it can generate significant amounts of Electromagnetic Interference (EMI). This is a huge problem for EMC as the system could fail the applicable EMC standards.

Routing and Via Placement

General placement

Firstly, consider the general component placement on the PCB. Placing signal tracking towards the board edge without ground copper surrounding it can create additional EMI, caused by longer ground return paths and radiation from tracks close to the board edge (as shown in figure 1).

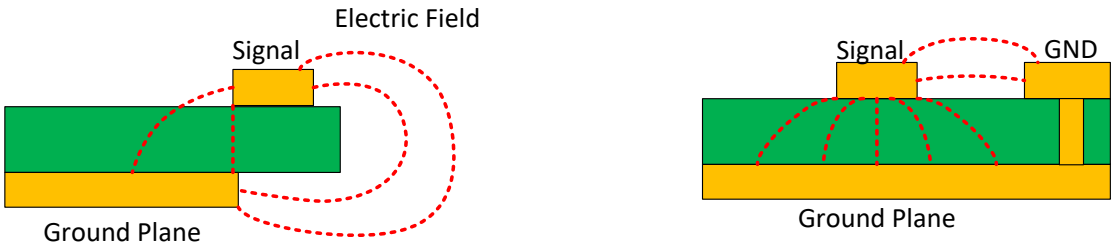

Figure 1: Different tracking approaches and their effects

Placing the components as centrally as possible allowing a good ground perimeter is good practice, as shown in figure 2. Figure 2 below shows the top view of the ground perimeter. The idea is to keep all the noise in the white box, to keep the ground solid, strongly tied and to keep the outside perimeter for decoupling purposes.

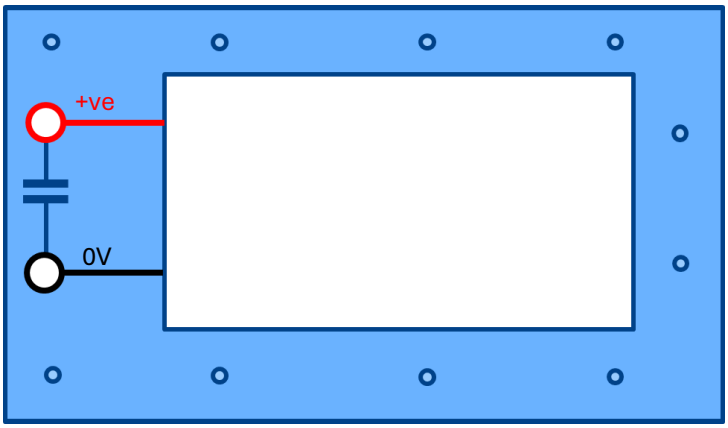

Figure 2: GND perimeter recommendation

General Tracking

The next point to consider is tracking. Tracks have inductance and capacitance between other tracks and ground planes. Keeping the noisiest tracks, e.g. the tracks of switching nodes, as short as possible benefits the overall performance of the PCB. Placing the DC-DC converter and the inductor close together and keeping the tracking short is essential for good EMC performance. The datasheets for the AP64xxxQ products have good guidance on how to optimize PCB layout for DC-DC converters:

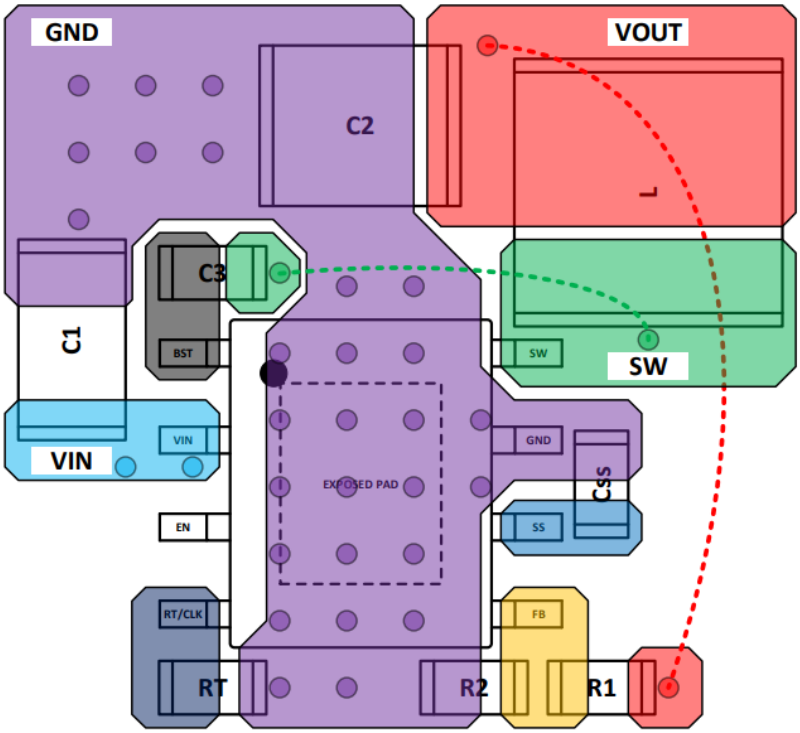

Figure 3: PCB layout recommendation for the AP64xxxQ family of DC-DC converters

DDB108

Figure 4 shows the DDB108R1, a demo board for the AP64xx2Q family of DC-DC converters, which has been designed to follow the guidance laid out in the datasheet. The DDB108R1 passes CISPR 25 Class 4 conducted.

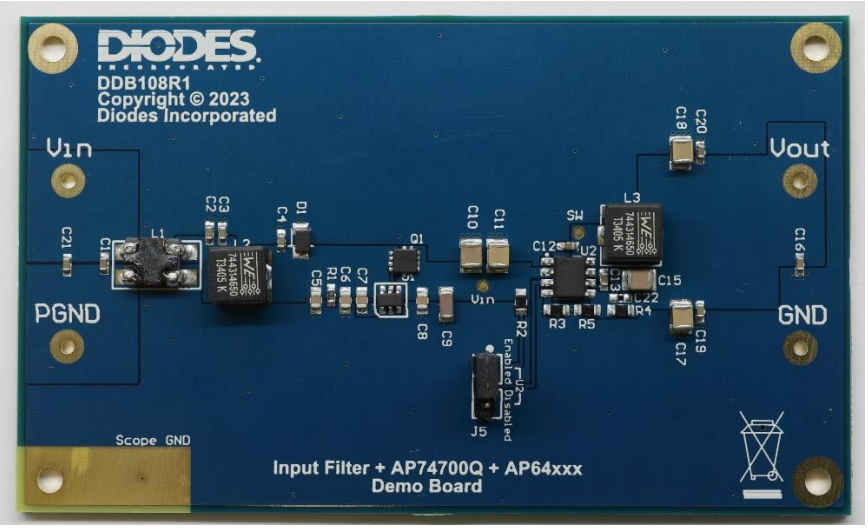

Figure 4: DDB108R1

This board will be shown as an example of following the simple guidelines laid out in this app note, as well as showing some improvements to the design (DDB108R2).

Switching Loop

Highlighted in figure 5 (in light blue) is the switching loop of the DDB108R2. The switching loop is designed to be kept as tight as possible. This is because the current loop for the switching part of the circuit is the main source of noise in a switching DC-DC converter. The loop will act like an antenna for high-frequency. This can disturb the other sensitive signals on the PCB and could even interfere with neighbouring electronics. The loop area of an antenna is directly proportional to its gain; therefore, a larger loop area means a loop antenna with larger gain which will increase EMI.

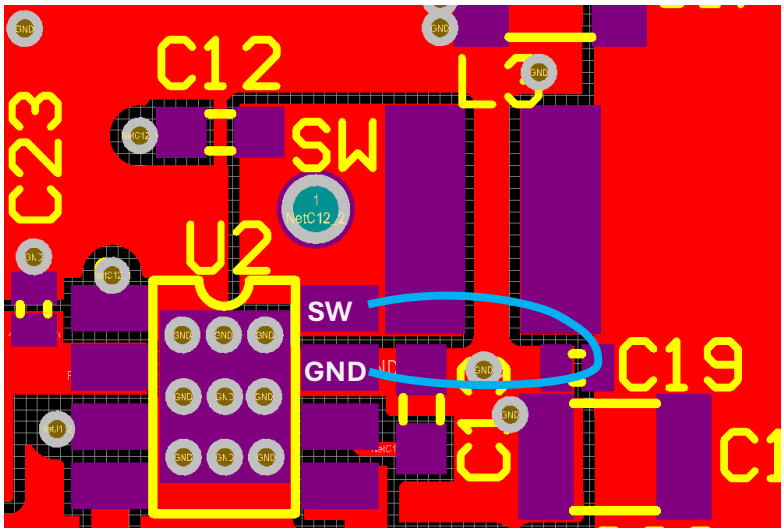

Figure 5: DDB108R2 Switching Loop

V_{IN} Decoupling Loop

Figures 6 and 7 show the two loops that we are trying to minimize in our circuit design. The V_{IN} decoupling loop is shown in green in both images. The purple loop in figure 6 denotes the switching loop discussed previously.

The inductance of the V_{IN} decoupling loop needs minimizing to minimize noise and ensure solid decoupling, making sure that the VIN track is kept as quiet as possible. This is vital as the input track is one that will conduct (and radiate) EMI directly to the outside world. Shown below is the DDB108R2, the ground decoupling loop is shown in green. It is kept as short as possible and decoupled with an 0402 capacitor (C23). The input decoupling is more of a priority than the bootstrap capacitor track (shown below by a light blue arrow), this has been implemented for the DDB108R2 as seen below.

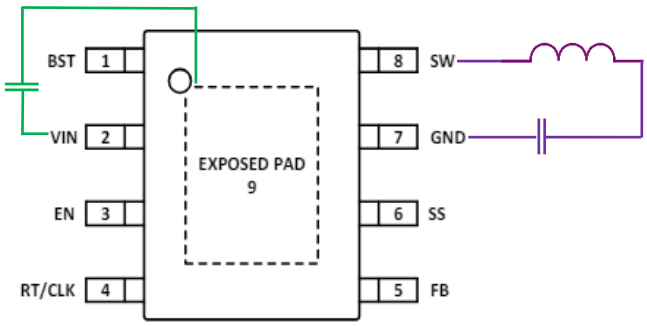

Figure 6: AP64xx2Q V_{IN} decoupling and switching loops decoupling loop

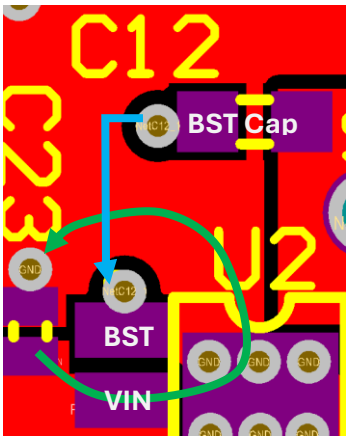

Figure 7: DDB108R2 V_{IN}

Feedback

Making sure that the ground point of the feedback components is as close as possible to the IC ground point is essential in ensuring regulator stability. Also having a common ground reference between the IC ground and feedback component ground ensures good output regulation. Figure 8 shows the component location (blue box and white arrow) and common ground point (green arrow).

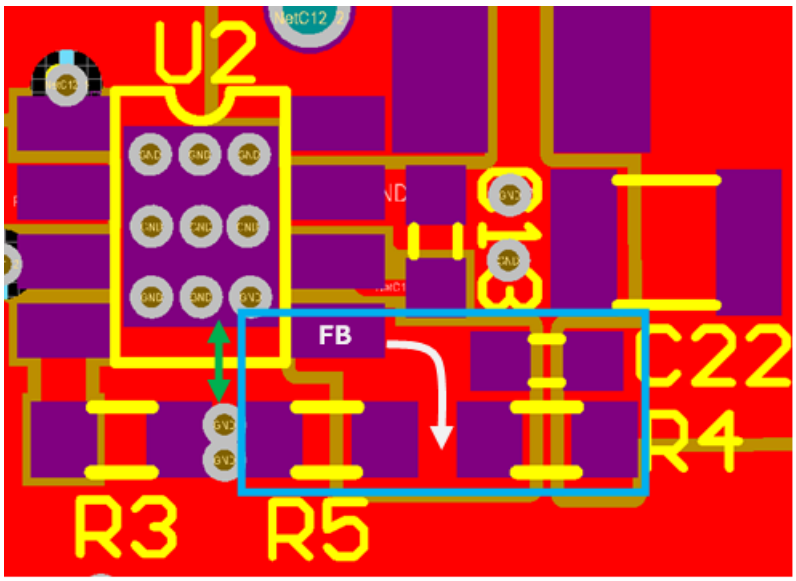

Figure 8: DDB108R2 feedback routing

Vias

It is important to keep plenty of stitching vias dotted around the ground plane. This is to ensure that there is ground plane continuity across layers and there is a short, direct path for the currents to travel between the different grounds. This reduces inductances and ensures there is as little difference in ground potential as possible.

The ground pin of each component (where applicable) has parallel vias surrounding it, which reduces inductance allowing for better high-frequency connection. If the DC-DC converter has a ground tab, make sure that the ground pad has plenty of vias to fill the pad.

It is vital that there is sufficient ground flooding around vias/holes, as cuts in the ground plane can act as antennas. Figure 9 shows how to correctly place vias to allow for sufficient ground flooding.

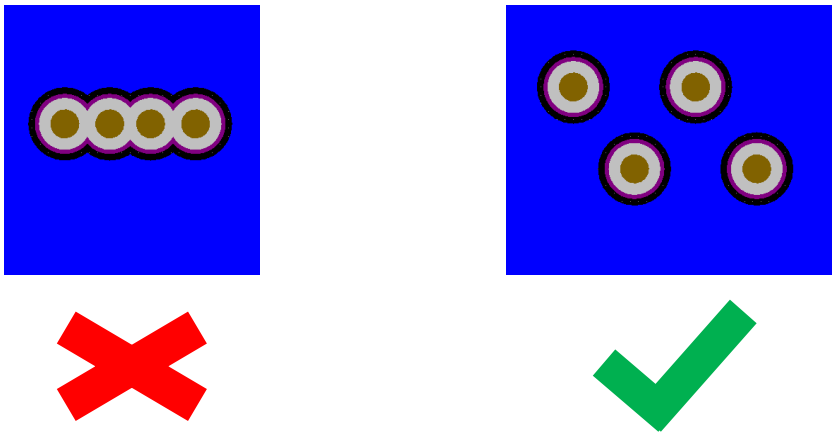

Figure 9: Via Placement, left is incorrect, right shows a suggestion of correct placement

In figure 10, you can see how the ground current behaves with the two via placements as shown in figure 9. The image on the left (below) illustrates that the vias have created a large cutout in the ground plane which means the ground currents need to take a longer path compared to the image on the right.

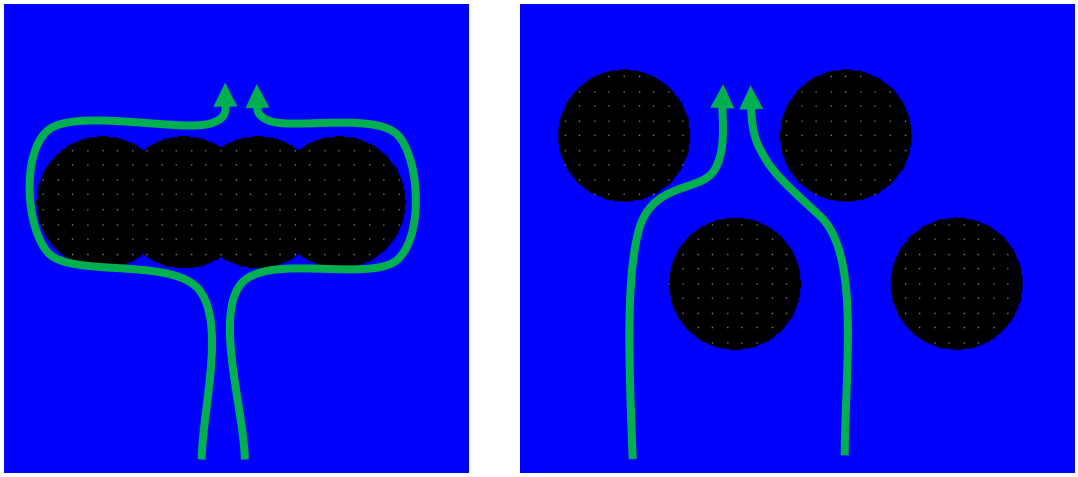

Figure 10: Ground current paths of different via placements

Layer Stacking

The number of layers and layer stack-up is a vital consideration. Whilst a 2-layer board can work, 4 layers are recommended for both heat dissipation and EMC. By allowing solid ground planes and more layers to route on, it makes PCB design a lot easier for the engineer. It is important to think of loop sizes in the Z-axis as well as the X/Y axes. The loop sizes are not only the routing on the top of the board, but also include the ground return path across layers. The are many layer stack-ups that could work, however our recommended use of 4 layers for DC-DC converters is shown in figure 11:

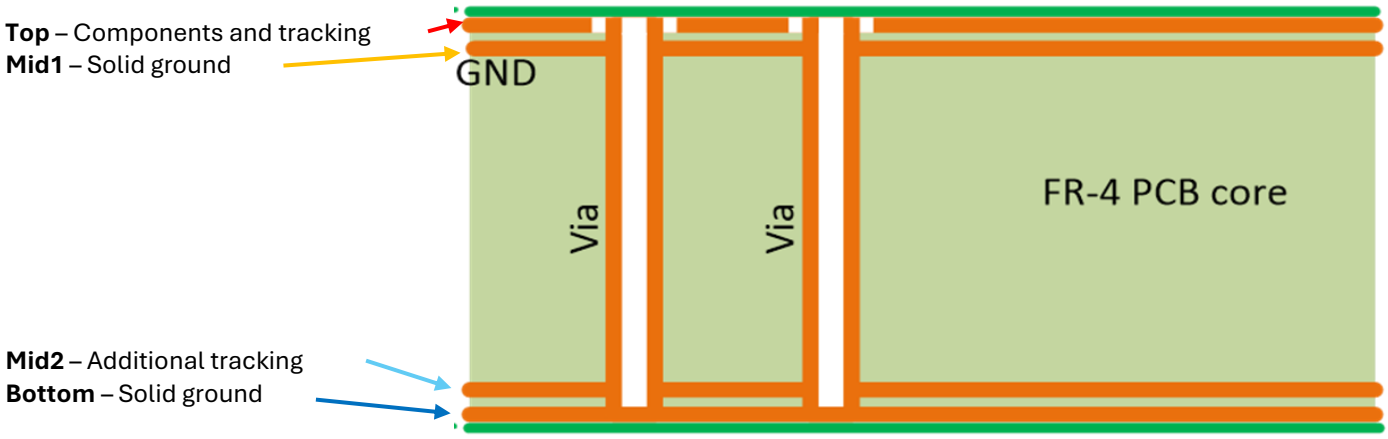

Figure 11: 4-Layer stack recommendation

Top is used for component placement and most of the tracking.

Mid1 is an adjacent ground layer, this minimises the vertical loop size.

Mid2 is for any additional tracking, preferably only a layer dedicated to power traces.

Bottom is another solid ground layer, serving as shielding to help radiated emissions.

Figure 12 shows the different ground return loop area sizes, and inductance of a 2-layer board.
Figure 13 shows the different ground return loop area sizes, and inductance of a 4-layer board.

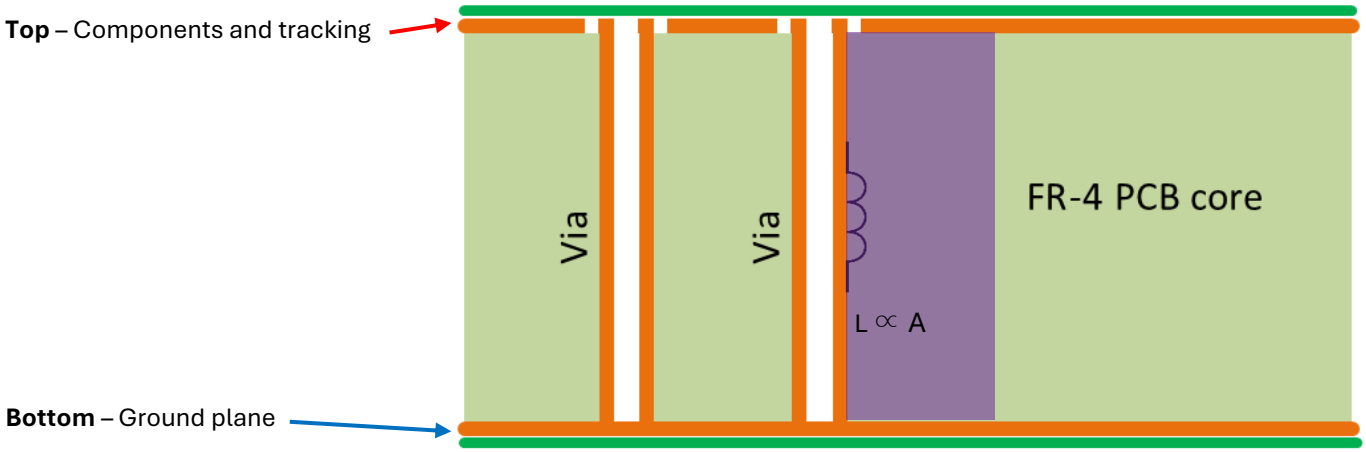

Figure 12: 2-Layer PCB cross section, purple box indicating vertical ground return loop area

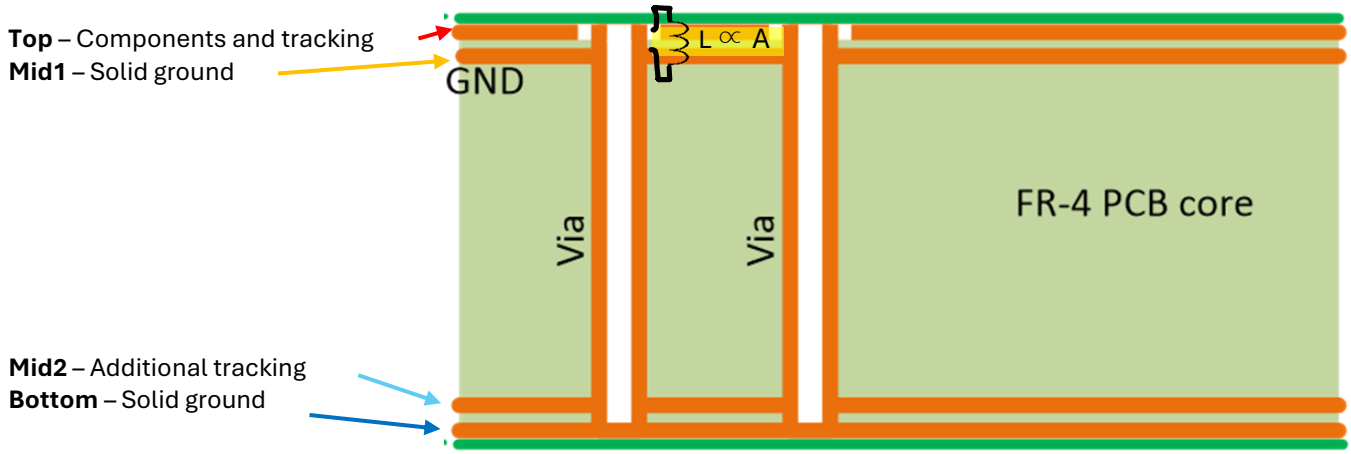

Figure 13: 4-layer PCB cross section, yellow box indicating vertical ground return loop area

In figure 12, the purple area is the ground return loop area, while in figure 13 the yellow area is the ground return loop area. The 4-layer board in figure 13 has a much smaller vertical loop area.

Figure 14 shows the difference in EMC performance between a 2-layer DDB108R1 (which has 1 routing layer and 1 solid ground plane) and a 4-layer DDB108R1 as shown in figure 4, (which has 1 routing layer and 3 solid ground planes).

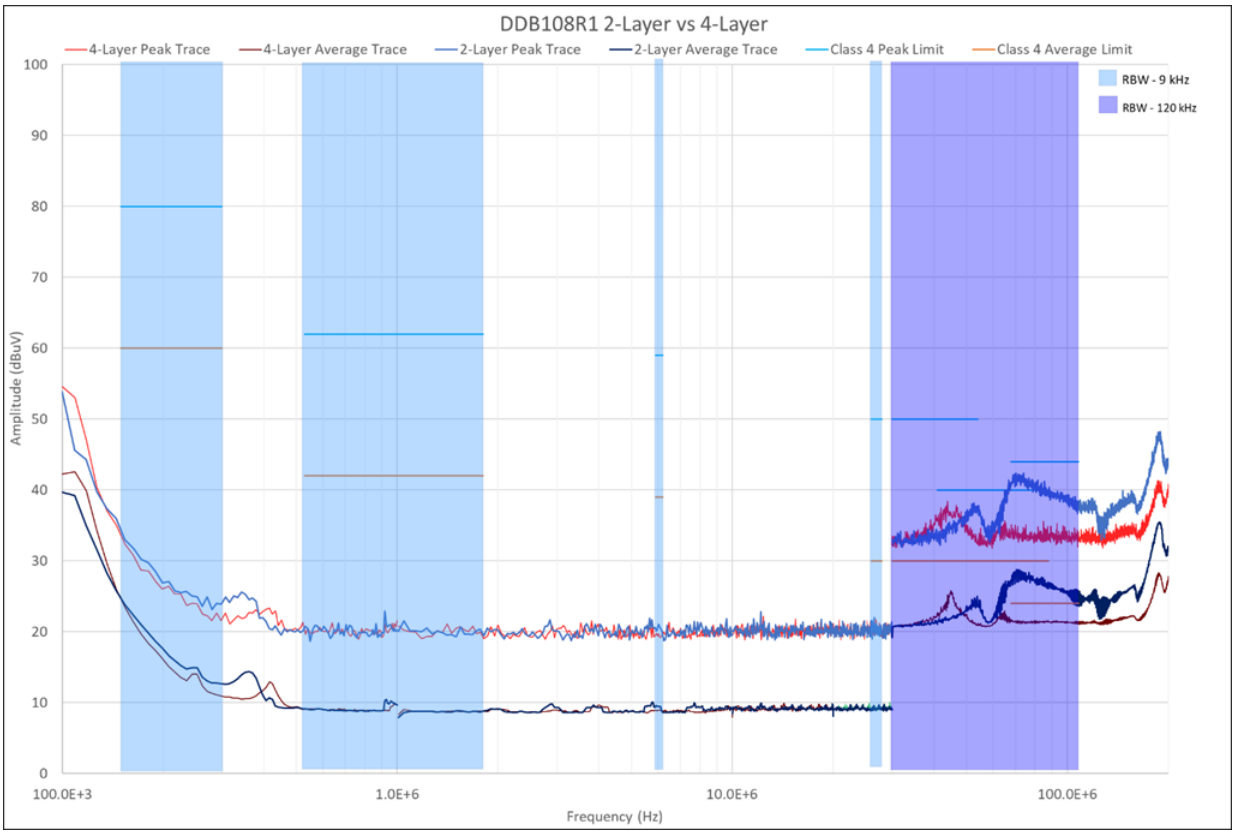

Figure 14: DDB108R1 Spectrum analyser plot, 100kHz - 200MHz, conducted emissions

As shown in figure 14, the biggest difference in EMC performance occurs in frequencies above 26MHz.

This is where the 4-layer board displays improved performance due to the minimized vertical loop area and minimized inductance in the decoupling. In this case, it is the difference between passing and failing the class 4 limits of the CISPR 25 automotive EMC standard.

Capacitor Placement and Footprint

Capacitors are essential to lowering the noise in a PCB by providing low impedance paths to ground for high-frequency noise. They have a natural frequency response as shown below in figure 15:

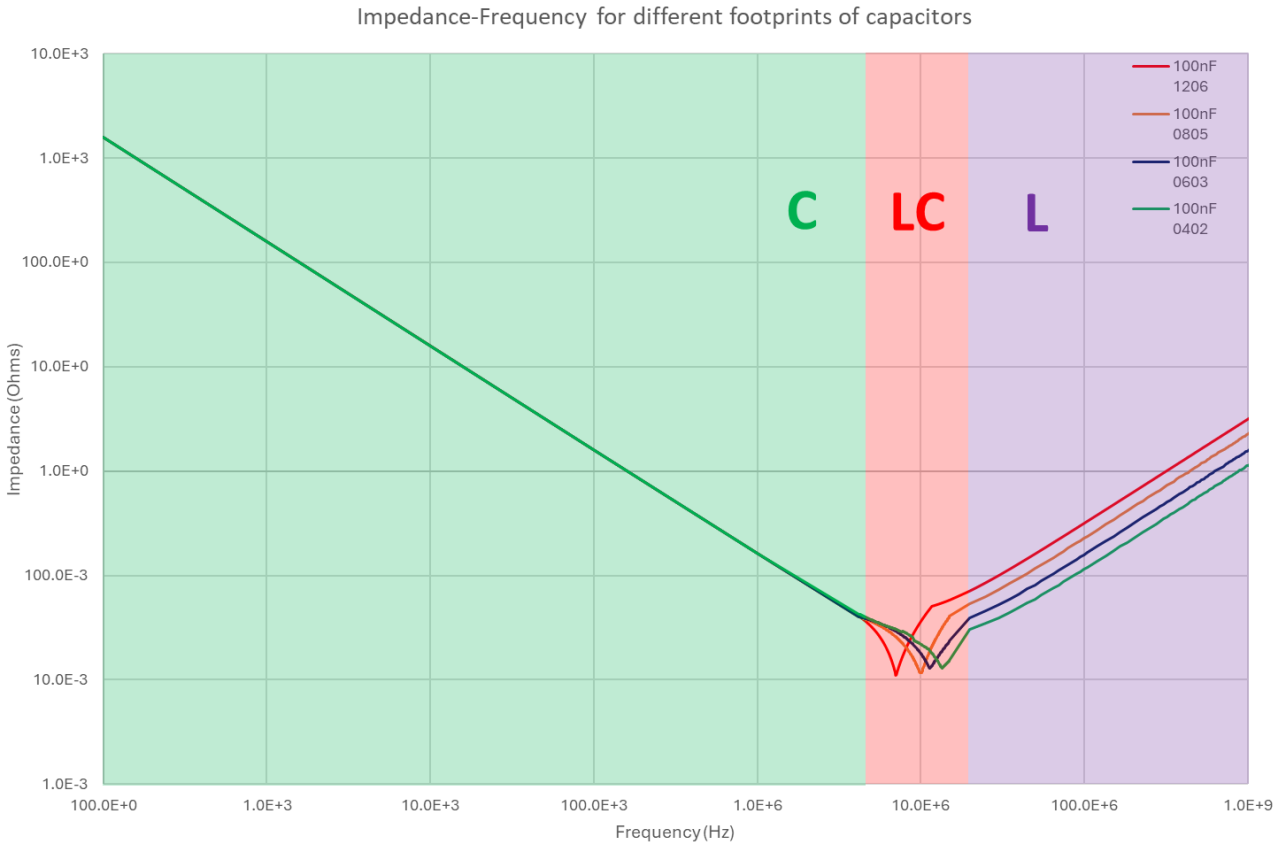

Figure 15: Example Z-F graph for different footprints of capacitors, 100kHz – 1GHz

A real capacitor is not a perfect device, and it has parasitic inductance. We can break down the impedance vs frequency into three simple regions.

1. The green region shows where the capacitance dominates. The parasitics can be ignored in this region.
2. The purple region side shows the range in which parasitic inductance dominates. The parasitic inductance is determined by the package size (all else being equal, e.g. manufacturer, material, voltage rating).
3. The red region shows the resonance of the component, determined by its combined Inductance, capacitance, and resistance.

From an EMC standpoint we are very interested in the parasitic inductance as it significantly influences the impedance at frequencies of interest (e.g. the 50MHz - 2GHz range), and physically smaller capacitors offer advantages for high-frequency decoupling.

Next is placement; placing decoupling capacitors directly in between the input/output terminals are almost essential, as shown in Figure 16 as “C21”. These capacitors should be at maximum an 0603 footprint.

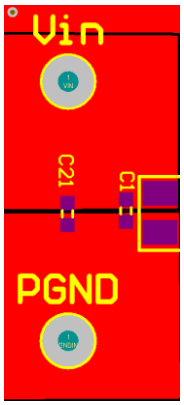

Figure 16: Input Coupling on the DDB108R2

The input track must be decoupled, as the input capacitor will reduce current spikes drawn from the input supply and the switching noise from the device.

Decoupling this pin using the stated capacitance in the datasheet for the device you are using is recommended, but it is also advisable to pair these capacitors with a smaller 0402/0201 capacitor that is directly next to the input pin and has the absolute shortest path to ground possible (as shown earlier in figure 7).

The same practice should be carried out for the output pin, pairing larger footprint capacitors with smaller footprint capacitors.

Conclusion

DC-DC devices can generate a significant amount of EMI but following these simple PCB layout guidelines can help in containing EMI and preventing it from spreading beyond the board and causing EMC issues.

A good PCB layout helps engineers reduce issues in their system design, such as harmful resonant frequencies that would be masked by the higher noise floor of an unoptimized PCB. Overall, this reduces the need for additional components and expensive countermeasures, therefore reducing system complexity and total cost.

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