Active Capacitor Discharge Circuit Considerations for FPGAs

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The multiple power rails of today's FPGAs and high-performance processors must be powered up and powered down in strict sequence. The decoupling capacitors normally attached to the power rails must be actively discharged, to ensure proper control of the power-down sequence and to complete power-down in an acceptable time. This article describes the principles and design of active discharge circuitry, and explains selection criteria for key components such as power MOSFETs to ensure repeatable performance and reliability.

Introduction

Many of today's system-on-chip FPGAs, ASICs and application processors require multiple separate power rails to supply low-voltage core logic, 3.3V or 5V I/Os, and other circuitry such as a memory bus or 1.2V Ethernet drivers. Powering up these rails in the correct sequence is known to be critical to ensure correct system operation. A power sequencer is used to enable each point-of-load (POL) converter in turn, bringing up individual power rails at the right time. It can be equally important to ensure the power-down procedure follows the reverse sequence, but the decoupling capacitors on power supply lines can prevent the system powering down correctly. Unless these capacitors are actively discharged, the charge remaining decays at an indeterminate rate after the POLs have been disabled, and so can disrupt the sequence.

Active Capacitor Discharge

The discharge time for each decoupling capacitor can be controlled using a series resistance to set the RC time constant. This enables the sequencer to turn off each POL after a known time delay following deactivation of the previous converter in the sequence. The resistor value should be selected to discharge the capacitor to 5% of its fully-charged voltage within a suitable time, avoiding excessive discharge current and noise but also allowing the sequence to be completed in an acceptable time after the signal to turn the system off has been received.

The schematic of Figure 1 illustrates a design by Diodes Inc. for active discharge using an N-channel Power MOSFET DMN3027LFG (Q2) as a switch to discharge the decoupling capacitor to ground through the resistance R2, which is chosen to achieve a suitable RC time constant. The presence of R2 also prevents sharp rising current peaks that could cause EMI issues and also transient thermal stress on both the N-channel Power MOSFET and capacitor bank.
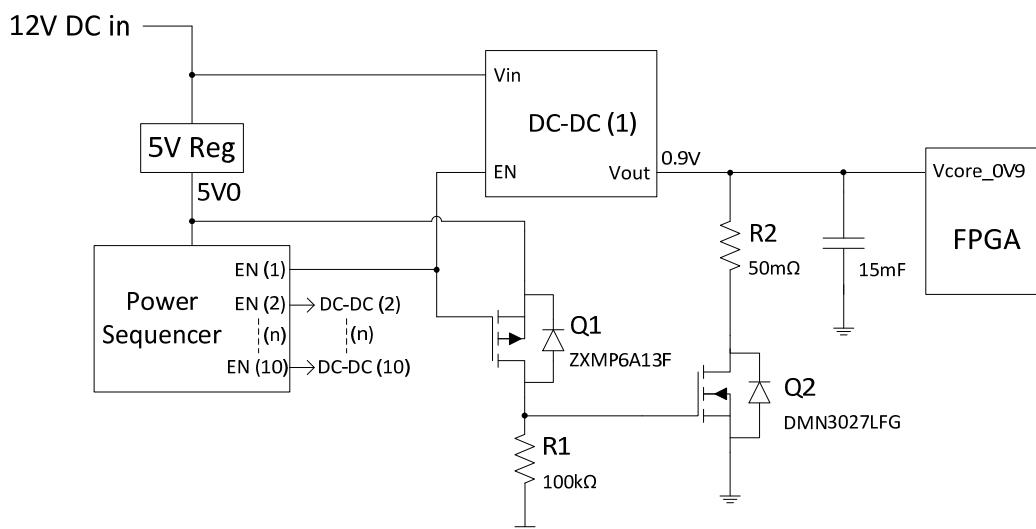

Figure 1. Active capacitor discharge is essential for correct power-down sequencing.

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In Figure 1, the power sequencer's EN output is connected to the enable pin on the DC-DC regulator, and also to the gate of the P-channel MOSFET (Q1). When the sequencer output goes low to disable the DC-DC regulator, Q1 inverts the signal thereby turning on Q2 to discharge the capacitor. The discharge circuit assumes the DC-DC regulator cannot continue producing an output once the shutdown signal is applied. If there is power available from the DC-DC regulator's output after the shutdown command is activated, Q2 will try to sink the full output current capability of the DC-DC regulator. This must be prevented by inserting a delay before the discharge circuit is activated.

Critical Component Choices
Although the active-discharge circuit is easy to implement, care is needed to select the right resistor as well as P-channel and N-channel MOSFETs, so as to minimize vulnerability to transients and overheating that can impair reliability.

The MOSFET Q1 should be selected by referring to the output voltage threshold of the power-sequencer. The selected device should have a high enough gate threshold voltage ($V_{GS(th)}$) to ensure it remains turned off when the sequencer output is high, bearing in mind that $V_{GS(th)}$ falls with increasing junction temperature. The chosen sequencer for this example operates from a 5V supply, and has minimum specified high-level output voltage of 4.19V. The $V_{GS(th)}$ of Q1 must be greater than 0.9V at the ambient operating temperature of 60°C to ensure correct operation. Moreover, the gate should be pulled down to source potential using a 100kΩ resistor to avoid false turn-on. Checking the normalised curves for $V_{GS(th)}$ versus temperature in the MOSFET datasheet shows that the Diodes Inc. ZXMP6A13F meets the requirements: the guaranteed minimum $V_{GS(th)}$ is 1V at room temperature, falling to about 0.9V at 60°C.

For the purposes of this example, we shall assume that the sequencer must turn off a total of 10 voltage rails within 100ms. Hence, the decoupling-capacitor bank on each rail must be discharged in less than 10ms. Aiming for a 3x RC time constant of 8ms ensures that the capacitor is discharged below 5% of its full voltage within the required time. To calculate the RC constant, the MOSFET $R_{DS(ON)}$, parasitic trace resistances and ESR of the capacitor bank must be considered, together with the resistor R2.

Assuming the capacitor ESR and trace resistances combined are no greater than 10mΩ, and the total decoupling bank capacitance is 15mF, suitable values for $R_{DS(ON)}$ and R2 can be calculated from the expression:

$$3 \times (10m\Omega + R2 + (1.5 \times R_{DS(ON)})) \times 15mF = 8ms$$

Assuming R2 = 50mΩ, the Power MOSFET Q2 must have $R_{DS(ON)}$ less than 80mΩ at V_{GS} = 4.5V and ambient temperature of 25˚C.

When selecting the MOSFET, the effect of temperature-related change and lot-to-lot variation of $R_{DS(ON)}$ should also be considered. $R_{DS(ON)}$ can vary by as much as 15mΩ over the expected operating temperature range at 4.5V gate drive. For this reason it is best to ensure that R2 is about double the manufacturer-specified maximum $R_{DS(ON)}$ of the chosen MOSFET. If R2 is to be 50mΩ, a MOSFET such as the Diodes Inc. DMN3027LFG N-channel MOSFET can be selected. This device has typical and maximum $R_{DS(ON)}$ of 22mΩ and 26.5mΩ respectively at V_{GS} = 4.5V, at room temperature. Hence, $R_{DS(ON)}$ can vary from about 15mΩ to 40mΩ, giving 95% (3x RC) discharge time between 3.9 to 5.4ms with a worst case capacitor bank size of 20mF.

Assessing Safe Operating Area
Because the DMN3027LFG will dissipate the capacitor's energy as a function of both current and voltage over time, it is necessary to assess the maximum single pulse that the Power MOSFET can safely handle whilst ensuring the junction temperature does not exceed the absolute maximum rating, typical $T_{J(max)}$ = 150°C. This can be seen by inspecting the Safe Operating Area (SOA) in the MOSFET datasheet (Figure 2). The SOA should be based on the application's ambient operating temperature with the required MOSFET gate drive. In the case of discharging the 0.9V charged capacitor bank, an acceptable SOA curve should indicate single-pulse peak current capability of at least 1V for pulse widths between 1ms and 10ms. The SOA should be for a typical

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application ambient temperature, which is assumed to be 60°C, whilst mounted on a PCB with minimal heat-sinking, otherwise known as minimum recommended pad (MRP) layout.
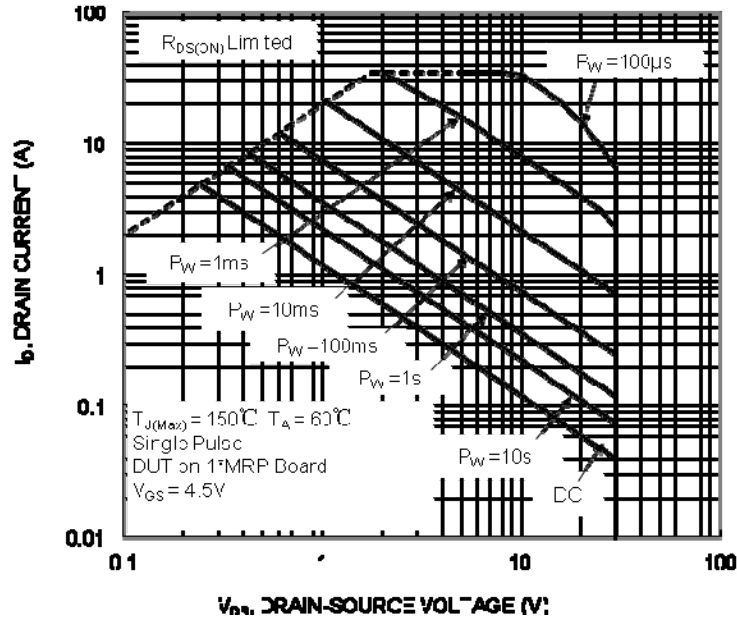

Figure 2. SOA for DMN3027LFG N-channel MOSFET.

It is also necessary to consider the power dissipation in both the DMN3027LFG (Q2) MOSFET and the series resistor R2. The worst case scenario will be caused by charging and discharging the capacitor for short periods of time. Assuming, as a worst case, that the power sequencer could enter a continuous loop enabling and then disabling the DC-DC regulator every 20ms (10ms enable + 10ms disable), about 0.5W would be dissipated across the DMN3027LFG and R2. This is calculated by knowing the total energy stored in the capacitor bank will be discharged every 20ms:

$P = E \div t = \frac{1}{2}CV^2 \div 20ms = 500mW$ (assuming C = 20mF charged to 1V)

Since the maximum temperature-adjusted $R_{DS(ON)}$ of the DMN3027LFG is 40mΩ, the power dissipation in Q2 and R2 is 222mW and 278mW, respectively. At the lowest $R_{DS(ON)}$ of 15mΩ, the power dissipation in R2 would increase to 385mW. Hence a resistor of 0.5W rating is required.

In the typical application, the ambient temperature is expected to reach 60°C and the DMN3027LFG has junction-to-ambient thermal resistance ($R_{θJA}$) 130°C/W on minimum recommended pad layout, then T_J reaches 90°C when dissipating 222mW. This gives plenty of headroom from the $T_{J(max)}$ = 150°C.

Putting Calculation Into Practice

For test purposes, a capacitor bank of six 2,200µF electrolytic capacitors (13.2mF nominal total) and an active discharge circuit, comprising the Diodes Inc. ZXMP6A13F P-channel MOSFET (Q1) and the DMN3027LFG N-channel MOSFET (Q2), was assembled according to the diagram in Figure 1. The ZXMP6A13F was manually triggered with a 5V signal.

Figure 3. Results recorded without (left) and with (right) 50mΩ series discharge resistor.

First, the capacitor bank was discharged through only the DMN3027LFG, to illustrate the effect of adding the 50mΩ resistor R2. Figure 3 shows the peak current reaches about 30A, but this will be reduced at higher temperature because the MOSFET $R_{DS(ON)}$ increases. Adding R2 limits the peak current to about 11A, and also reduces the temperature dependence of the discharge current. With the resistor in circuit, the discharge time to 95% of the initial 1V charged state occurs in 3 to 4ms, which is close to the figure calculated from theoretical values.

Conclusion

When working with complex FPGAs and System-on-Chip devices that operate from multiple power rails, it is equally important to power-down each POL in the correct order as it is to ensure the correct power-up sequence. This is necessary to prevent damage to parts of the chip. When powering-down, however, the decoupling capacitors that are essential when the system is running normally can cause turn-off times to become unpredictable. Actively discharging these capacitors to ensure each power rail is turned off within a known time enables correct and safe shutdown.

Taking the time to consider worst-case conditions and the stresses on components such as the power MOSFET switch can pay dividends by ensuring long-term reliability and minimizing dependence on environmental effects such as temperature.

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