ALM1108

µASIC

Programmable Mixed-Signal IC

Description

The ALM1108 is an ultra-small programmable µASIC featuring LUTs, logic macrocells, timers, oscillators, and more. Each macrocell within the ALM1108 contains multiple, configurable settings and initial states for maximum flexibility.

The ALM1108's macrocells are connected via hardware-defined matrix connections, not abstracted firmware. This enables asynchronous design at low power as well as more reliable operations compared to microcontrollers. Unlike a fixed ASIC, the timing and event sequences can be updated with a programming software change.

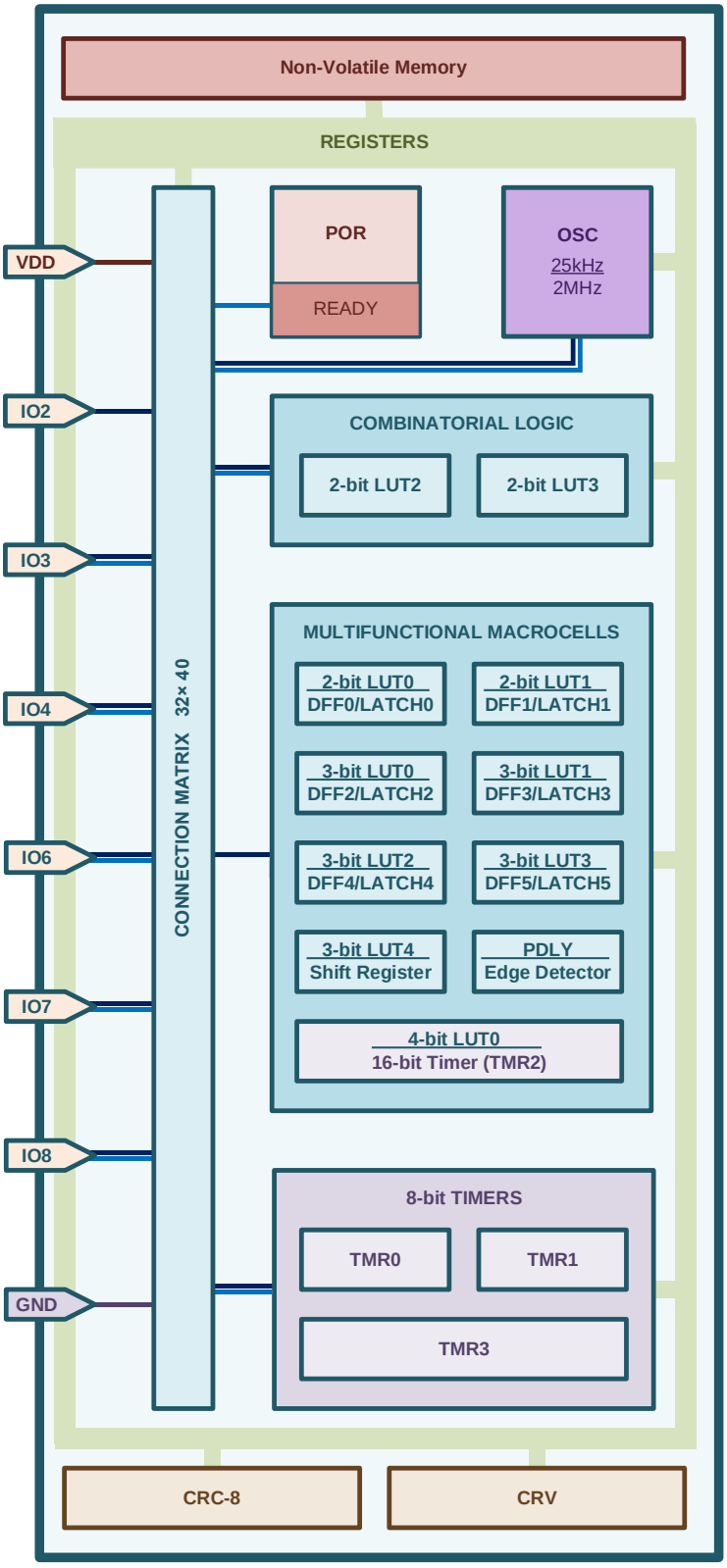
The ALM1108's functional reliability is enhanced by CRC-8 and Continuous Register Verification (CRV).

Features

- Two Operation Ranges:
  - 1.71 V to 3.60 V Supply; Operating Temperature Range: 0°C to 85°C
  - 2.10V to 3.60 V Supply; Operating Temperature Range: -40°C to 85°C
- Six Digital Inputs/Outputs
  - One Digital Input
  - Five Digital Inputs/Outputs
- Two Combinatorial 2-bit Look Up Tables (LUTs)
- Nine Multifunctional Macrocell
  - Two Selectable D Flip-Flop (DFF) / Latches or 2-bit LUTs
  - Four Selectable D Flip-Flop / Latches or 3-bit LUTs
  - One Selectable Shift Register or 3-bit LUT
    - Shift Register (SR) – 16 stage / 3 outputs
  - One Selectable 16-bit Timer with bidirectional counting (TMR) or 4-bit LUT
  - One Programmable Delay or Edge Detector
- Three 8-bit Timers with external clock/reset
- Oscillator (OSC)
- Power On Reset (POR)
- Data Protection Feature
  - CRC-8
  - Continuous Registers Verification (CRV)
- Package Options
  - 8-pin X1-QFN1012-8 (Type AX) package (1.0×1.2×0.42 mm, 0.4 mm pitch)
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen, Antimony and Beryllium Free. "Green" Device (Note 3)**
- **For automotive applications requiring specific change control (i.e. parts qualified to AEC-Q100/101/104/200, PPAP capable, and manufactured in IATF 16949 certified facilities), please contact us or your local Diodes representative. https://www.diodes.com/quality/product-definitions/**

Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen, Antimony and Beryllium-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl), <1000ppm antimony compounds and <1000ppm Beryllium.

Architecture Block Diagram



The ALM1108 (Figure 1, Table 1) has 6 multi-function I/O pins which can function as a user-defined Input or Output. Refer to Table 1 for pin definitions. For all of the 6 user-defined I/O pins on the ALM1108, the pins can serve as both Digital Input and Digital Output, except IO2 which can only serving as a Digital Input PIN.

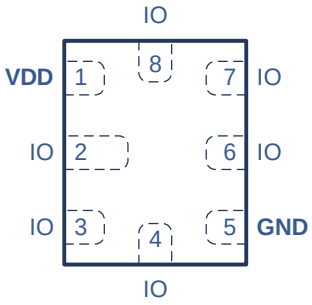


Figure 1. Top View (X1-QFN1012-8 (Type AX))

Table 1 Functional PIN Description

PIN # X1-QFN1012-8 (Type AX)	PIN Name	Function	Input Options	Output Options
1	VDD	Power Supply	--	--
2	IO2	Digital Input	Digital Input w/o Schmitt Trigger Digital Input w/ Schmitt Trigger Digital Input Low Voltage	--
3	IO3	Digital I/O	Digital Input w/o Schmitt Trigger Digital Input w/ Schmitt Trigger Digital Input Low Voltage	Push-Pull ×1 Push-Pull ×2 Open Drain NMOS ×1 Open Drain NMOS ×2 Open Drain PMOS ×1 Open Drain PMOS ×2
4	IO4	Digital I/O	Digital Input w/o Schmitt Trigger Digital Input w/ Schmitt Trigger Digital Input Low Voltage	Push-Pull ×1 Push-Pull ×2 Open Drain NMOS ×1 Open Drain NMOS ×2 Open Drain PMOS ×1 Open Drain PMOS ×2
5	GND	Ground	--	--
6	IO6	Digital I/O	Digital Input w/o Schmitt Trigger Digital Input w/ Schmitt Trigger Digital Input Low Voltage	Push-Pull ×1 Push-Pull ×2 Open Drain NMOS ×1 Open Drain NMOS ×2 Open Drain PMOS ×1 Open Drain PMOS ×2
7	IO7	Digital I/O	Digital Input w/o Schmitt Trigger Digital Input w/ Schmitt Trigger Digital Input Low Voltage	Push-Pull ×1 Push-Pull ×2 Open Drain NMOS ×1 Open Drain NMOS ×2 Open Drain PMOS ×1 Open Drain PMOS ×2
8	IO8	Digital I/O	Digital Input w/o Schmitt Trigger Digital Input w/ Schmitt Trigger Digital Input Low Voltage	Push-Pull ×1 Push-Pull ×2 Open Drain NMOS ×1 Open Drain NMOS ×2 Open Drain PMOS ×1 Open Drain PMOS ×2

Macrocell Manifest

Macrocell Name	Description	Number of Units	Total Units	Referenced Section
IOs			**6**	**5**
Digital Input	• Digital Input (low or normal voltage; with or without a Schmitt Trigger) • 10 kΩ/100 kΩ/1 MΩ Pull-Down resistors	• One Digital Input	1	5.1, 5.3, 5.6.1, 5.4
Digital Input/Output	• Digital Input (low or normal voltage; with or without a Schmitt Trigger) • Open Drain Outputs: NMOS ×1(2), PMOS ×1(2) • Push Pull Outputs: PP ×1(2) • 10 kΩ/100 kΩ/1 MΩ Pull-Up/Pull-Down resistors	• Thirteen Digital IOs	5	5.1, 5.2, 5.3, 5.6.2, 5.6.3, 5.6.4, 5.6.5, 5.6.6, 5.5
Connection Matrix			**1**	**6**
Connection Matrix	• Digital matrix connections are based on user design	• Size 32×40	1	6.1, 6.2, 6.3
Combinatorial Logic Look Up Tables			**2**	**7**
2-bit LUT	• 2-bit Look-Up Table	• Two 2-bit LUTs	2	7.1
Multifunctional Macrocells			**9**	**8**
2-bit LUT	• 2-bit Look-Up Table	• Two 2-bit LUTs shared with DFF/LATCH w/o RST	2	8.1
3-bit LUT	• 3-bit Look-Up Table	• Four 3-bit LUTs shared with DFF/LATCH w/ RST • One 3-bit LUT shared with Shift Register	5	8.2, 8.3
4-bit LUT	• 4-bit Look-Up Table	• One 4-bit LUT shared with 16-bit Timer	1	8.4
DFF w/o RST	• D Flip-Flop w/o RST	• Two DFFs shared with 2-bit LUTs or LATCHs w/o RST	2	8.1
DFF w/ RST	• D Flip-Flop w/ RST	• Four DFFs shared with 3-bit LUTs or LATCHs w/ RST	4	8.2
LATCH w/o RST	• LATCH w/o RST	• Two LATCHs shared with 2-bit LUTs or DFFs w/o RST	2	8.1
LATCH w/ RST	• LATCH w/ RST	• Four LATCHs shared with 3-bit LUTs or DFFs w/ RST	4	8.2
Shift Register	• 16 stages / 3 outputs • Two outputs with 1 to 16 selectable stages • One output with 1 stage	• One Shift Register shared with 3-bit LUT	1	8.3
16-bit TMR	• 16-bit Timer with bidirectional counting	• One 16-bit TMR shared with 4-bit LUT	1	8.4
PDLY	• Programmable Delay • 140 ns / 280 ns / 420 ns / 560 ns @ VDD = 3.3 V	• One PDLY shared with Edge Detector	1	8.5
Edge Detector	• Rising Edge Detector • Falling Edge Detector • Both Edge Detector	• One Edge Detector shared PDLY	1	8.5
8-bit Timers			**3**	**9**

8-bit TMR	• One input from the Connection Matrix for DLY IN/RST IN
	• One input from the Connection Matrix for an external couter/clock source
	• Four Modes:
	  • Delay
	  • One Shot
	  • Frequency Detector
	  • Counter
		• Two 8-bit TMR with two inputs from Connection Matrix	2	9.1, 9.3

8-bit TMR	• One input from the Connection Matrix which has a shred function of DLY IN or EXT CLK input
	• Four Modes:
	  • Delay
	  • One Shot
	  • Frequency Detector
	  • Counter
		• One 8-bit TMR with one input from Connection Matrix	1	9.4

Data Protection			**2**	**11**
CRC-8	• Validity of correct NVM programming and NVM loading	•	1	11.1
CRV	• Continuous Registers Verification	•	1	11.2
Oscillators			**1**	**12**
25kHz 2MHz	• 25 kHz or 2 MHz selectable frequency or external clock source • $CLK_{Prescaler}$: /1, /2, /4, and /8 • Out clock frequency controlled with two outputs scaled by $OUT0_{Prescaler}$ and $OUT1_{Prescaler}$: /1, /2, /4, /8, /16, /32, /64 or /128	• One OSC (25kHz/2MHz)	1	12
POR			**2**	**13**
IO2 Reset	• Reset by events of IO2	•	1	13.4

Contents

1. Application Examples

The ALM1108 is a programmable mixed-signal IC which can be configured and used for a wide array of applications. Below you can find two simple use cases for the ALM1108.

Example 1.1: Power sequencer (~40% of blocks are used)

Most of the complex electronic systems have definite power supply control to ensure that every part of the system starts up properly. This example (Figure 1.2) shows the implementation of such a system based on ALM1108. IN rising event runs the two-channel start up power supply sequence and IN falling event runs power down sequence (Figure 1.1).

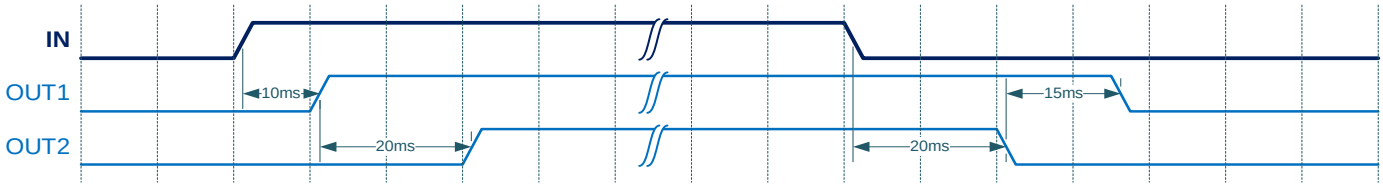


Figure 1.1. Power Sequencer requirements

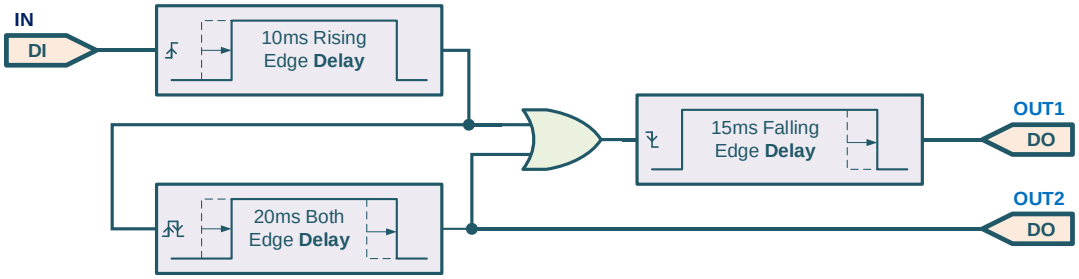


Figure 1.2. Power Sequencer implementation

Example 1.2 Watchdog timer (~35% of blocks are used)

ALM1108 allows the customer to implement a watchdog timer (Figure 1.4). If the device does not detect either rising or falling edge of IN signal during 100ms, it generates 500ms LOW pulse (Figure 1.3).

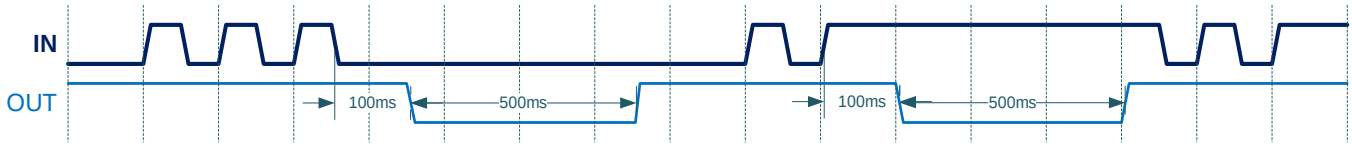


Figure 1.3. Watchdog requirements

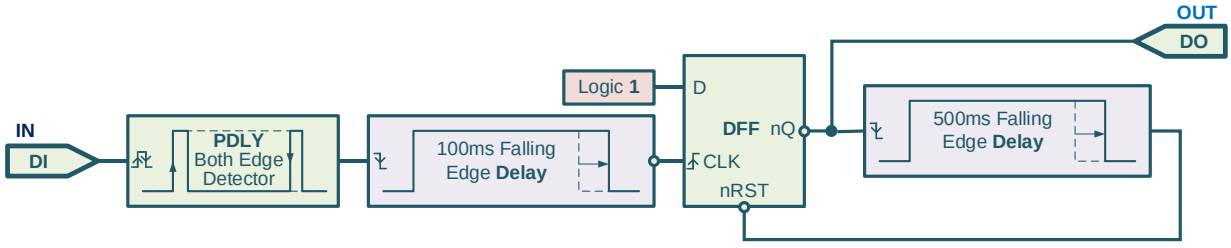


Figure 1.4. Watchdog implementation

2. How to Get Samples and Go to Production

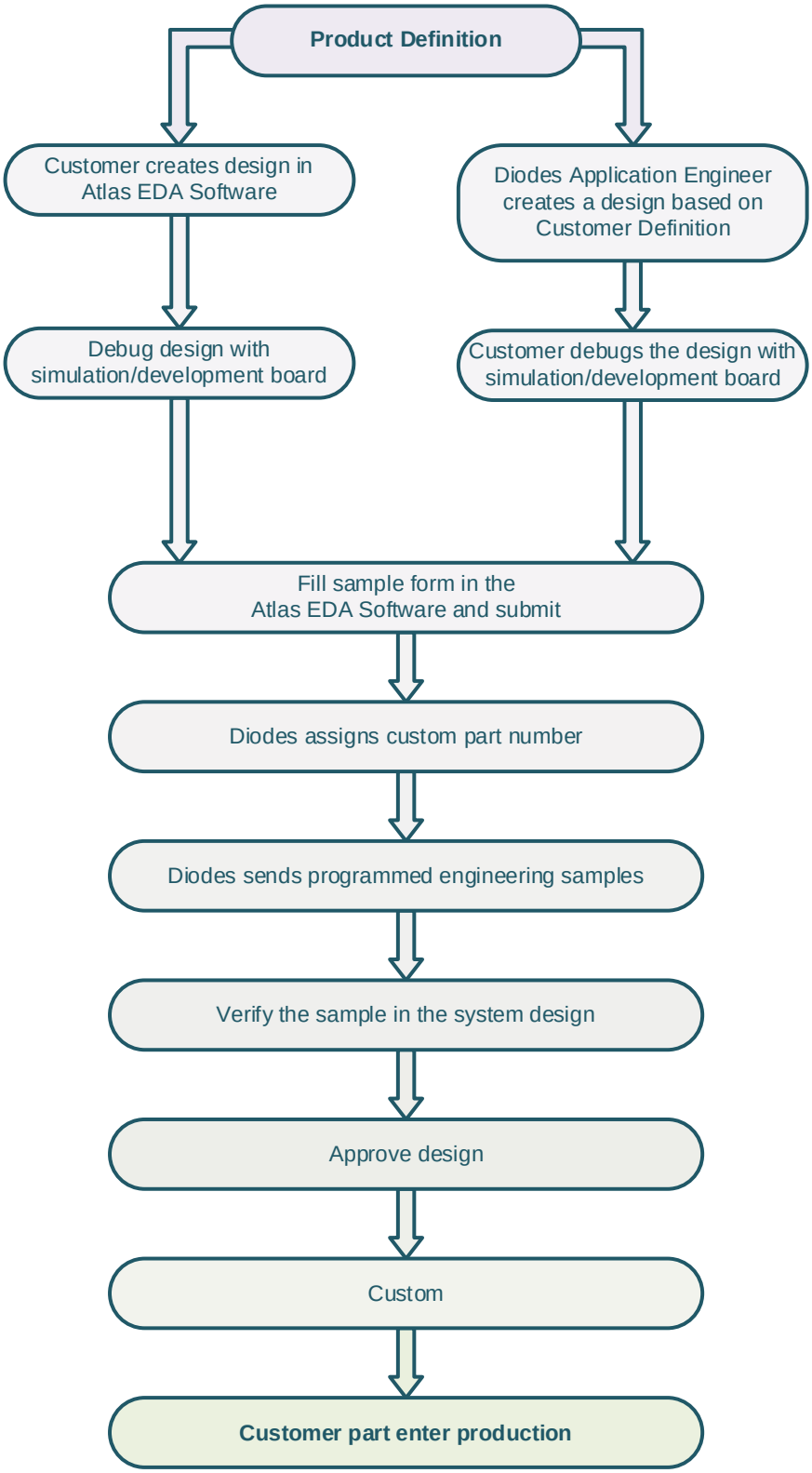


Figure 2.1. Steps to create a custom µASIC device

3. Ordering information

3.1. Ordering Information

Part Number	Package	Packing	
		Qty.	Carrier
ALM1108YB8-7	X1-QFN1012-8 (Type AX)	3,000	7” Tape and Reel

The custom program part number will be created when design is submitted.

4. Electrical Specifications

4.1. Absolute Maximum Conditions

Table 4.1. Absolute Maximum Conditions

Parameter		Min.	Max.	Unit
Supply voltage on VDD relative to GND		-0.5	7	V
DC Input voltage		GND - 0.5	VDD + 0.5	V
Maximum Average or DC Current Through VDD PIN (Per chip side, see Note 4.1)			100	mA
Maximum Average or DC Current Through GND PIN (Per chip side, see Note 4.1)			100	mA
Maximum Average or DC Current (Through pin)	PP×1	--	12	mA
	PP×2	--	17	mA
	OD(NMOS)×1	--	18	mA
	OD(NMOS)×2	--	28	mA
	OD(PMOS)×1		12	mA
	OD(PMOS)×2		17	mA
Current at Input PIN (Note 4.2)		-10.0	10.0	mA
Input leakage (Absolute Value)		--	1000	nA
Storage Temperature Range		-65	150	°C
Junction Temperature		--	150	°C
ESD Protection (Human Body Model)		2000	--	V
ESD Protection (Charged Device Model)		1300	--	V
Moisture Sensitivity Level		1		

Note 4.1 *The power rails are divided in two sides. PINs 2, 3 and 4 are connected to one side, pins 6, 7 and 8 to another*

Note 4.2 *Limiting input pin current is only necessary for input voltages that exceed absolute maximum input voltage ratings*

4.2. General Specifications

Table 4.2. General characteristics

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
T_{SU}	Startup Time	From V_{DD} rising past PON_{THR}	--	0.28	1.00	ms
PON_{THR}	Power On Threshold	V_{DD} Level Required to Start Up the Chip	--	1.6	--	V
$POFF_{THR}$	Power Off Threshold	V_{DD} Level Required to Switch Off theChip	--	1.55	--	V

4.3. IO Specifications

Table 4.3. IO Electrical Characteristics (VDD = 1.71V to 3.60V, T = 0 °C to +85 °C Unless Otherwise Noted)

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage		1.71	3.30	3.60	V
T_A	Operating Temperature		0	25	85	°C

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
V_O	Operating Voltage Applied to any PIN in HIGH-Impedance State		GND – 0.3	--	V_{DD}+0.3	V
C_{VDD}	Capacitor Value at VDD		--	0.1	--	μF
V_{IH}	HIGH-Level Input Voltage	Logic Input (Note 4.3)	0.7xV_{DD}	--	V_{DD}+0.3	V
		Logic Input with Schmitt Trigger	0.8xV_{DD}	--	V_{DD}+0.3	V
		LOW-Voltage Logic Input (Note 4.3)	1.25	--	V_{DD}+0.3	V
V_{IL}	LOW-Level Input Voltage	Logic Input (Note 4.3)	GND-0.3	--	0.3xV_{DD}	V
		Logic Input with Schmitt Trigger	GND-0.3	--	0.2xV_{DD}	V
		LOW-Voltage Logic Input (Note 4.3)	GND-0.3	--	0.5	V
V_{HYS}	Schmitt Trigger Hysteresis Voltage	Logic Input with Schmitt Trigger	--	0.5	--	V
V_{OH}	HIGH-Level Output Voltage	Push-Pull ×1, Open Drain PMOS ×1, I_{OH} = 100 μA, V_{DD} = 1.8 V	1.770	1.790	--	V
		Push-Pull ×2, Open Drain PMOS ×2, I_{OH} = 100 μA, V_{DD} = 1.8 V	1.780	1.800	--	V
		Push-Pull ×1, Open Drain PMOS ×1, I_{OH} = 3 mA, V_{DD} = 2.1 V	1.590	1.760	--	V
		Push-Pull ×2, Open Drain PMOS ×2, I_{OH} = 3 mA, V_{DD} = 2.1 V	1.850	1.950	--	V
		Push-Pull ×1, Open Drain PMOS ×1, I_{OH} = 3 mA, V_{DD} = 3.3 V	2.980	3.120	--	V
		Push-Pull ×2, Open Drain PMOS ×2, I_{OH} = 3 mA, V_{DD} = 3.3 V	3.140	3.210	--	V
V_{OL}	LOW-Level Output Voltage	Push-Pull ×1, I_{OL} = 100 μA, V_{DD} = 1.8 V	--	0.008	0.017	V
		Push-Pull ×2, I_{OL} = 100 μA, V_{DD} = 1.8 V	--	0.004	0.007	V
		Push-Pull ×1, I_{OL} = 3 mA, V_{DD} = 2.1 V	--	0.210	0.320	V
		Push-Pull ×2, I_{OL} = 3 mA, V_{DD} = 2.1 V	--	0.110	0.160	V
		Push-Pull ×1, I_{OL} = 3 mA, V_{DD} = 3.3 V	--	0.128	0.260	V
		Push-Pull ×2, I_{OL} = 3 mA, V_{DD} = 3.3 V	--	0.063	0.130	V
		Open Drain NMOS ×1, I_{OL} = 100 μA, V_{DD} = 1.8 V	--	0.004	0.007	V
		Open Drain NMOS ×2, I_{OL} = 100 μA, V_{DD} = 1.8 V	--	0.002	0.005	V
		Open Drain NMOS ×1, I_{OL} = 100 μA, V_{DD} = 2.1 V	--	0.110	0.170	V
		Open Drain NMOS ×2, I_{OL} = 100 μA, V_{DD} = 2.1 V	--	0.055	0.090	V
		Open Drain NMOS ×1, I_{OL} = 3 mA, V_{DD} = 3.3 V	--	0.063	0.130	V
		Open Drain NMOS ×2, I_{OL} = 3 mA, V_{DD} = 3.3 V	--	0.032	0.070	V
I_{OH}	HIGH-Level Output Current (see Note 4.4)	Push-Pull ×1, Open Drain PMOS ×1, V_{OH} = VDD - 0.2, V_{DD} = 1.8 V	1.000	1.500	--	mA
		Push-Pull ×2, Open Drain PMOS ×2, V_{OH} = VDD - 0.2, V_{DD} = 1.8 V	2.000	2.980	--	mA
		Push-Pull ×1, Open Drain PMOS ×1, V_{OH} = 2.4 V, V_{DD} = 2.1 V	1.300	1.800	--	mA
		Push-Pull ×2, Open Drain PMOS ×2, V_{OH} = 2.4 V, V_{DD} = 2.1 V	2.800	3.700	--	mA
		Push-Pull ×1, Open Drain PMOS ×1, V_{OH} = 2.4 V, V_{DD} = 3.3 V	5.700	11.000	--	mA
		Push-Pull ×2, Open Drain PMOS ×2, V_{OH} = 2.4 V, V_{DD} = 3.3 V	11.300	21.700	--	mA

I_{OL}	LOW-Level Output Current (see Note 4.4)	Push-Pull ×1, V_{OL} = 0.15 V, V_{DD} = 1.8 V	1.000	1.500	--	mA
		Push-Pull ×2, V_{OL} = 0.15 V, V_{DD} = 1.8 V	2.000	3.000	--	mA
		Open Drain NMOS ×1, V_{OL} = 0.15 V, V_{DD} = 1.8 V	2.000	2.700	--	mA
		Open Drain NMOS ×2, V_{OL} = 0.15 V, V_{DD} = 1.8 V	4.000	5.400	--	mA
		Push-Pull ×1, V_{OL} = 0.4 V, V_{DD} = 2.1 V	3.100	4.500	--	mA
		Push-Pull ×2, V_{OL} = 0.4 V, V_{DD} = 2.1 V	7.000	9.100	--	mA
		Open Drain NMOS ×1, V_{OL} = 0.4 V, V_{DD} = 2.1 V	7.000	9.100	--	mA
		Open Drain NMOS ×2, V_{OL} = 0.4 V, V_{DD} = 2.1 V	14.100	18.200	--	mA
		Push-Pull ×1, V_{OL} = 0.4 V, V_{DD} = 3.3 V	4.400	8.500	--	mA
		Push-Pull ×2, V_{OL} = 0.4 V, V_{DD} = 3.3 V	9.100	16.900	--	mA
		Open Drain NMOS ×1, V_{OL} = 0.4 V, V_{DD} = 3.3 V	9.200	16.900	--	mA
		Open Drain NMOS ×2, V_{OL} = 0.4 V, V_{DD} = 3.3 V	17.900	33.400	--	mA
R_{PULL}	Pull-Up or Pull-Down Resistance	1000 kΩ; For Pull-Up V_{IN} = GND; For Pull-Down V_{IN} = V_{DD}	--	1000	--	kΩ
		100 kΩ; For Pull-Up V_{IN} = GND; For Pull-Down V_{IN} = V_{DD}	--	100	--	kΩ
		10 kΩ; For Pull-Up V_{IN} = GND; For Pull-Down V_{IN} = V_{DD}	--	10	--	kΩ
C_{IN}	Input Capacitance		--	4	--	pF

Note 4.3 No hysteresis
Note 4.4 DC or average current through any pin should not exceed value given in Absolute Maximum Conditions

Table 4.4. IO Electrical Characteristics (VDD = 2.1V to 3.60V, T = -40 °C to +85 °C Unless Otherwise Noted)

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage		1.71	3.30	3.60	V
T_A	Operating Temperature		0	25	85	°C
V_O	Operating Voltage Applied to any PIN in HIGH-Impedance State		GND – 0.3	--	V_{DD}+0.3	V
C_{VDD}	Capacitor Value at VDD		--	0.1	--	µF
V_{IH}	HIGH-Level Input Voltage	Logic Input (Note 4.3)	0.7xV_{DD}	--	V_{DD}+0.3	V
		Logic Input with Schmitt Trigger	0.8xV_{DD}	--	V_{DD}+0.3	V
		LOW-Voltage Logic Input (Note 4.3)	1.25	--	V_{DD}+0.3	V
V_{IL}	LOW-Level Input Voltage	Logic Input (Note 4.3)	GND-0.3	--	0.3xV_{DD}	V
		Logic Input with Schmitt Trigger	GND-0.3	--	0.2xV_{DD}	V
		LOW-Voltage Logic Input (Note 4.3)	GND-0.3	--	0.5	V
V_{HYS}	Schmitt Trigger Hysteresis Voltage	Logic Input with Schmitt Trigger	--	0.5	--	V
V_{OH}	HIGH-Level Output Voltage	Push-Pull ×1, Open Drain PMOS ×1, I_{OH} = 3 mA, V_{DD} = 2.1 V	1.590	1.760	--	V
		Push-Pull ×2, Open Drain PMOS ×2, I_{OH} = 3 mA, V_{DD} = 2.1 V	1.850	1.950	--	V
		Push-Pull ×1, Open Drain PMOS ×1, I_{OH} = 3 mA, V_{DD} = 3.3 V	2.980	3.120	--	V
		Push-Pull ×2, Open Drain PMOS ×2, I_{OH} = 3 mA, V_{DD} = 3.3 V	3.140	3.210	--	V

V_{OL}	LOW-Level Output Voltage	Push-Pull ×1, I_{OL} = 3 mA, V_{DD} = 2.1 V	--	0.210	0.320	V
		Push-Pull ×2, I_{OL} = 3 mA, V_{DD} = 2.1 V	--	0.110	0.160	V
		Push-Pull ×1, I_{OL} = 3 mA, V_{DD} = 3.3 V	--	0.128	0.260	V
		Push-Pull ×2, I_{OL} = 3 mA, V_{DD} = 3.3 V	--	0.063	0.130	V
		Open Drain NMOS ×1, I_{OL} = 100 µA, V_{DD} = 2.1 V	--	0.110	0.170	V
		Open Drain NMOS ×2, I_{OL} = 100 µA, V_{DD} = 2.1 V	--	0.055	0.090	V
		Open Drain NMOS ×1, I_{OL} = 3 mA, V_{DD} = 3.3 V	--	0.063	0.130	V
		Open Drain NMOS ×2, I_{OL} = 3 mA, V_{DD} = 3.3 V	--	0.032	0.070	V
I_{OH}	HIGH-Level Output Current (see Note 4.4)	Push-Pull ×1, Open Drain PMOS ×1, V_{OH} = 2.4 V, V_{DD} = 2.1 V	1.300	1.800	--	mA
		Push-Pull ×2, Open Drain PMOS ×2, V_{OH} = 2.4 V, V_{DD} = 2.1 V	2.800	3.700	--	mA
		Push-Pull ×1, Open Drain PMOS ×1, V_{OH} = 2.4 V, V_{DD} = 3.3 V	5.700	11.000	--	mA
		Push-Pull ×2, Open Drain PMOS ×2, V_{OH} = 2.4 V, V_{DD} = 3.3 V	11.300	21.700	--	mA
I_{OL}	LOW-Level Output Current (see Note 4.4)	Push-Pull ×1, V_{OL} = 0.4 V, V_{DD} = 2.1 V	3.100	4.500	--	mA
		Push-Pull ×2, V_{OL} = 0.4 V, V_{DD} = 2.1 V	7.000	9.100	--	mA
		Open Drain NMOS ×1, V_{OL} = 0.4 V, V_{DD} = 2.1 V	7.000	9.100	--	mA
		Open Drain NMOS ×2, V_{OL} = 0.4 V, V_{DD} = 2.1 V	14.100	18.200	--	mA
		Push-Pull ×1, V_{OL} = 0.4 V, V_{DD} = 3.3 V	4.400	8.500	--	mA
		Push-Pull ×2, V_{OL} = 0.4 V, V_{DD} = 3.3 V	9.100	16.900	--	mA
		Open Drain NMOS ×1, V_{OL} = 0.4 V, V_{DD} = 3.3 V	9.200	16.900	--	mA
		Open Drain NMOS ×2, V_{OL} = 0.4 V, V_{DD} = 3.3 V	17.900	33.400	--	mA
R_{PULL}	Pull-Up or Pull-Down Resistance	1000 kΩ; For Pull-Up V_{IN} = GND; For Pull-Down V_{IN} = V_{DD}	--	1000	--	kΩ
		100 kΩ; For Pull-Up V_{IN} = GND; For Pull-Down V_{IN} = V_{DD}	--	100	--	kΩ
		10 kΩ; For Pull-Up V_{IN} = GND; For Pull-Down V_{IN} = V_{DD}	--	10	--	kΩ
C_{IN}	Input Capacitance		--	4	--	pF
Note 4.5	*No hysteresis*					
Note 4.6	*DC or average current through any pin should not exceed value given in Absolute Maximum Conditions*					

4.4. Typical Current Consumption

Table 4.5. Typical Current Estimated for Each Macrocell

Symbol	Parameter	Note	VDD = 1.8 V	VDD = 2.1 V	VDD = 3.3 V	Unit
I_{DD}	Current	Chip Quiescent	0.18	0.21	0.36	µA
		OSC 2 MHz, PreScaler = 1	34.60	47.00	89.50	µA
		OSC 25 kHz, PreScaler = 1	0.77	0.98	3.00	µA

4.5. Timing Estimator

Table 4.6 Typical Propagation Time (t_{PROP}) for Each Macrocell

Start Point	End point	Note	VDD = 1.8 V		VDD = 3.3 V		Unit
			Low to High	High to Low	Low to High	High to Low	
DI w/o ST	DO PP×1	IO	42.5	49.6	14.9	18.1	ns
DI w/o ST	DO PP×2	IO	38.6	46.3	13.9	17.4	ns
DI w/ ST	DO PP×1	IO	43.0	50.1	15.7	18.7	ns
DI LV	DO PP×1	IO	40.3	61.5	13.2	22.0	ns
DI LV	DO PP×2	IO	36.4	58.2	11.8	21.1	ns
DI w/o ST	DO NMOS×1	IO	--	44.1	--	16.2	ns
DI w/o ST	DO NMOS×2	IO	--	42.6	--	15.6	ns
DI w/o ST	DO PMOS×1	IO	39.4	--	13.8	--	ns
DI w/o ST	DO PMOS×2	IO	37.4	--	12.8	--	ns
IN	OUT	2-bit LUT	16.6	20.7	6.0	7.1	ns
IN	OUT	3-bit LUT	20.9	23.9	7.7	8.5	ns
IN	OUT0	3-bit LUT	23.4	26.8	8.7	9.6	ns
IN	OUT1	3-bit LUT	22.9	26.0	8.5	9.3	ns
IN	OUT	4-bit LUT	22.9	27.1	8.3	9.7	ns
CLK	Q	DFF w/o nRST(nSET)	26.6	32.1	7.6	9.1	ns
CLK	nQ	DFF w/o nRST(nSET)	26.8	32.3	7.7	9.0	ns
CLK	Q	DFF w/ nRST(nSET)	32.5	38.0	9.5	10.8	ns
nRST	Q	DFF w/ nRST	--	33.7	--	10.2	ns
nSET	Q	DFF w/ nSET	29.6	--	8.7	--	ns
CLK	nQ	DFF w/ nRST(nSET)	31.9	40.3	9.5	11.3	ns
nRST	nQ	DFF w/ nRST	28.6	--	8.8	--	ns
nSET	nQ	DFF w/ nSET	--	38.0	--	11.2	ns
D	Q	LATCH w/o nRST(nSET)	26.2	29.3	7.5	8.8	ns
CLK	Q	LATCH w/o nRST(nSET)	23.8	28.4	7.1	8.6	ns
D	nQ	LATCH w/o nRST(nSET)	23.3	32.5	7.0	9.2	ns
CLK	nQ	LATCH w/o nRST(nSET)	23.1	30.5	7.0	8.9	ns
D	Q	LATCH w/ nRST(nSET)	31.3	32.6	9.0	9.7	ns
CLK	Q	LATCH w/ nRST(nSET)	28.2	32.8	8.4	9.7	ns
nRST	Q	LATCH w/ nRST	35.3	36.0	10.3	10.8	ns
nSET	Q	LATCH w/ nSET	28.1	40.3	8.8	12.1	ns
D	nQ	LATCH w/ nRST(nSET)	27.2	39.7	8.4	11.3	ns
CLK	nQ	LATCH w/ nRST(nSET)	26.7	35.7	8.3	10.5	ns
nRST	nQ	LATCH w/ nRST	32.1	44.3	9.6	13.1	ns
nSET	nQ	LATCH w/ nSET	35.6	36.8	11.1	11.4	ns
CLK	OUT0	Shift register	34.1	43.1	10.3	12.2	ns
CLK	OUT1	Shift register	36.1	45.6	11.0	13.2	ns
CLK	Q[1]	Shift register	29.0	34.2	8.7	10.1	ns
CLK	nOUT1	Shift register	39.4	44.0	11.8	13.0	ns
nRST	OUT0	Shift register	--	39.5	--	11.4	ns
nRST	OUT1	Shift register	--	41.6	--	12.0	ns
nRST	Q[1]	Shift register	--	29.5	--	8.9	ns
nRST	nOUT1	Shift register	35.7	--	10.6	--	ns
IN	OUT	PDLY / Edge Detector	32.9	33.0	8.9	7.8	ns
IN	OUT	8-bit TMR (Delay)	37.0	42.2	10.4	11.9	ns
IN	OUT	8-bit TMR (One-Shot)	48.3	45.4	14.6	13.6	ns
IN	OUT	8-bit TMR (Counter)	58.3	60.5	17.0	17.8	ns
IN	OUT	8-bit TMR (Frequency Detector)	54.2	48.8	15.5	14.6	ns
IN	OUT	8-bit TMR (Edge Detector)	39.3	35.6	11.6	10.5	ns
CLK	OUT	8-bit TMR (Delay)	54.4	58.0	15.4	16.8	ns
CLK	OUT	8-bit TMR (One-Shot)	--	54.9	--	16.0	ns
CLK	OUT	8-bit TMR (Counter)	36.8	35.9	10.7	10.2	ns
CLK	OUT	8-bit TMR (Frequency Detector)	--	121.4	--	34.3	ns
IN	OUT	16-bit TMR (Delay)	54.9	53.3	15.5	15.4	ns
IN	OUT	16-bit TMR (One-Shot)	64.4	54.4	19.6	16.3	ns
IN	OUT	16-bit TMR (Counter)	52.2	102.2	15.4	29.4	ns
IN	OUT	16-bit TMR (Frequency Detector)	69.2	60.9	20.5	18.0	ns
CLK	OUT	16-bit TMR (Delay)	82.2	92.8	23.4	27.0	ns

Start Point	End point	Note	VDD = 1.8 V		VDD = 3.3 V		Unit
			Low to High	High to Low	Low to High	High to Low	
CLK	OUT	16-bit TMR (One-Shot)	--	87.2	--	25.0	ns
CLK	OUT	16-bit TMR (Counter)	62.5	66.3	18.1	19.7	ns
CLK	OUT	16-bit TMR (Frequency Detector)	--	156.5	--	44.1	ns

Table 4.7 Expected Delays and Widths for Programmable Delay/Edge Detector

Symbol	Parameter	Note	V_{DD} = 1.8V	V_{DD} = 3.3V	Unit
T_{Width}	Width, 1 cell	Mode:(any)Edge Detect, Edge Detect Output	210.00	165.60	ns
T_{Width}	Width, 2 cells	Mode:(any)Edge Detect, Edge Detect Output	299.80	311.20	ns
T_{Width}	Width, 3 cells	Mode:(any)Edge Detect, Edge Detect Output	386.40	454.20	ns
T_{Width}	Width, 4 cells	Mode:(any)Edge Detect, Edge Detect Output	475.50	598.80	ns
T_{PROP}	Delay, 1 cell	Mode:(any)Edge Detect, Edge Detect Output	32.90	8.90	ns
T_{PROP}	Delay, 2 cells	Mode:(any)Edge Detect, Edge Detect Output	33.67	8.90	ns
T_{PROP}	Delay, 3 cells	Mode:(any)Edge Detect, Edge Detect Output	33.10	8.90	ns
T_{PROP}	Delay, 4 cells	Mode:(any)Edge Detect, Edge Detect Output	33.60	8.80	ns
T_{DLY}	Delay, 1 cell	Mode: Both Edge Delay, Edge Detect Output	296.10	193.59	ns
T_{DLY}	Delay, 2 cells	Mode: Both Edge Delay, Edge Detect Output	590.00	412.50	ns
T_{DLY}	Delay, 3 cells	Mode: Both Edge Delay, Edge Detect Output	854.00	618.50	ns
T_{DLY}	Delay, 4 cells	Mode: Both Edge Delay, Edge Detect Output	1098.29	820.59	ns

4.6. OSC Specifications

4.6.1. 25 kHz Oscillator

Table 4.8 25 kHz OSC Frequency Limits

Power Supply Range V_{DD}, V	Temperature Range					
	+25 °C		0 °C ... +85 °C		-40 °C ... +85 °C	
	Min, kHz	Max, kHz	Min, kHz	Max, kHz	Min, kHz	Max, kHz
1.8 V ±5%	23.590	26.290	23.200	26.400	-	-
3.3 V ±10%	24.210	25.760	24.090	25.970	23.780	26.310
2.1 V…3.60 V	23.030	29.570	22.770	30.180	21.280	31.500
2.5 V…3.60 V	24.200	26.580	24.080	27.480	23.830	29.490
1.71V…3.60 V	20.400	29.580	20.010	30.210	-	-

Table 4.9 25 kHz OSC Frequency Error (Error Calculated Relative to Nominal Value)

Power Supply Range V_{DD}, V	Temperature Range					
	+25 °C		0 °C ... +85 °C		-40 °C ... +85 °C	
	Min	Max	Min	Max	Min	Max
1.8 V ±5%	-5.64%	5.16%	-7.20%	5.60%	-	-
3.3 V ±10%	-3.16%	3.04%	-3.64%	3.88%	-4.88%	5.24%
2.1 V…3.60 V	-7.88%	18.28%	-8.92%	20.72%	-14.88%	26.00%
2.5 V…3.60 V	-3.20%	6.32%	-3.68%	9.92%	-4.68%	17.96%
1.71V…3.60 V	-18.40%	18.32%	-19.96%	20.84%	-	-

Table 4.10 25 kHz OSC Power On Delay at Room Temperature

Power Supply Range V_{DD}, V	T_{POD}, us	
	Typ	Max
1.71	18.00	41.00
1.80	18.00	41.00
3.30	15.00	41.00
3.60	15.00	41.00

Table 4.11 25 kHz OSC Frequency Settling Time

Parameter	Typ	Max	Unit
Frequency Settling Time	2	10	Cycles

Note 4.7 The OSC frequency error during settling time is less than 10%

4.6.2. 2 MHz Oscillator

Table 4.12 2 MHz OSC Frequency Limits

Power Supply Range V_{DD}, V	Temperature Range					
	+25 °C		0 °C ... +85 °C		-40 °C ... +85 °C	
	Min, MHz	Max, MHz	Min, MHz	Max, MHz	Min, MHz	Max, MHz
1.8 V ±5%	1.300	2.120	1.150	2.400	-	-
3.3 V ±10%	1.790	2.310	1.610	2.530	1.540	2.550
2.1 V…3.60 V	1.490	2.300	1.450	2.610	1.430	2.620
2.5 V…3.60 V	1.700	2.310	1.540	2.550	1.510	2.680
1.71V…3.60 V	1.170	2.400	1.160	2.640	-	-

Table 4.13 2 MHz OSC Frequency Error (Error Calculated in Relation to Nominal Value)

Power Supply Range V_{DD}, V	Temperature Range					
	+25 °C		0 °C ... +85 °C		-40 °C ... +85 °C	
	Min	Max	Min	Max	Min	Max
1.8 V ±5%	-35.00%	6.00%	-42.50%	20.00%	-	-
3.3 V ±10%	-10.50%	15.50%	-19.50%	26.50%	-23.00%	27.50%
2.1 V…3.60 V	-25.50%	15.00%	-27.50%	30.50%	-28.50%	31.00%
2.5 V…3.60 V	-15.00%	15.50%	-23.00%	27.50%	-24.50%	34.00%
1.71V…3.60 V	-41.50%	20.00%	-42.00%	32.00%	-	-

Table 4.14 2 MHz OSC Power On Delay at Room Temperature

Power Supply Range V_{DD}, V	T_{POD}, us	
	Typ	Max
1.71	0.410	0.500
1.80	0.380	0.500
2.10	0.310	0.500
3.30	0.260	0.500

Table 4.15 2 MHz OSC Frequency Settling Time

Parameter	Typ	Max	Unit
Frequency Settling Time	9	11	Cycles

Note 4.8 The OSC frequency error during settling time is less than 10%

5. I/O PINs

5.1. Input Modes

Each of the IOs can be configured as a Digital Input with or without a buffered Schmitt trigger, or they can also be configured as a Digital Input Low Voltage.

5.2. Output Modes

All IOs except IO2 can be configurable as digital outputs.

5.3. Pull Up/Down Resistors

All IOs have an option for user-selectable resistors connected to the input structure, with the selectable values being 10 kΩ, 100 kΩ, and 1 MΩ. In the case of IO2, the resistors are fixed to a pull-down configuration. In the case of all other I/O pins, the internal resistors can be configured as pull-up or pull-downs.

5.4. IO Structure (for IO2)

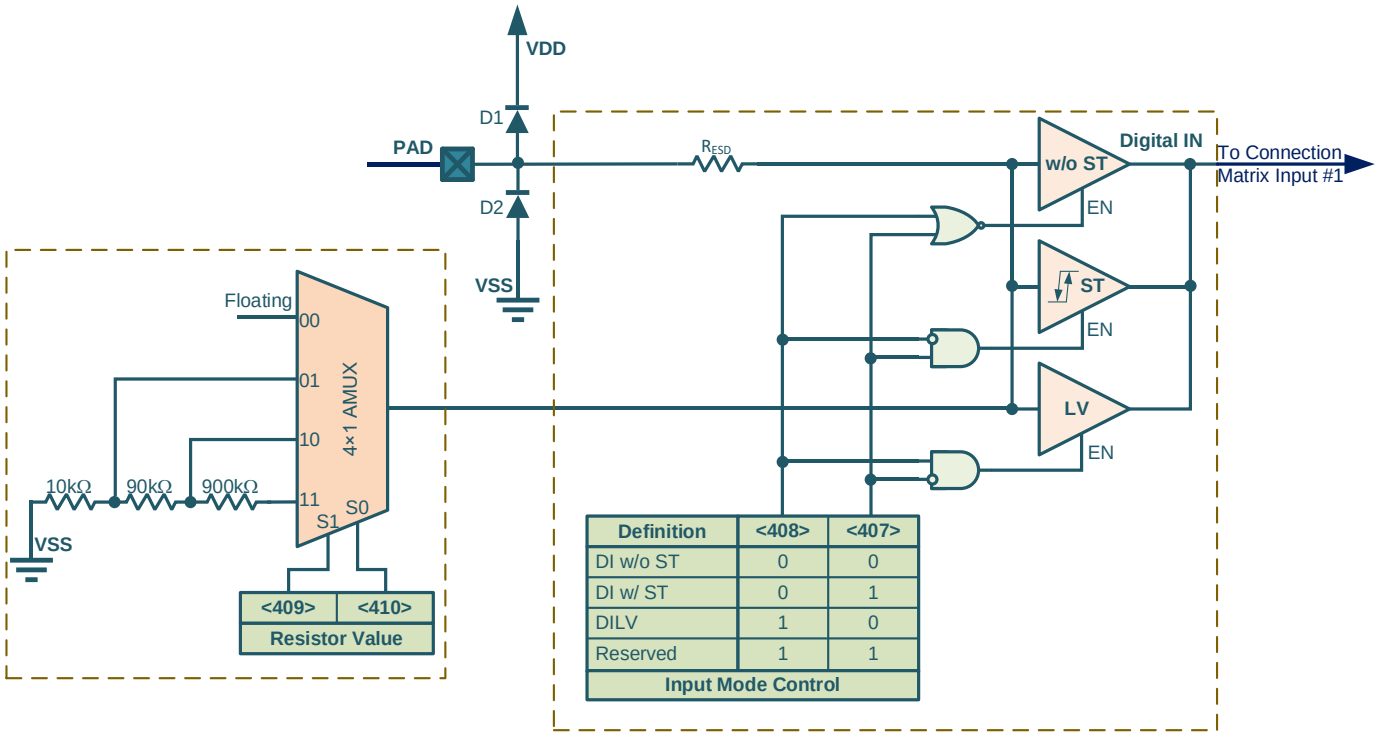


Figure 5.1. IO2 Structure Diagram

5.5. IO Structure (for IO3, IO4, IO6, IO7, IO8)

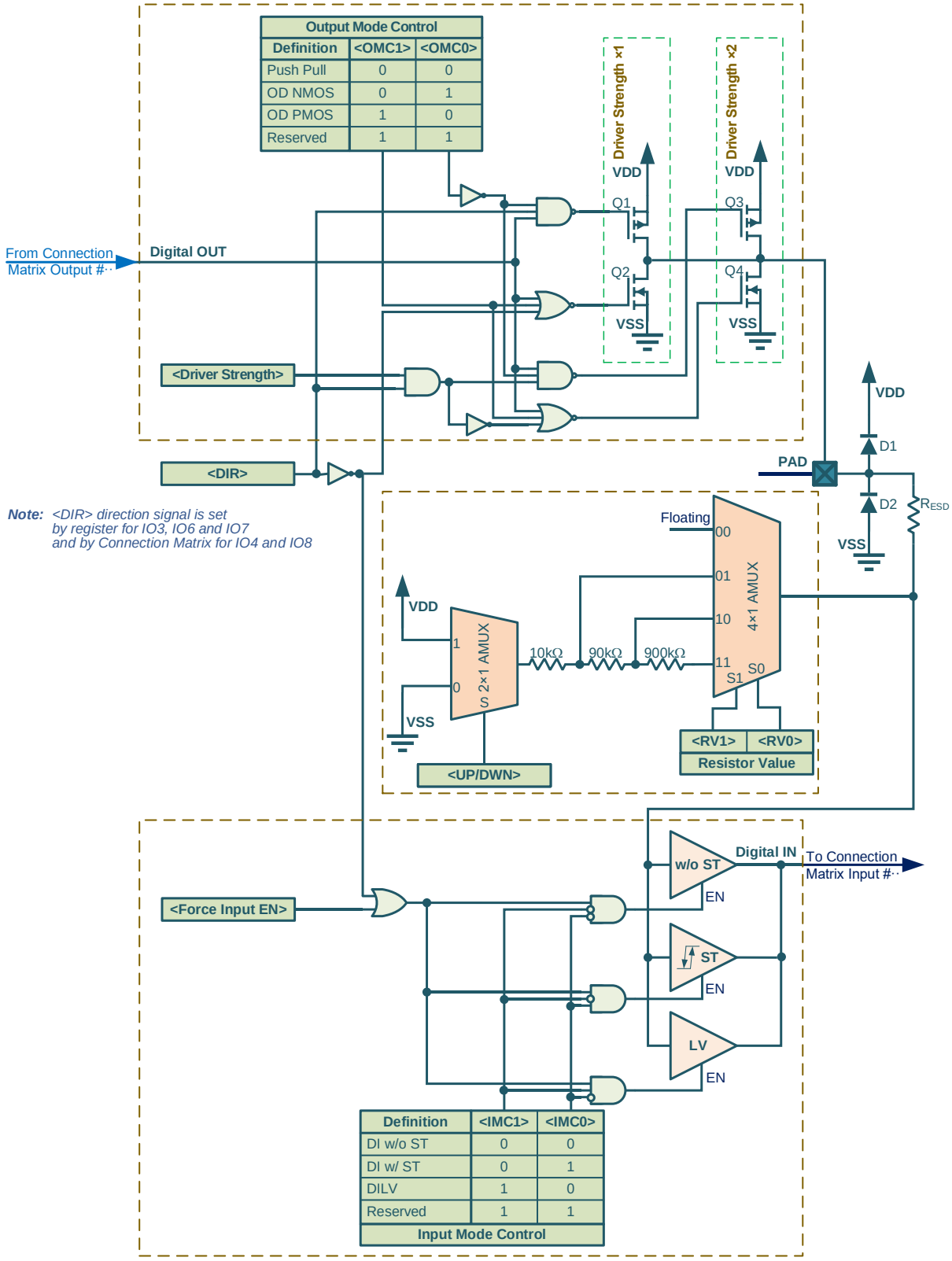


Figure 5.2. IO Structure Diagram

5.6. I/O Register Settings

5.6.1. IO2 Register Settings

Table 5.1 IO2 Register Settings

Signal Function	Register Bit Address	Register Definition
IO2 Input Mode Control	<408:407>	00: Digital Input without Schmitt trigger 01: Digital Input with Schmitt trigger 10: Digital Input Low Voltage 11: Reserved
IO2 Pull Down Resistor Value selection	<410:409>	00: Floating 01: 10 kΩ Resistor 10: 100 kΩ Resistor 11: 1 MΩ Resistor

5.6.2. IO3 Register Settings

Table 5.2 IO3 Register Settings

Signal Function	Register Bit Address	Register Definition
IO3 Driver Strength selection	<337>	0: ×1 Driver Strength 1: ×2 Driver Strength
IO3 Force Input Enable	<369>	0: Disable 1: Enable (Input is always ON)
IO3 Direction	<404>	0: Input Mode 1: Output Mode
IO3 Input Mode Control	<413:412>	00: Digital Input without Schmitt trigger 01: Digital Input with Schmitt trigger 10: Digital Input Low Voltage 11: Reserved
IO3 Output Mode Control	<415:414>	00: Push Pull 01: Open Drain NMOS 10: Open Drain PMOS 11: Reserved
IO3 Pull Up/Down Resistor Value selection	<417:416>	00: Floating 01: 10 kΩ Resistor 10: 100 kΩ Resistor 11: 1 MΩ Resistor
IO3 Pull Up/Down Resistor selection	<418>	0: Pull Down Resistor 1: Pull Up Resistor

5.6.3. IO4 Register Settings

Table 5.3 IO4 Register Settings

Signal Function	Register Bit Address	Register Definition
IO4 Driver Strength selection	<338>	0: ×1 Driver Strength 1: ×2 Driver Strength
IO4 Force Input Enable	<370>	0: Disable 1: Enable (Input is always ON)
IO4 Input Mode Control	<420:419>	00: Digital Input without Schmitt trigger 01: Digital Input with Schmitt trigger 10: Digital Input Low Voltage 11: Reserved
IO4 Output Mode Control	<422:421>	00: Push Pull 01: Open Drain NMOS 10: Open Drain PMOS 11: Reserved

Signal Function	Register Bit Address	Register Definition
IO4 Pull Up/Down Resistor Value selection	<424:423>	00: Floating 01: 10 kΩ Resistor 10: 100 kΩ Resistor 11: 1 MΩ Resistor
IO4 Pull Up/Down Resistor selection	<425>	0: Pull Down Resistor 1: Pull Up Resistor

5.6.4. IO6 Register Settings

Table 5.4 IO6 Register Settings

Signal Function	Register Bit Address	Register Definition
IO6 Driver Strength selection	<339>	0: ×1 Driver Strength 1: ×2 Driver Strength
IO6 Force Input Enable	<371>	0: Disable 1: Enable (Input is always ON)
IO6 Direction	<405>	0: Input Mode 1: Output Mode
IO6 Input Mode Control	<427:426>	00: Digital Input without Schmitt trigger 01: Digital Input with Schmitt trigger 10: Digital Input Low Voltage 11: Reserved
IO6 Output Mode Control	<429:428>	00: Push Pull 01: Open Drain NMOS 10: Open Drain PMOS 11: Reserved
IO6 Pull Up/Down Resistor Value selection	<431:430>	00: Floating 01: 10 kΩ Resistor 10: 100 kΩ Resistor 11: 1 MΩ Resistor
IO6 Pull Up/Down Resistor selection	<432>	0: Pull Down Resistor 1: Pull Up Resistor

5.6.5. IO7 Register Settings

Table 5.5 IO7 Register Settings

Signal Function	Register Bit Address	Register Definition
IO7 Driver Strength selection	<340>	0: ×1 Driver Strength 1: ×2 Driver Strength
IO7 Force Input Enable	<372>	0: Disable 1: Enable (Input is always ON)
IO7 Direction	<406>	0: Input Mode 1: Output Mode
IO7 Input Mode Control	<434:433>	00: Digital Input without Schmitt trigger 01: Digital Input with Schmitt trigger 10: Digital Input Low Voltage 11: Reserved
IO7 Output Mode Control	<436:435>	00: Push Pull 01: Open Drain NMOS 10: Open Drain PMOS 11: Reserved
IO7 Pull Up/Down Resistor Value selection	<438:437>	00: Floating 01: 10 kΩ Resistor 10: 100 kΩ Resistor 11: 1 MΩ Resistor
IO7 Pull Up/Down Resistor selection	<439>	0: Pull Down Resistor 1: Pull Up Resistor

5.6.6. IO8 Register Settings

Table 5.6 IO8 Register Settings

Signal Function	Register Bit Address	Register Definition
IO8 Driver Strength selection	<341>	0: ×1 Driver Strength 1: ×2 Driver Strength
IO8 Force Input Enable	<373>	0: Disable 1: Enable (Input is always ON)
IO8 Input Mode Control	<441:440>	00: Digital Input without Schmitt trigger 01: Digital Input with Schmitt trigger 10: Digital Input Low Voltage 11: Reserved
IO8 Output Mode Control	<443:442>	00: Push Pull 01: Open Drain NMOS 10: Open Drain PMOS 11: Reserved
IO8 Pull Up/Down Resistor Value selection	<445:444>	00: Floating 01: 10 kΩ Resistor 10: 100 kΩ Resistor 11: 1 MΩ Resistor
IO8 Pull Up/Down Resistor selection	<446>	0: Pull Down Resistor 1: Pull Up Resistor

6. Connection Matrix

The ALM1108 Connection Matrix is used to create internal routing for the internal functions of the device once it is programmed. The one-time NVM cell provides programming for the registers during its Test Mode Operation. All of the connection points for each logic cell within the ALM1108 has a specific digital bit code assigned to it that is set to active HIGH or inactive LOW based on the created design. Once the 512 register bits of the ALM1108 are programmed, a fully custom circuit will be created.

The Connection Matrix has 32 inputs and 40 outputs. Each individual input to the Connection Matrix is hard-wired to a particular macrocell output: including IOs, Multifunctional Macrocells, Logic **1**, Logic **0,** etc. Each individual output from the Connection Matrix is hard-wired to a particular macrocell input and uses a 5-bit register to select one of the 32 input lines (see Section 6.1 Example of Matrix Connection).

For a complete list of the ALM1108 register table, see Section 15 Appendix A – ALM1108 Register Definition.

6.1. Example of Matrix Connection

A simple design example to highlight the Matrix Connection is shown in Figure 6.1.

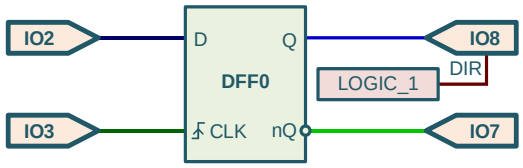


Figure 6.1. Example Design

Figure 6.2 and Figure 6.3 explain the strategy of the Matrix Connection configuration.

Function	IN	Logic 0	IO2	IO3	IO4	DFF0 (Q)	DFF1 (Q)	. . .	. . .	. . .	DFF0 (nQ)	. . .	LOGIC_1
OUT	#	0	1	2	3	4	5	. . .	. . .	. . .	27	. . .	31
IO3 <4:0>	0												
IO4 <9:5>	1												
IO4 (DIR) <14:10>	2												
DFF0(CLK) <20:16>	3												
DFF0(D) <25:21>	4												
2-bit LUT1(IN0) <30:26>	5												
. .	. .												
. .	. .												
. .	. .												
IO6 <190:186>	36												
IO7 <196:192>	37												
IO8 <201:197>	38												
IO8(DIR) <206:202>	39												

Figure 6.2. Connection Matrix Structure

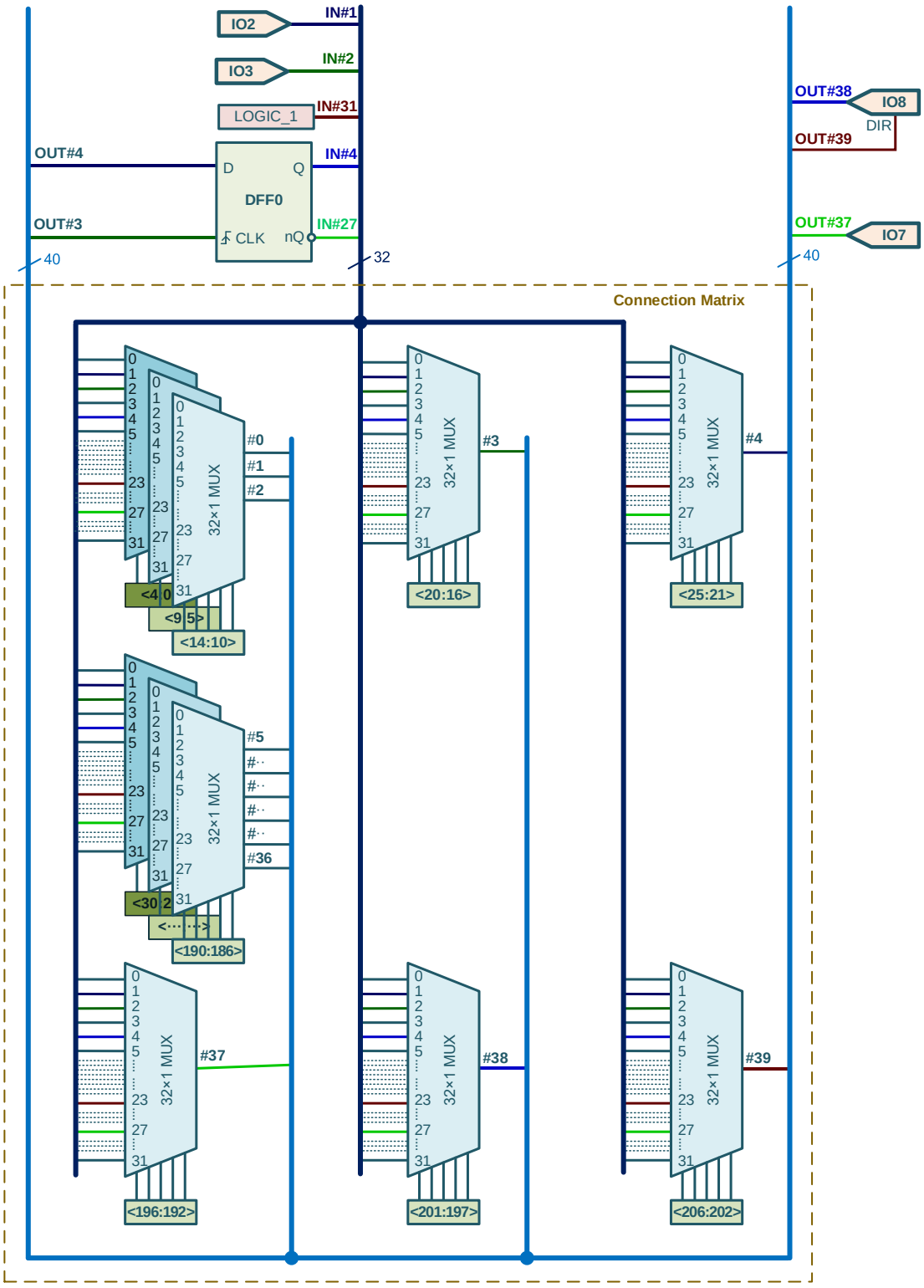


Figure 6.3. Block Diagram of Connection Matrix

6.2. Matrix Input Table

Table 6.1. Matrix Input Table

Matrix Input Number	Matrix Input Signal Function	Matrix Decode				
		4	3	2	1	0
0	Logic **0**	0	0	0	0	0
1	IO2 DOUT	0	0	0	0	1
2	IO3 DOUT	0	0	0	1	0
3	IO4 DOUT	0	0	0	1	1
4	2-bit LUT0 OUT / DFF0/LATCH0 Q	0	0	1	0	0
5	2-bit LUT1 OUT / DFF1/LATCH1 Q	0	0	1	0	1
6	2-bit LUT2 OUT	0	0	1	1	0
7	2-bit LUT3 OUT	0	0	1	1	1
8	3-bit LUT0 OUT0 / DFF2/LATCH2 (SET/RST) Q	0	1	0	0	0
9	3-bit LUT1 OUT0 / DFF3/LATCH3 (SET/RST) Q	0	1	0	0	1
10	3-bit LUT2 OUT / DFF4/LATCH4 (SET/RST) Q	0	1	0	1	0
11	3-bit LUT3 OUT / DFF5/LATCH5 (SET/RST) Q	0	1	0	1	1
12	Shift Register OUT0	0	1	1	0	0
13	Shift Register OUT1	0	1	1	0	1
14	4-bit LUT0 OUT / TMR2 OUT (w/ EXTCLK)	0	1	1	1	0
15	TMR0 OUT (w/ EXTCLK Shared with TMR1 EXTCLK)	0	1	1	1	1
16	TMR1 OUT (w/ EXTCLK shared with TMR0 EXTCLK)	1	0	0	0	0
17	TMR3 OUT	1	0	0	0	1
18	TMR3 ED	1	0	0	1	0
19	PDLY OUT	1	0	0	1	1
20	OSC OUT0	1	0	1	0	0
21	OSC OUT1	1	0	1	0	1
22	3-bit LUT4 OUT / Shift Register (1st stage) Q[1]	1	0	1	1	0
23	Ready	1	0	1	1	1
24	IO6 DOUT	1	1	0	0	0
25	IO7 DOUT	1	1	0	0	1
26	IO8 DOUT	1	1	0	1	0
27	DFF0/LATCH0 nQ	1	1	0	1	1
28	DFF1/LATCH1 nQ	1	1	1	0	0
29	3-bit LUT0 OUT1 / DFF2/LATCH2 (SET/RST) nQ	1	1	1	0	1
30	3-bit LUT1 OUT1 / DFF3/LATCH3 (SET/RST) nQ	1	1	1	1	0
31	Logic **1**	1	1	1	1	1

6.3. Matrix Output Table

Table 6.2. Matrix Output Table

Register Bit Address	Matrix Output Signal Function	Matrix Output Number
<4:0>	IO3 DIN	0
<9:5>	IO4 DIN	1
<14:10>	IO4 DIR	2
<20:16>	IN0 of 2-bit LUT0 or CLK of DFF0 or L of LATCH0	3
<25:21>	IN1 of 2-bit LUT0 or D of DFF0/LATCH0	4
<30:26>	IN0 of 2-bit LUT1 or CLK of DFF1 or L of LATCH1	5
<35:31>	IN1 of 2-bit LUT1 or D of DFF1/LATCH1	6
<40:36>	IN0 of 2-bit LUT2	7
<48:44>	IN1 of 2-bit LUT2	8
<53:49>	IN0 of 2-bit LUT3	9
<58:54>	IN1 of 2-bit LUT3	10
<63:59>	IN0 of 3-bit LUT0 or CLK of DFF2 or L of LATCH2	11
<68:64>	IN1 of 3-bit LUT0 or D of DFF2/LATCH2	12
<73:69>	IN2 of 3-bit LUT0 or nRST(nSET) of DFF2/LATCH2	13
<78:74>	IN0 of 3-bit LUT1 or CLK of DFF3 or L of LATCH3	14
<83:79>	IN1 of 3-bit LUT1 or D of DFF3/LATCH3	15
<89:85>	IN2 of 3-bit LUT1 or nRST(nSET) of DFF3/LATCH3	16
<94:90>	IN0 of 3-bit LUT2 or CLK of DFF4 or L of LATCH4	17
<99:95>	IN1 of 3-bit LUT2 or D of DFF4/LATCH4	18
<104:100>	IN2 of 3-bit LUT2 or nRST(nSET) of DFF4/LATCH4	19
<109:105>	IN0 of 3-bit LUT3 or CLK of DFF5 or L of LATCH5	20
<114:110>	IN1 of 3-bit LUT3 or D of DFF5/LATCH5	21
<119:115>	IN2 of 3-bit LUT3 or nRST(nSET) of DFF5/LATCH5	22
<124:120>	IN0 of 3-bit LUT4 or D of Shift Register	23
<129:125>	IN1 of 3-bit LUT4 or nRST of Shift Register	24
<134:130>	IN2 of 3-bit LUT4 or CLK of Shift Register	25
<139:135>	IN0 of 4-bit LUT0 or CLK of TMR2	26
<145:141>	IN1 of 4-bit LUT0 or IN of TMR2 (RST for Counter Mode)	27
<150:146>	IN2 of 4-bit LUT0 or KEEP of TMR2	28
<155:151>	IN3 of 4-bit LUT0 or UP of TMR2	29
<160:156>	IN of TMR0 (RST for Counter Mode)	30
<165:161>	IN of TMR1 (RST for Counter Mode)	31
<170:166>	CLK of TMR0/TMR1	32
<175:171>	IN of TMR3 (EXT CLK for Counter Mode)	33
<180:176>	IN of PDLY	34
<185:181>	PWRDWN of OSC (Higher Priority) (HIGH is Power Down).	35
<190:186>	IO6 DIN	36
<196:192>	IO7 DIN	37
<201:197>	IO8 DIN	38
<206:202>	IO8 DIR	39

7. Combinatorial Logic

Two Look Up Tables (LUTs) within the ALM1108 provide the support for combinatorial logic. There are two 2-bit LUTs and eight Multifunctional Macrocells that can be used as LUTs. For more details, please see Section 8 Multifunctional Macrocells.

7.1. 2-bit LUT

The 2-bit LUT (Figure 7.1) takes in two input signals from the connection matrix and produces a single output that goes back into the connection matrix. The LUT allows implementing user-defined combinatorial logic function, including standard digital logic gates (AND, NAND, OR, NOR, XOR, XNOR). Standard logic gate configuration of the LUT is shown in the Table 7.1.

Table 7.1. Truth Table of Standard Logic Gates

Function	MSB			LSB
AND-2	1	0	0	0
NAND-2	0	1	1	1
OR-2	1	1	1	0
NOR-2	0	0	0	1
XOR-2	0	1	1	0
XNOR-2	1	0	0	1

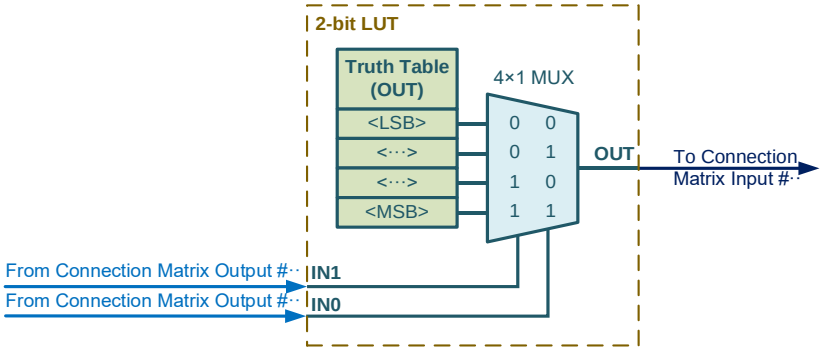


Figure 7.1. 2-bit LUTs

7.1.1. 2-bit LUT2 Macrocell

Registers of 2-bit LUT2 defined its output function set out in Table 7.2.

Table 7.2. 2-bit LUT2 Truth Table

IN1	IN0	OUT	
0	0	<227>	LSB
0	1	<228>	
1	0	<229>	
1	1	<230>	MSB

7.1.2. 2-bit LUT3 Macrocell

Registers of 2-bit LUT3 defined its output function set out in Table 7.3.

Table 7.3. 2-bit LUT3 Truth Table

IN1	IN0	OUT	
0	0	<231>	LSB
0	1	<232>	
1	0	<233>	
1	1	<234>	MSB

8. Multifunctional Macrocells

Nine multifunction macrocells (MF) in the ALM1108 can serve more than one logic or timing function. They can serve as a Look Up Table (LUT) or as another logic or timing function in four of the cases. Functions that can be implemented in these macrocells:

- Two selectable 2-bit LUTs or DFF/LATCHs;
- Four selectable 3-bit LUTs or DFF/LATCHs;
- One 3-bit LUT or 16-bit Shift Register;
- One 4-bit LUT or 8-Bit TMR;
- One Programmable Delay or Edge Detector.

8.1. MF (2-bit LUT / DFF/LATCH) Macrocells

The ALM1108 has MF macrocells capable of serving as either 2-bit LUTs, DFFs, or LATCHs (see Figure 8.1).

When the MF macrocells are used as LUT, the 2-bit LUT takes in two input signals from the connection matrix and produces a single output that goes back into the connection matrix. The LUT allows implementing user-defined combinatorial logic function, including standard digital logic gates (AND, NAND, OR, NOR, XOR, XNOR). Standard logic gate configuration of the LUT is shown in the Table 8.1.

When the macrocells are used as DFF or LATCH, the two input signals from the connection matrix go to the data (D), clock/latch (CLK/L) inputs for the DFF/LATCH, and the outputs Q and nQ go back to the connection matrix. Operation of the DFF and LATCH are shown in Table 8.2, Table 8.3.

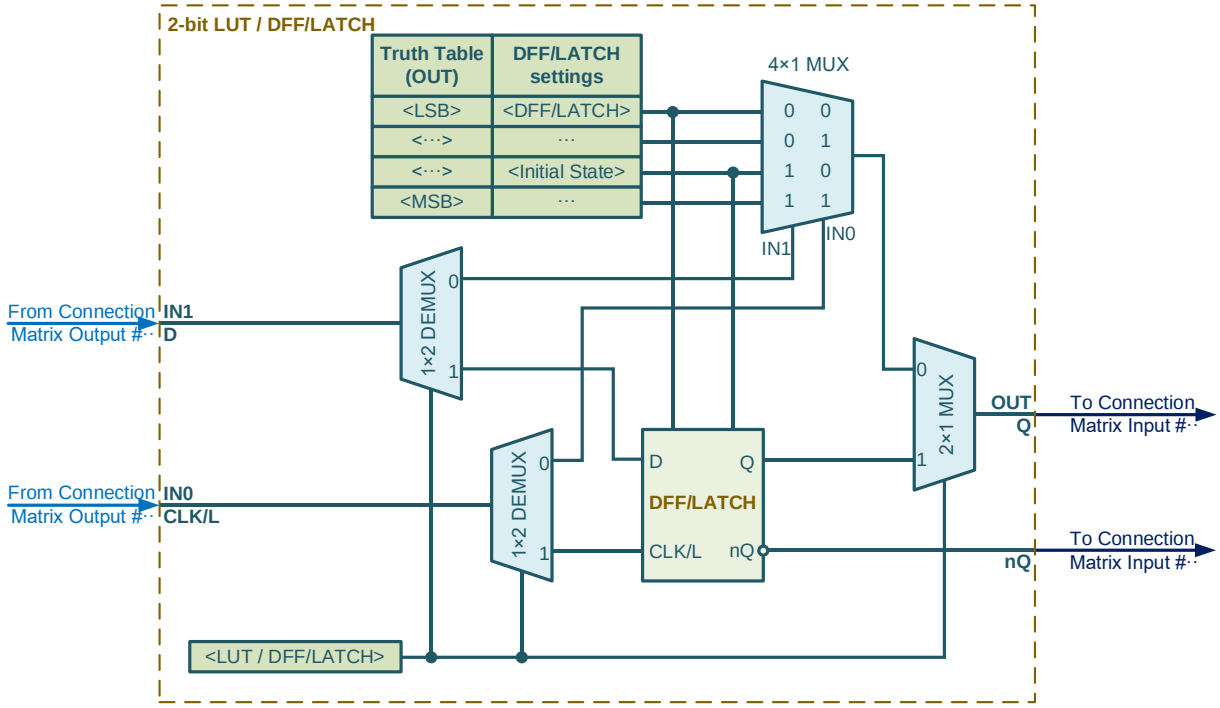


Figure 8.1. Schematic diagram of 2-bit LUT / DFF/LATCH

Table 8.1. 2-bit LUT Truth Table of Standard Logic Gates

Function	MSB			LSB
AND-2	1	0	0	0
NAND-2	0	1	1	1
OR-2	1	1	1	0
NOR-2	0	0	0	1
XOR-2	0	1	1	0

Table 8.2. Operation of the DFF

D	CLK	Q(t)/nQ(t)
0	↑	0/1
0	↓	t–1
1	↑	1/0
1	↓	t–1

Note 8.1: X – Don't Care
Note 8.2: t–1 – Previous State

Table 8.3. Operation of the LATCH

L	D	Q(t)/nQ(t)
0	0	0/1
0	1	1/0
1	0	t–1
1	1	t–1

Note 8.3: X – Don't Care
Note 8.4: t–1 – Previous State

8.1.1. 2-bit LUT0 / DFF0/LATCH0 Macrocell

Register settings of 2-bit LUT0 / DFF0/LATCH0 macrocell set out in Table 8.4.

Table 8.4. 2-bit LUT0 / DFF0/LATCH0 Register Settings

Signal Function	Register Bit Address	Register Definition
LUT or DFF/LATCH selection	<235>	0: LUT 1: DFF/LATCH
LUT data	<218:215>	4-bit data
DFF or LATCH selection	<215>	0: DFF function 1: LATCH function
DFF/LATCH initial state selection	<217>	0: LOW 1: HIGH

The 2-bit LUT0 / DFF0/LATCH0 macrocell, if programmed for a LUT function, uses 4-bit register to define its output function by reg<218:215> (see Table 8.5).

Table 8.5. 2-bit LUT0 Truth Table

IN1	IN0	OUT	
0	0	<215>	LSB
0	1	<216>	
1	0	<217>	
1	1	<218>	MSB

8.1.2. 2-bit LUT1 / DFF1/LATCH1 Macrocell

Register settings of 2-bit LUT1 / DFF1/LATCH1 macrocell set out in Table 8.6.

Table 8.6. 2-bit LUT1 / DFF1/LATCH1 Register Settings

Signal Function	Register Bit Address	Register Definition
LUT or DFF/LATCH	<236>	0: LUT 1: DFF/LATCH
LUT data	<223:220>	4-bit data
DFF or LATCH selection	<220>	0: DFF function 1: LATCH function
DFF/LATCH initial state selection	<222>	0: LOW 1: HIGH

The 2-bit LUT1 / DFF1/LATCH1 macrocell, if programmed for a LUT function, uses 4-bit register to define its output function by reg<223:220> (see Table 8.7).

Table 8.7. 2-bit LUT1 Truth Table

IN1	IN0	OUT	
0	0	<220>	LSB
0	1	<221>	
1	0	<222>	
1	1	<223>	MSB

8.2. MF (3-bit LUT / DFF/LATCH) Macrocells

The ALM1108 has an MF macrocell that can serve as either 3-bit LUTs or as DFF/LATCHs (Figure 8.2, Figure 8.3).

When the MF macrocells are used as LUT, the 3-bit LUT takes in three input signals from the connection matrix and produces a single output for 3-bit LUT2 and 3-bit LUT3, and two outputs for 3-bit LUT0 and 3-bit LUT1 that go back into the connection matrix. The LUT allows the implementation of user-defined combinatorial logic function, including standard digital logic gates (AND, NAND, OR, NOR, XOR, XNOR). Standard logic gate configuration of the LUT is shown in Table 8.8.

When the macrocells are used as DFF or LATCH, the three input signals from the connection matrix go to the data (D), clock/latch (CLK/L) and (n)RST/(n)SET inputs of the DFF/LATCH, and the output (DFF4/LATCH4, DFF5/LATCH5) or outputs (DFF2/LATCH2, DFF3/LATCH3) go back to the connection matrix. Operation of the DFF and LATCH are shown in Table 8.9, Table 8.10.

Table 8.8. 3-bit LUT Truth Table of Standard Logic Gates

Function	MSB							LSB
AND-3	1	0	0	0	0	0	0	0
NAND-3	0	1	1	1	1	1	1	1
OR-3	1	1	1	1	1	1	1	0
NOR-3	0	0	0	0	0	0	0	1
XOR-3	1	0	0	1	0	1	1	0
XNOR-3	0	1	1	0	1	0	0	1

Table 8.9. Operation of the DFF

nRST/nSET	D	CLK	Q(t)
nRST = 0	X	X	0/1
nSET = 0	X	X	1/0
1	0	↑	0/1
1	0	↓	t–1
1	1	↑	1/0
1	1	↓	t–1

Note 8.5: X – Don't Care

Note 8.6: t–1 – Previous State

Table 8.10. Operation of the LATCH

nRST/nSET	L	D	Q(t)/nQ(t)
nRST = 0	X	X	0/1
nSET = 0	X	X	1/0
1	0	0	0/1
1	0	1	1/0
1	1	0	t–1
1	1	1	t–1

Note 8.7: X – Don't Care

Note 8.8: t–1 – Previous State

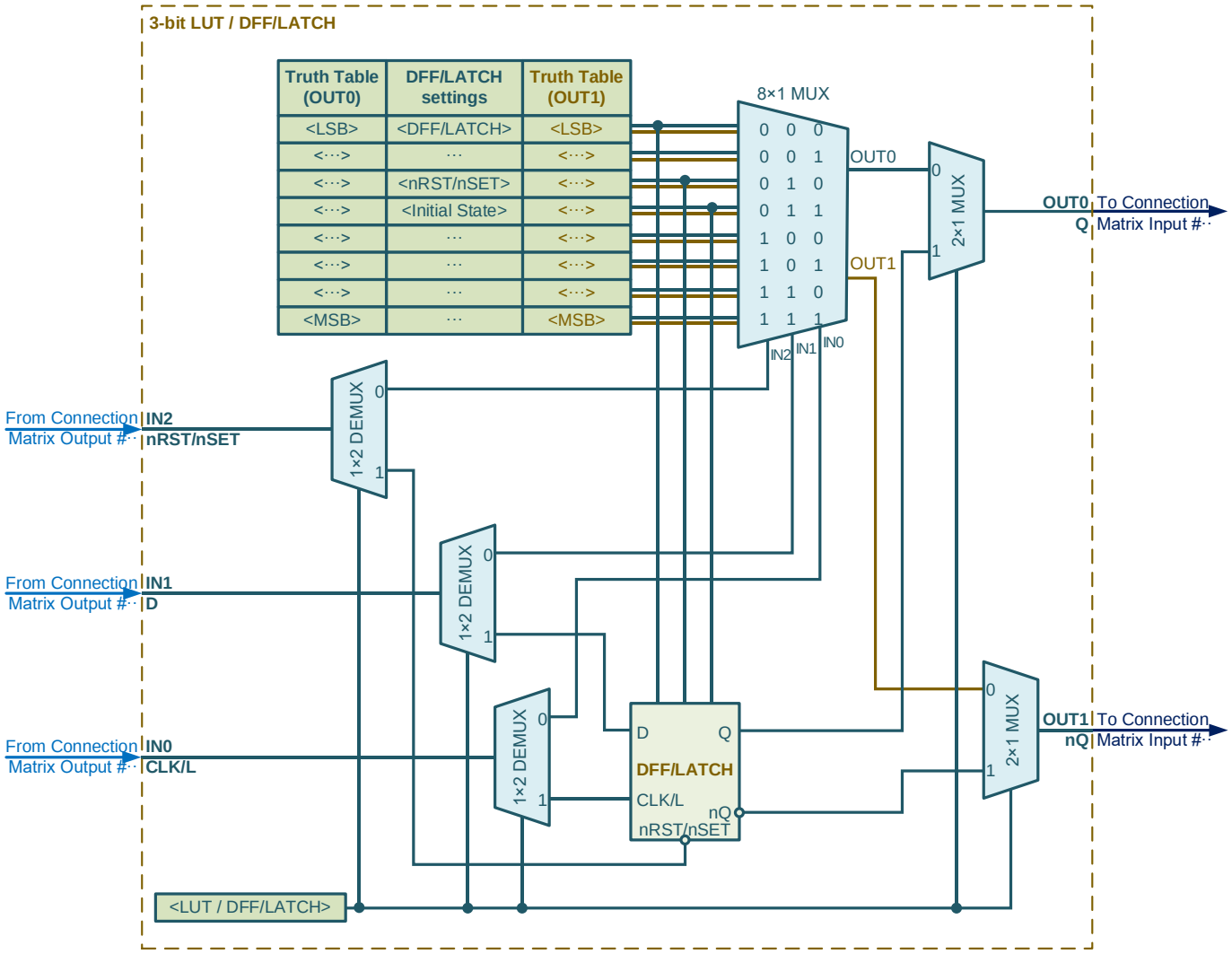


Figure 8.2. Schematic diagram of 3-bit LUT / DFF/LATCH (with nRST/nSET and 2 OUTs)

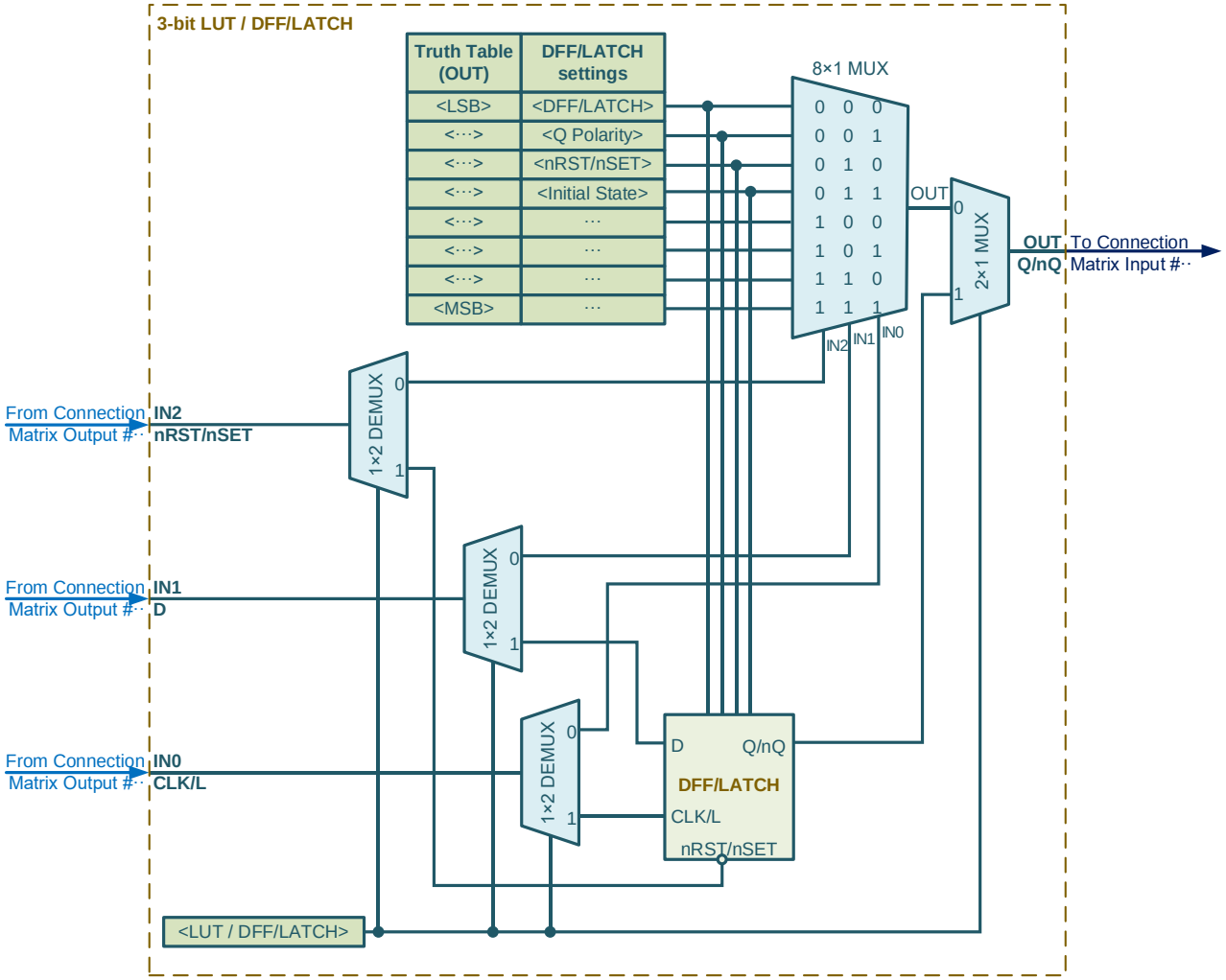


Figure 8.3. Schematic diagram of 3-bit LUT / DFF/LATCH (with nRST/nSET and single OUT)

8.2.1. 3-bit LUT0 / DFF2/LATCH2

Schematic diagram of 3-bit LUT0 / DFF2/LATCH2 macrocell is shown in Figure 8.2. Its register settings set out in Table 8.11.

Table 8.11. 3-bit LUT0 / DFF2/LATCH2 Register Settings

Signal Function	Register Bit Address	Register Definition
LUT or DFF/LATCH select	<293>	0: LUT 1: DFF/LATCH
LUT OUT0 data	<244:237>	8-bit data
LUT OUT1 data	<252:245>	8-bit data
DFF or LATCH selection	<237>	0: DFF function 1: LATCH function
DFF/LATCH nRST/nSET selection	<239>	0: nRST from matrix out 1: nSET from matrix out
DFF/LATCH initial state selection	<240>	0: LOW 1: HIGH

The 3-bit LUT0 / DFF2/LATCH2 macrocell, if programmed for a LUT function, uses 8-bit register to define its output function (see Table 8.12):
OUT0 by reg<244:237>;
OUT1 by reg<252:245>.

Table 8.12. 3-bit LUT0 Truth Table

IN2	IN1	IN0	OUT0	OUT1	
0	0	0	<237>	<245>	LSB
0	0	1	<238>	<246>	
0	1	0	<239>	<247>	
0	1	1	<240>	<248>	
1	0	0	<241>	<249>	
1	0	1	<242>	<250>	
1	1	0	<243>	<251>	
1	1	1	<244>	<252>	MSB

8.2.2. 3-bit LUT1 / DFF3/LATCH3

Schematic diagram of 3-bit LUT1 / DFF3/LATCH3 macrocell is shown in Figure 8.2. Its register settings set out in Table 8.13.

Table 8.13. 3-bit LUT1 / DFF3/LATCH3 Register Settings

Signal Function	Register Bit Address	Register Definition
LUT or DFF/LATCH selection	<294>	0: LUT 1: DFF/LATCH
LUT OUT0 data	<260:253>	8-bit data
LUT OUT1 data	<268:261>	8-bit data
DFF or LATCH selection	<253>	0: DFF function 1: LATCH function
DFF/LATCH nRST/nSET selection	<255>	0: nRST from matrix out 1: nSET from matrix out
DFF/LATCH initial state selection	<256>	0: LOW 1: HIGH

The 3-bit LUT1 / DFF3/LATCH3 macrocell, if programmed for a LUT function, uses 8-bit register to define its output function (see Table 8.14):

OUT0 by reg<260:253>;
OUT1 by reg<268:261>.

Table 8.14. 3-bit LUT1 Truth Table

IN2	IN1	IN0	OUT0	OUT1	
0	0	0	<253>	<261>	LSB
0	0	1	<254>	<262>	
0	1	0	<255>	<263>	
0	1	1	<256>	<264>	
1	0	0	<257>	<265>	
1	0	1	<258>	<266>	
1	1	0	<259>	<267>	
1	1	1	<260>	<268>	MSB

8.2.3. 3-bit LUT2 / DFF4/LATCH4

Schematic diagram of 3-bit LUT2 / DFF4/LATCH4 macrocell is shown in Figure 8.3. Its register settings set out in

Table 8.15.

Table 8.15. 3-bit LUT2 / DFF4/LATCH4 Register Settings

Signal Function	Register Bit Address	Register Definition
LUT or DFF/LATCH selection	<295>	0: LUT 1: DFF/LATCH
LUT data	<276:269>	8-bit data
DFF or LATCH selection	<269>	0: DFF function 1: LATCH function
DFF/LATCH output polarity selection	<270>	0: Non-Inverted (Q) 1: Inverted (nQ)
DFF/LATCH nRST/nSET selection	<271>	0: nRST from matrix out 1: nSET from matrix out
DFF/LATCH initial state selection	<272>	0: LOW 1: HIGH

The 3-bit LUT2 / DFF4/LATCH4 macrocell, if programmed for a LUT function, uses 8-bit register to define its output function by reg<276:269> (see Table 8.16).

Table 8.16. 3-bit LUT2 Truth Table

IN2	IN1	IN0	OUT	
0	0	0	<269>	LSB
0	0	1	<270>	
0	1	0	<271>	
0	1	1	<272>	
1	0	0	<273>	
1	0	1	<274>	
1	1	0	<275>	
1	1	1	<276>	MSB

8.2.4. 3-bit LUT3 / DFF5/LATCH5

Schematic diagram of 3-bit LUT3 / DFF5/LATCH5 macrocell is shown in Figure 8.3. Its register settings set out in Table 8.21.

Table 8.17. 3-bit LUT3 / DFF5/LATCH5 Register Settings

Signal Function	Register Bit Address	Register Definition
LUT or DFF/LATCH selection	<296>	0: LUT 1: DFF/LATCH
LUT data	<284:277>	8-bit data
DFF or LATCH selection	<277>	0: DFF function 1: LATCH function
DFF/LATCH Output polarity selection	<278>	0: Non-Inverted (Q) 1: Invertede (nQ)
DFF/LATCH nRST/nSET selection	<279>	0: nRST from matrix out 1: nSET from matrix out
DFF/LATCH initial state selection	<280>	0: LOW 1: HIGH

The 3-bit LUT3 / DFF5/LATCH5 macrocell, if programmed for a LUT function, uses 8-bit register to define its output function by reg<284:277> (see Table 8.18).

Table 8.18. 3-bit LUT3 Truth Table

IN2	IN1	IN0	OUT	
0	0	0	<277>	LSB
0	0	1	<278>	
0	1	0	<279>	
0	1	1	<280>	
1	0	0	<281>	
1	0	1	<282>	
1	1	0	<283>	
1	1	1	<284>	MSB

8.3. MF (3-bit LUT4 / Shift Register) Macrocell

The MF macrocell has a capability to serve as either a 3-bit LUT or as a Shift Register (SHR).

When the MF macrocell is used as LUT, the 3-bit LUT takes in three input signals from the connection matrix and produces a single output, that go back into the connection matrix. The LUT allows implementing user-defined combinatorial logic function, including standard digital logic gates (AND, NAND, OR, NOR, XOR, XNOR). Standard logic gates configuration of the LUT is shown in the Table 8.19.

The Shift Register contains sixteen stages cascade of positive edge triggered DFFs. The signal from any stage can be routed to OUT0 and OUT1 independently. The Q[1] output is always connected to the output of the first stage. The Shift Register has Data (D), Clock (CLK) and Reset (nRST) inputs from connection matrix. Applying low-level signal to the nRST sets all stage values to zero.

Schematic diagram of 3-bit LUT4 / Shift Register macrocell is shown on Figure 8.4.

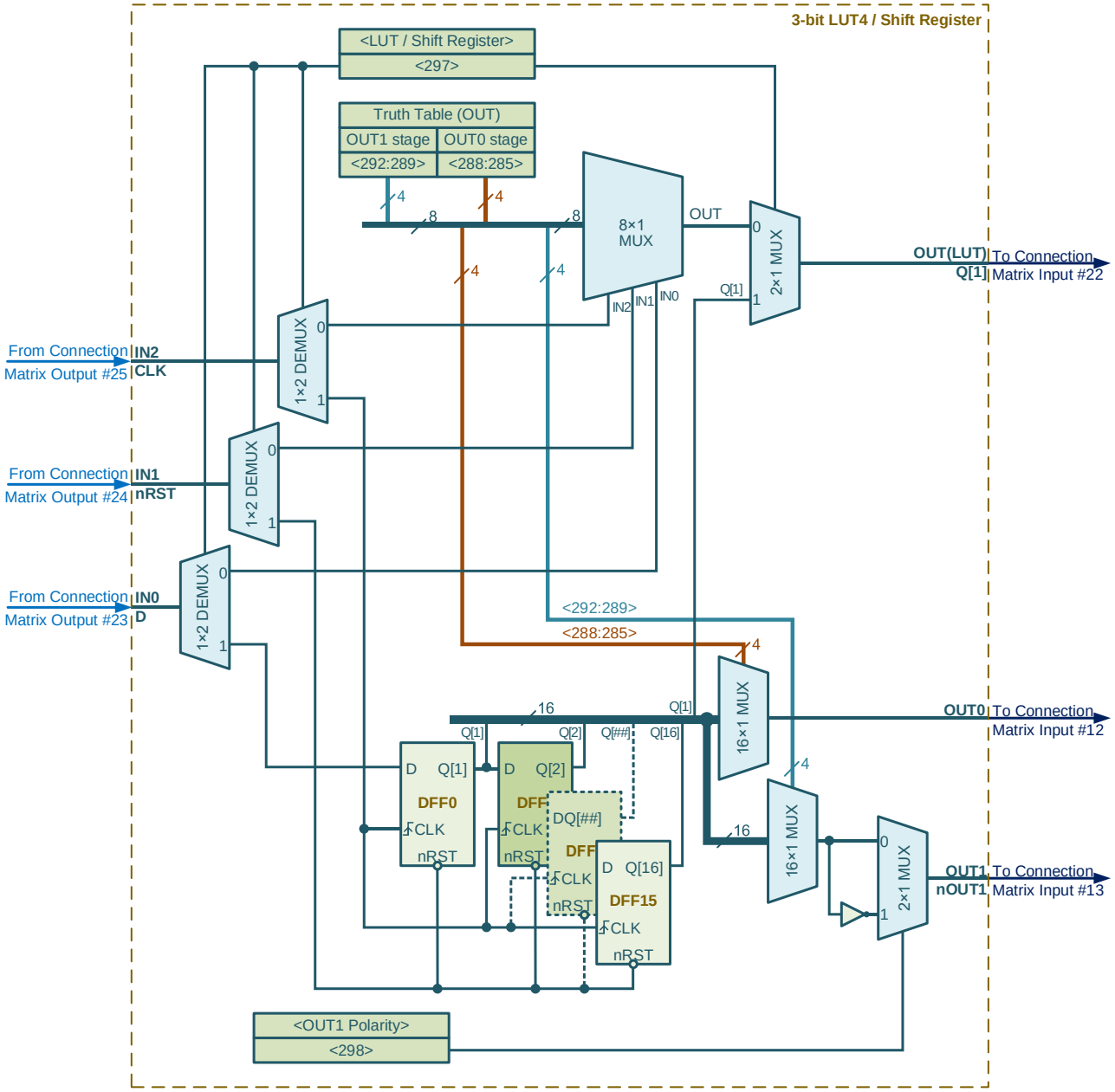


Figure 8.4. 3-bit LUT4 / Shift Register

Table 8.19. 3-bit LUT Truth Table of Standard Logic Gates

Function	MSB							LSB
AND-3	1	0	0	0	0	0	0	0
NAND-3	0	1	1	1	1	1	1	1
OR-3	1	1	1	1	1	1	1	0
NOR-3	0	0	0	0	0	0	0	1
XOR-3	1	0	0	1	0	1	1	0
XNOR-3	0	1	1	0	1	0	0	1

8.3.1. 3-bit LUT4 / Shift Register

The MF registers set out in Table 8.20.

Table 8.20. 3-bit LUT4 / SHR Registers Settings

Signal Function	Register Bit Address	Register Definition
LUT or Shift Register output selection	<297>	0: LUT 1: Shift Register
LUT data	<292:285>	8-bit data
OUT0 stage selection	<288:285>	Data (Shift Register number)
OUT1 stage selection	<292:289>	Data (Shift Register number)
Shift Register OUT1 polarity selection	<298>	0: Non-Inverted (OUT1) 1: Inverted (nOUT1)

The 3-bit LUT4 / Shift Register macrocell, if programmed for a LUT function, uses 8-bit register to define its output function by reg<292:285> (see Table 8.21).

Table 8.21. 3-bit LUT4 Truth Table

IN2	IN1	IN0	OUT	
0	0	0	<285>	LSB
0	0	1	<286>	
0	1	0	<287>	
0	1	1	<288>	
1	0	0	<289>	
1	0	1	<290>	
1	1	0	<291>	
1	1	1	<292>	MSB

8.4. MF (4-bit LUT0 / 16-Bit Timer) Macrocells

One macrocell has the capability to serve as either 4-bit LUTs or as 16-bit timer (TMR) (Figure 8.5).

When the MF macrocells are used as LUT, the 4-bit LUT takes in four input signals from the connection matrix and produces a single output that goes back into the connection matrix. The LUT allows implementing user-defined combinatorial logic function, including standard digital logic gates (AND, NAND, OR, NOR, XOR, XNOR). Standard logic gates configuration of the LUT is shown in the Table 8.22.

When the macrocells are used to implement TMR function, four input signals from the connection matrix go to the external clock (EXTCLK), IN (RST for Counter and FSM modes), KEEP and UP for the TMR, with the output going back to the connection matrix.

The timer has the following mode of operation:

- Delay
- Counter
- One Shot
- Frequency Detector

The output polarity of the TMR is configurable and can be selected as non-inverted or inverted.

The KEEP input allows to pause counting by applying HIGH level to KEEP, the counting is resume after KEEP goes LOW.

In Delay mode, the TMR delays the input signal by the selected edge event (rising edge, falling edge, both edges) for a time determined by the Control Data, input clock signal, and selected divider value. If input signal is shorter than the delay value, the signal does not propagate to the output. The timing diagrams of this mode are shown in Figure 9.2…Figure 9.7.

In the Counter mode the TMR divides input clock signal by the value determined by the Control Data, input clock signal, and selected divider value. The output of the TMR goes HIGH every time when the Counted Value (current value of the counter) is equal 0. The RST of the TMR resets the Counted value to 0 by one of the following events: rising edge, falling edge, both edge, high level. The timing diagrams of this mode are shown in Figure 9.8…Figure 9.13.

The TMR2 has an optional Finite State Machine (FSM) function. There are two matrix inputs for Up and Keep that support FSM functionality. Any counter within the part counts down by default. In FSM mode, it is possible to reverse counting direction by applying HIGH level to the UP input. Timing diagrams of the FSM are shown in Figure 9.27…Figure 9.30.

In One-Shot mode, this macrocell generates a high-level pulse with a set width when detecting the edge event, which is selectable by the registers on its IN input. The pulse width is determined by the Control Data, input clock signal, and selected divider value. Any incoming edges are ignored during pulse width generation. The timing diagrams of this mode are shown in Figure 9.14…Figure 9.19.

In Frequency Detector mode the TMR functions in the following scenarios:

- Rising Edge: The output will go HIGH if the time between two rising edges is less than the delay.
  The output will go LOW if the next rising edge has not come after the last rising edge in specified time.
- Falling Edge: The output will go HIGH if the time between two falling edges is less than the set time.
  The output will go LOW if the next falling edge has not come after the last falling edge in specified time.
- Both Edges: The output will go HIGH if the time between the rising and falling edges is less than the set time, which is equivalent to the length of the pulse.
  The output will go LOW if the next rising/falling edge has not come after the last falling/rising edge in specified time.

The timing diagrams of the Frequency Detector Mode is shown in the Figure 9.20…Figure 9.25.

Time of Timers for each mode can be calculated using the following formulas (Note 8.9, Note 8.10):

- Delay (Figure 9.2…Figure 9.7)
  Delay Time = (Control Data + 1 + VAR) / F_{CLK};
- Counter Figure 9.8…Figure 9.13, Figure 9.27…Figure 9.30)
  Output Period = (Control Data + 1) / F_{CLK};
  Output Frequency = F_{CLK} / (Control Data + 1);
- One Shot (Figure 9.14…Figure 9.19)
  Pulse width = (Control Data + 1 + VAR) / F_{CLK};
- Frequency Detector (Figure 9.20…Figure 9.25)
  Detected Frequency = F_{CLK} / (Control Data + 1 + VAR).

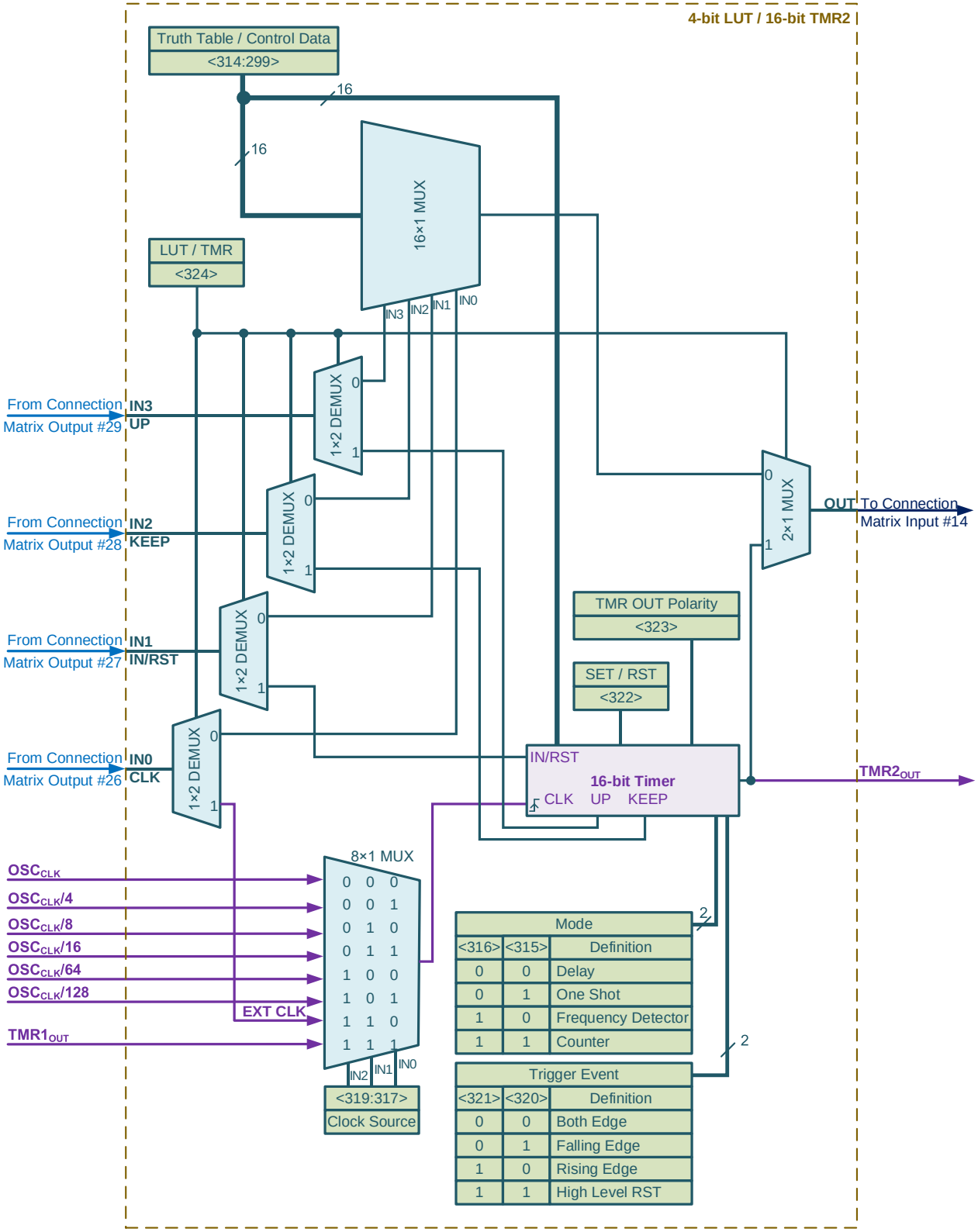
Note 8.9 *F_{CLK} – CLK input frequency.*

Note 8.10 *VAR = 0…1 – defined by the asynchronous time between the input signal and the first clock pulse.*

Note 8.11 *Counters initialize with Control Data after POR.*

Table 8.22. 4-bit LUT Truth Table of Standard Logic Gates

Function	MSB															LSB
AND-4	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
NAND-4	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
OR-4	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0
NOR-4	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
XOR-4	0	1	1	0	1	0	0	1	1	0	0	1	0	1	1	0
XNOR-4	1	0	0	1	0	1	1	0	0	1	1	0	1	0	0	1



Mode		
<316>	<315>	Definition
0	0	Delay
0	1	One Shot
1	0	Frequency Detector
1	1	Counter

Trigger Event		
<321>	<320>	Definition
0	0	Both Edge
0	1	Falling Edge
1	0	Rising Edge
1	1	High Level RST

Figure 8.5. 4-bit LUT0 / TMR2

8.4.1. 4-bit LUT0 / TMR2

Settings of 4-bit LUT0 / TMR2 is set out in Table 8.23.

Table 8.23. 4-bit LUT0 / TMR2 Register Settings

Signal Function	Register Bit Address	Register Definition
LUT or TMR selection	<324>	0: LUT 1: TMR
LUT data	<314:299>	16-bit data
TMR Control Data	<314:299>	1 – 65535: (Delay Time = (Control Data +1) / Frequency)
TMR Mode selection	<316:315>	00: Delay 01: One Shot 10: Frequency Detector 11: Counter
TMR Clock Source selection	<319:317>	000: OSC_{CLK} 001: OSC_{CLK} /4 010: OSC_{CLK} /8 011: OSC_{CLK} /16 100: OSC_{CLK} /64 101: OSC_{CLK} /128 110: External CLK 111: $TMR1_{OUT}$
TMR Trigger Event selection	<321:320>	00: On Both Falling and Rising Edges 01: On Falling Edge only 10: On Rising Edge only 11: No Delay on either Falling or Rising Edges for Delay Mode / High Level Reset for Counter Mode
SET/RST selection (for Counter mode)	<322>	0: Reset to 0 1: Set to Control Data
TMR Output polarity selection	<323>	0: Non-Inverted (OUT) 1: Inverted (nOUT)

The 4-bit LUT0 / TMR2 macrocell, if programmed for a LUT function, uses 16-bit register to define its output function by reg<314:299> (see Table 8.12).

Table 8.24. 4-bit LUT0 Truth Table

IN3	IN2	IN1	IN0	OUT	
0	0	0	0	<299>	LSB
0	0	0	1	<300>	
0	0	1	0	<301>	
0	0	1	1	<302>	
0	1	0	0	<303>	
0	1	0	1	<304>	
0	1	1	0	<305>	
0	1	1	1	<306>	
1	0	0	0	<307>	
1	0	0	1	<308>	
1	0	1	0	<309>	
1	0	1	1	<310>	
1	1	0	0	<311>	
1	1	0	1	<312>	
1	1	1	0	<313>	
1	1	1	1	<314>	MSB

8.5. MF (PDLY / Edge Detector) - Programmable Delay / Edge Detector Macrocell

The ALM1108 has a macrocell that can serve as programmable delay (PDLY) or as an edge detector (Figure 8.6).

In PDLY mode, the macrocell serves as both edge delay with four selectable delay value T_{ADJ}: 140 ns, 280 ns, 420 ns, 560 ns. If input signal is shorter than the delay value, the signal does not propagate to the output and is filtered out.

In Edge Detector mode, the macrocell generates a high level pulse (for non-inverted polarity) when detecting the respective selected edge event (rising edge, falling edge, both edges). The pulse width value (T_{WIDTH}) is configurable (140 ns, 280 ns, 420 ns, 560 ns).
See the timing diagrams below for further information (Figure 8.7).

The output polarity of the macrocell is configurable and can be selected as non-inverted or inverted.

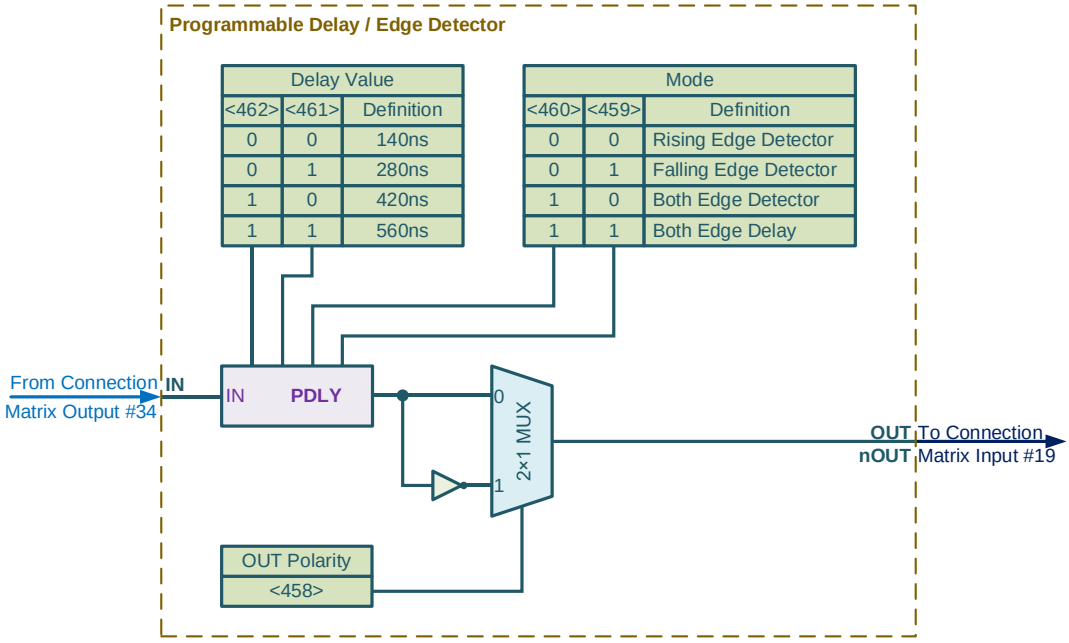


Figure 8.6. Programmable Delay

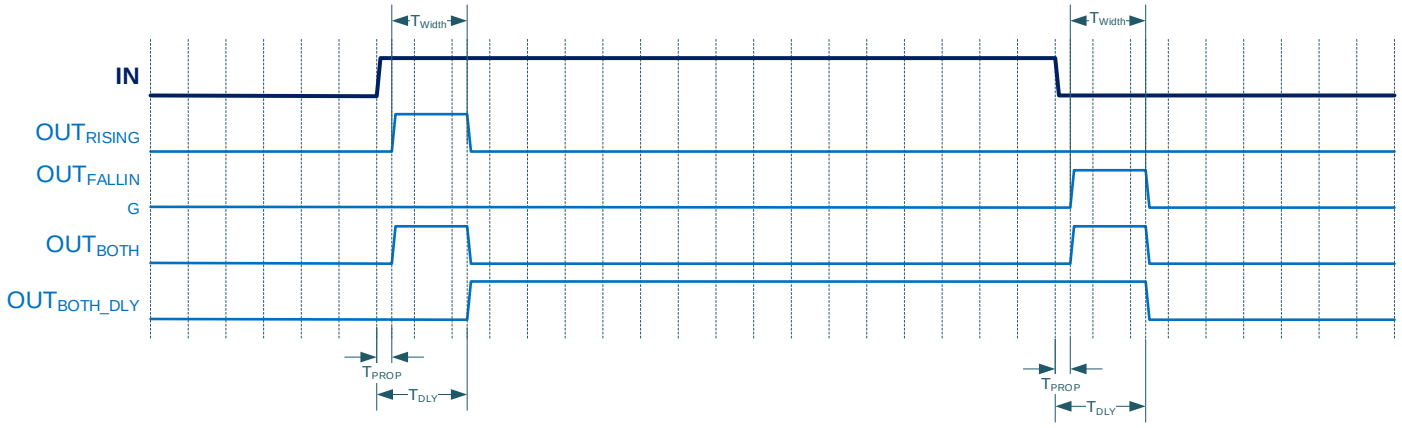


Figure 8.7. Edge Detector Output

8.5.1. PDLY / Edge Detcotr

Settings of PDLY / Edge Detector is shown in Table 8.25.

Table 8.25. Programmable Delay Register Settings

Signal Function	Register Bit Address	Register Definition
Programmable Delay OUT polarity selection	<458>	0: Non-Inverted (OUT) 1: Inverted (nOUT)
Edge Mode of PDLY & Edge Detector selection	<460:459>	00: Rising Edge Detector 01: Falling Edge Detector 10: Both Edge Detector 11: Both Edge Delay
Delay value selection for programmable delay & edge detector (V_{DD} = 3.3 V, typical condition)	<462:461>	00: 140 ns 01: 280 ns 10: 420 ns 11: 560 ns

9. Timers (TMR)

The ALM1108 has three configurable 8-bit timers (TMR0, TMR1 – see Figure 9.1, TMR3 – see Figure 9.31).

TMR0 and TMR1 have one input from the connection matrix for IN/RST, and one for an external counter/clock source (for a total of two inputs from the connection matrix). One of the Timer macrocells (TMR3) has one input from the connection matrix, which has a shared function of IN or external CLK input. The outputs of TMR0 and TMR1 go back to the connection matrix. TMR3 has an additional output of Edge Detector.

Each timer has the following mode of operation:

- Delay
- Counter
- One Shot
- Frequency Detector
- Edge Detector

The output polarity of the TMR is configurable and can be selected as non-inverted or inverted.

In Delay mode, the TMR delays the input signal by the selected edge event (rising edge, falling edge, both edges) for a time determined by the Control Data, input clock signal, and selected divider value. If input signal is shorter than the delay value, the signal does not propagate to the output. The timing diagrams of this mode are shown in Figure 9.2…Figure 9.7.

In Counter mode, the TMR divides input clock signal by the value determined by the Control Data, input clock signal, and selected divider value. The output of the TMR goes HIGH every time when the Counted Value (current value of the counter) is equal 0. The RST of the TMR resets the Counted value to 0 by one of the following events: rising edge, falling edge, both edge, high level. The timing diagrams of this mode are shown in Figure 9.8…Figure 9.13.

In One-Shot mode, this macrocell generates a high-level pulse with a set width when detecting the edge event, which is selectable by the registers on its IN input. The pulse width is determined by the Control Data, input clock signal, and selected divider value. Any incoming edges are ignored during pulse width generation. The timing diagrams of this mode are shown in Figure 9.14…Figure 9.19.

In Frequency Detector mode, the TMR functions in the following scenarios:

- Rising Edge: The output will go HIGH if the time between two rising edges is less than the delay.
  The output will go LOW if the next rising edge has not come after the last rising edge in specified time.
- Falling Edge: The output will go HIGH if the time between two falling edges is less than the set time.
  The output will go LOW if the next falling edge has not come after the last falling edge in specified time.
- Both Edges: The output will go HIGH if the time between the rising and falling edges is less than the set time, which is equivalent to the length of the pulse.
  The output will go LOW if the next rising/falling edge has not come after the last falling/rising edge in specified time.

The timing diagrams of the Frequency Detector Mode are shown in Figure 9.20…Figure 9.25.

In Edge Detector mode, the TMR generates short high level pulse (for non-inverted polarity) when detecting the respective selected edge event (rising edge, falling edge, both edges). The timing diagrams of this mode are shown in Figure 9.26.

Time of Timers for each mode can be calculated using the following formulas (Note 8.9, Note 8.10):

- Delay (Figure 9.2…Figure 9.7)
  Delay Time = (Control Data + 1 + VAR) / F_{CLK};
- Counter Figure 9.8…Figure 9.13)
  Output Period = (Control Data + 1) / F_{CLK};
  Output Frequency = F_{CLK} / (Control Data + 1);
- One Shot (Figure 9.14…Figure 9.19)
  Pulse width = (Control Data + 1 + VAR) / F_{CLK};
- Frequency Detector (Figure 9.20…Figure 9.25)
  Detected Frequency = F_{CLK} / (Control Data + 1 + VAR).

Note 9.1 *F_{CLK} – CLK input frequency.*

Note 9.2 *VAR = 0…1 – defined by the asynchronous time between the input signal and the first clock pulse.*

Note 9.3 *Counters initialize with Control Data after POR.*

There is also one Multifunctional Macrocell that can implement either 4-bit LUT or 16-bit TMR (See Section 8.4 MF (4-bit LUT0 / 16-Bit Timer) Macrocells).

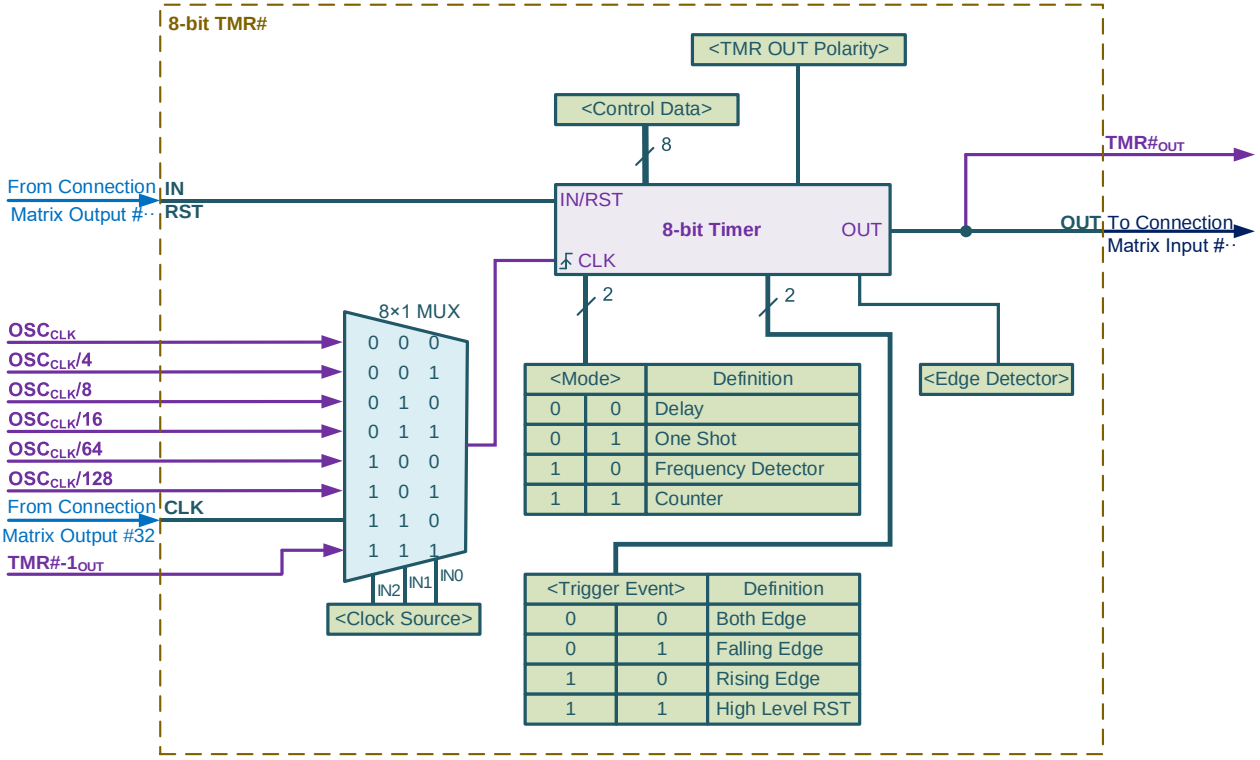


Figure 9.1. Timers

9.1. TMR Timing Diagrams

9.1.1. Delay Mode (Control Data: 4)

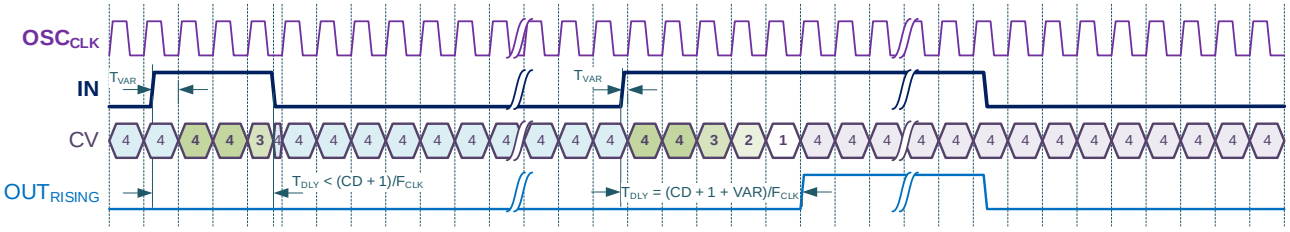


Figure 9.2. Delay Mode Timing Diagram (Rising Edge Detect, Forced OSC)

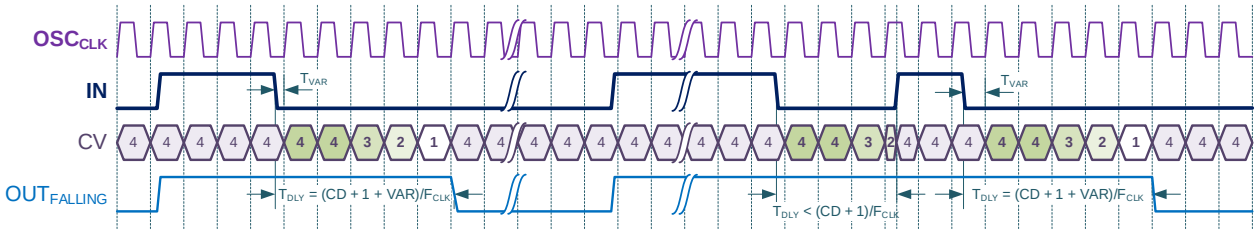


Figure 9.3. Delay Mode Timing Diagram (Falling Edge Detect, Forced OSC)

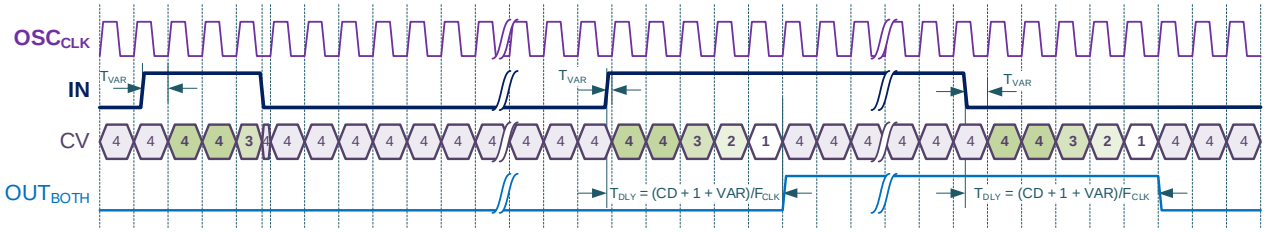


Figure 9.4. Delay Mode Timing Diagram (Both Edge Detect, Forced OSC)

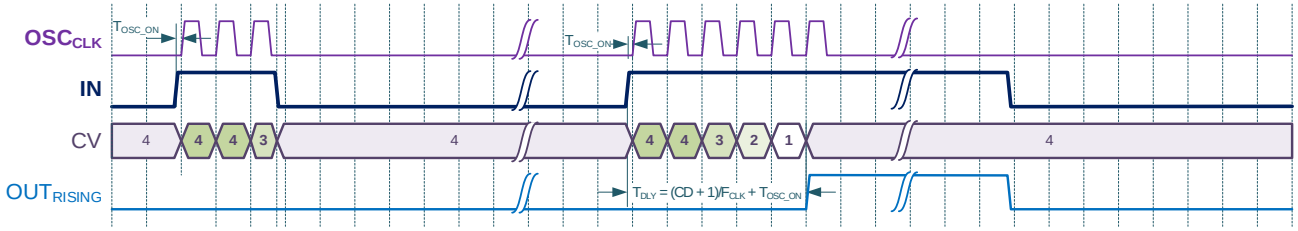


Figure 9.5. Delay Mode Timing Diagram (Rising Edge Detect, Auto OSC)

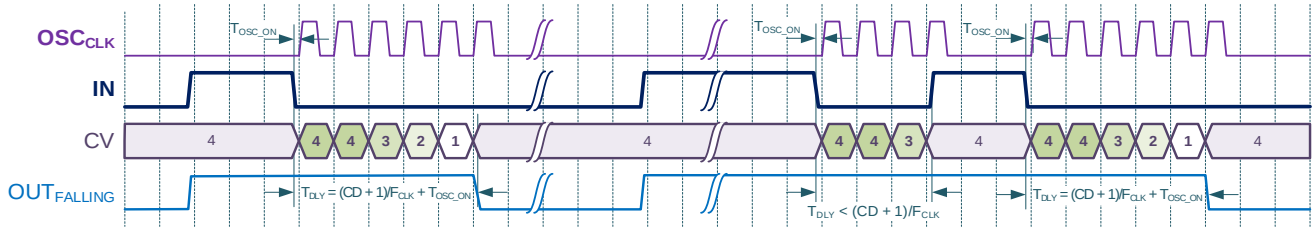


Figure 9.6. Delay Mode Timing Diagram (Falling Edge Detect, Auto OSC)

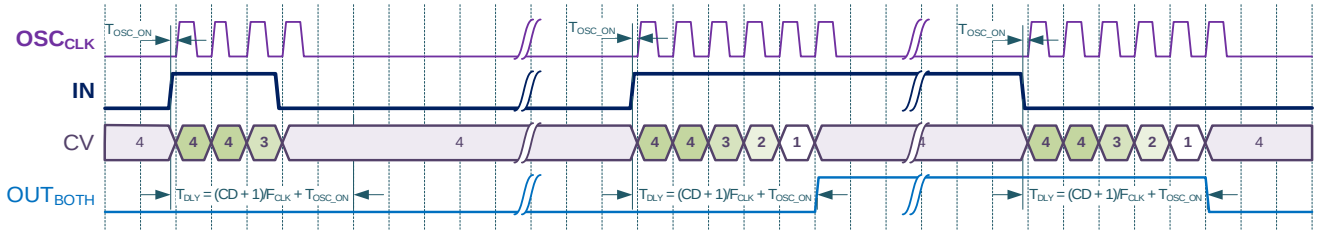


Figure 9.7. Delay Mode Timing Diagram (Both Edge Detect, Auto OSC)

9.1.2. Counter Mode (Control Data: 4)

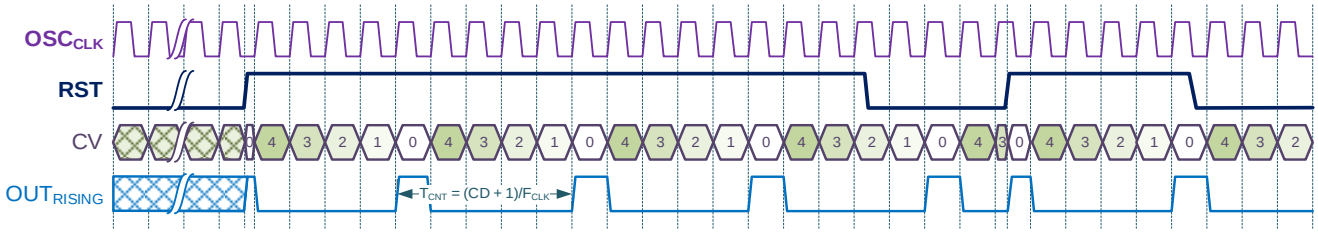


Figure 9.8. Counter Mode Timing Diagram (TMR0, TMR1, Rising Reset, Forced OSC, Auto OSC)

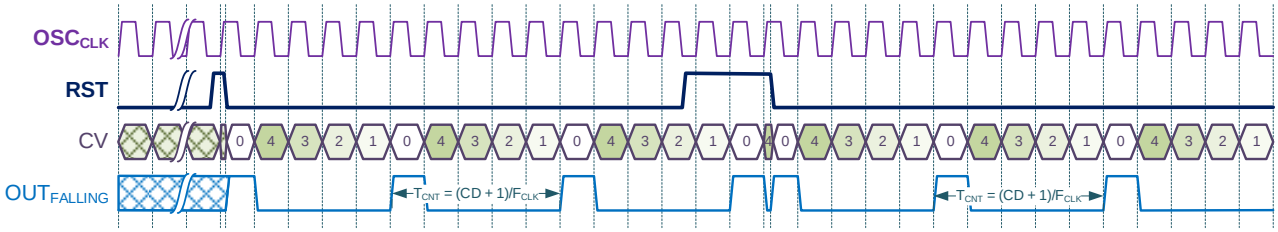


Figure 9.9. Counter Mode Timing Diagram (TMR0, TMR1, Falling Reset, Forced OSC, Auto OSC)

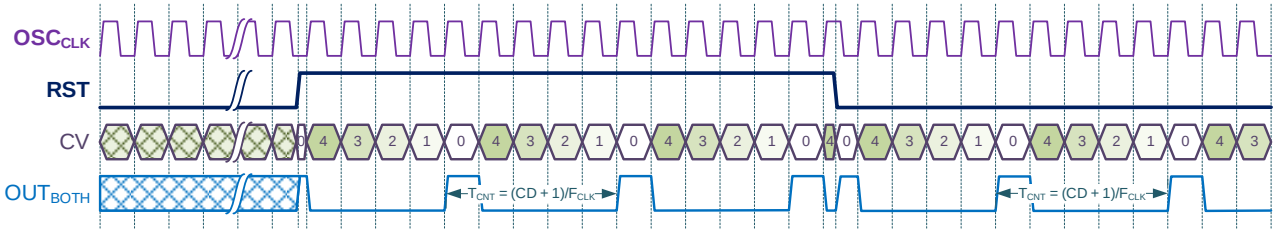


Figure 9.10. Counter Mode Timing Diagram (TMR0, TMR1, Both Edge Reset, Forced OSC, Auto OSC)

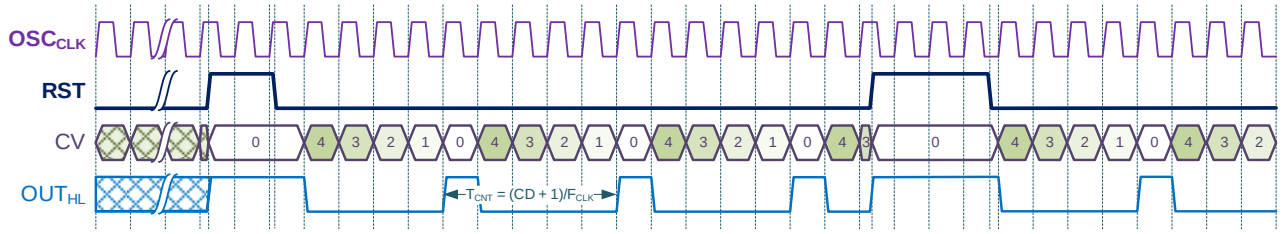


Figure 9.11. Counter Mode Timing Diagram (TMR0, TMR1, High Level Reset, Forced OSC)

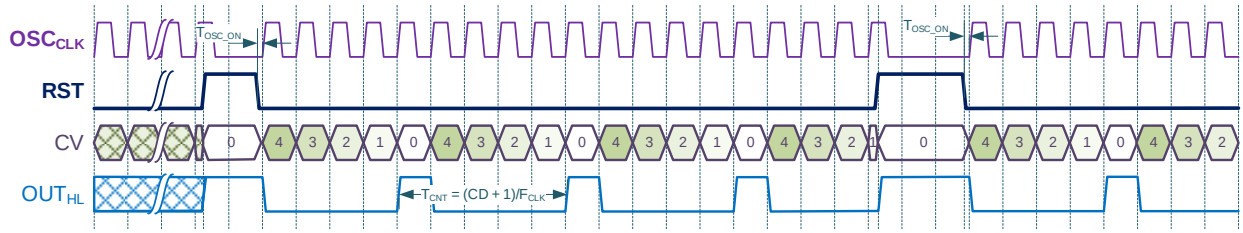


Figure 9.12. Counter Mode Timing Diagram (TMR0, TMR1, High Level Reset, Auto OSC)

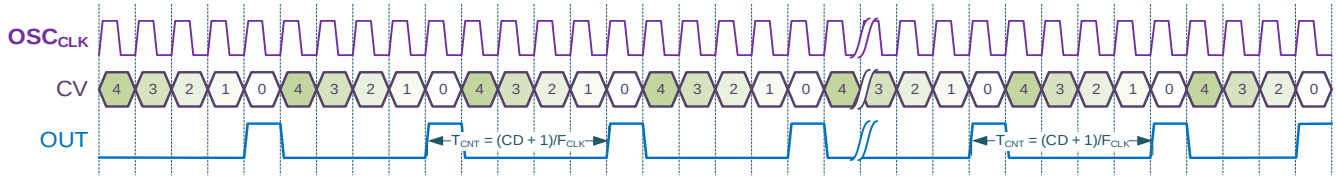


Figure 9.13. Counter Mode Timing Diagram (TMR3, Auto OSC, Forced OSC)

9.1.3. One-Shot Generator Mode (Control Data: 4)

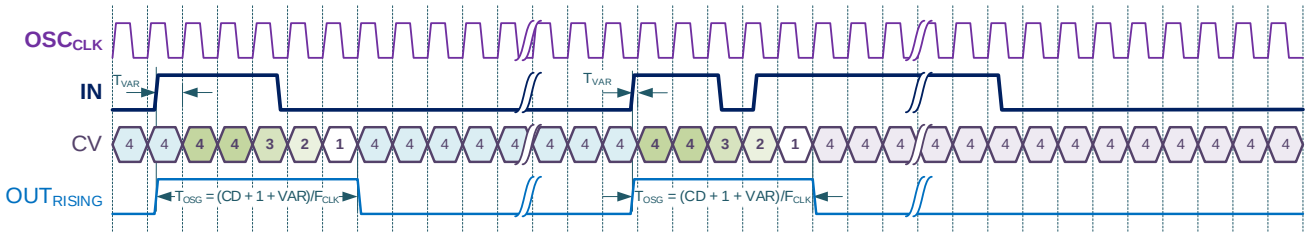


Figure 9.14. One-Shot Generator Mode Timing Diagram (Rising Edge, Forced OSC)

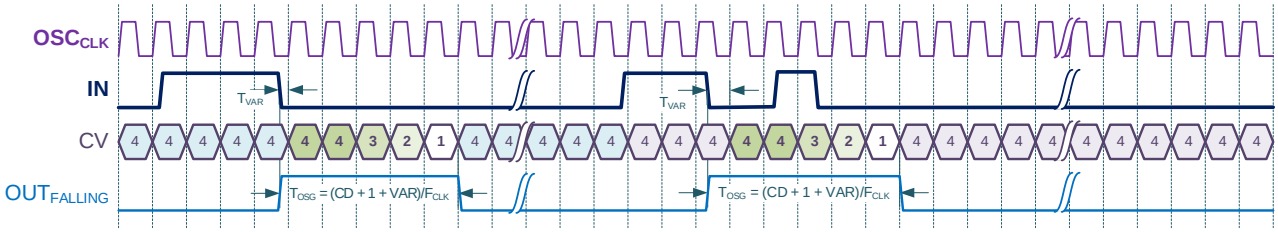


Figure 9.15. One-Shot Generator Mode Timing Diagram (Falling Edge, Forced OSC)

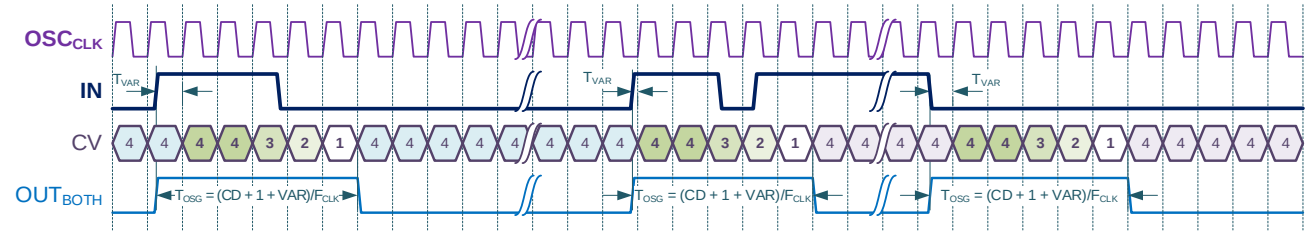


Figure 9.16. One-Shot Generator Mode Timing Diagram (Both Edge, Forced OSC)

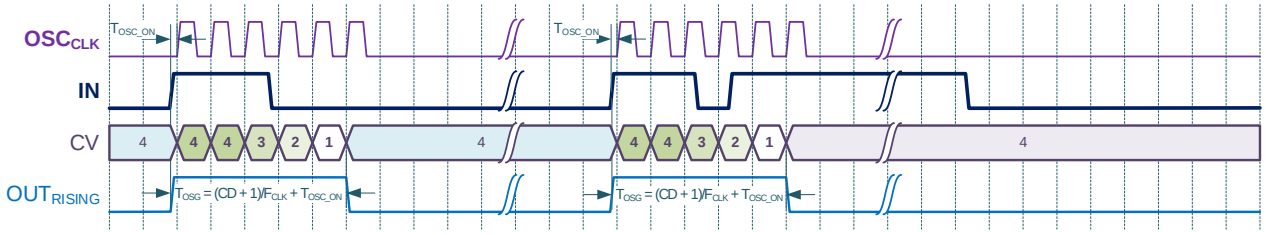


Figure 9.17. One-Shot Generator Mode Timing Diagram (Rising Edge, Auto OSC)

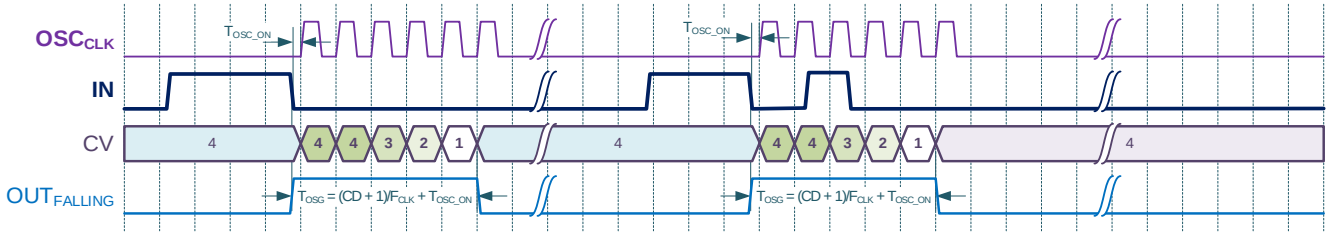


Figure 9.18. One-Shot Generator Mode Timing Diagram (Falling Edge, Auto OSC)

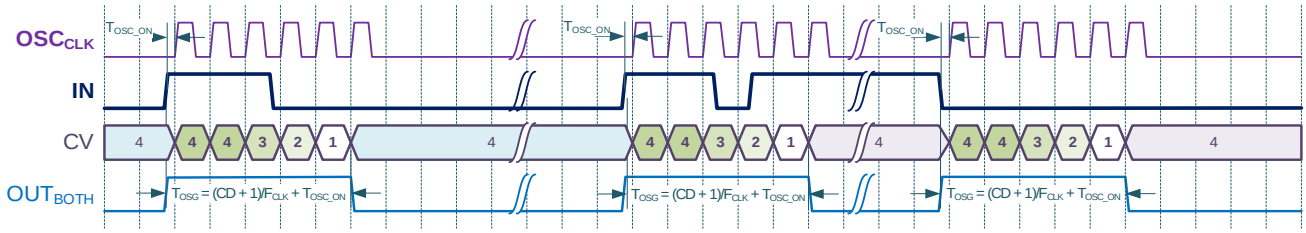


Figure 9.19. One-Shot Generator Mode Timing Diagram (Both Edge, Auto OSC)

9.1.4. Frequency Detector Mode (Control Data: 4)

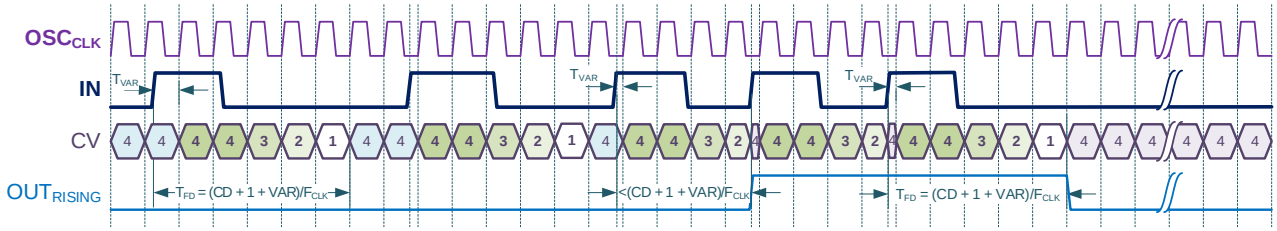


Figure 9.20. Frequency Detector Mode Timing Diagram (Rising Edge, Forced OSC)

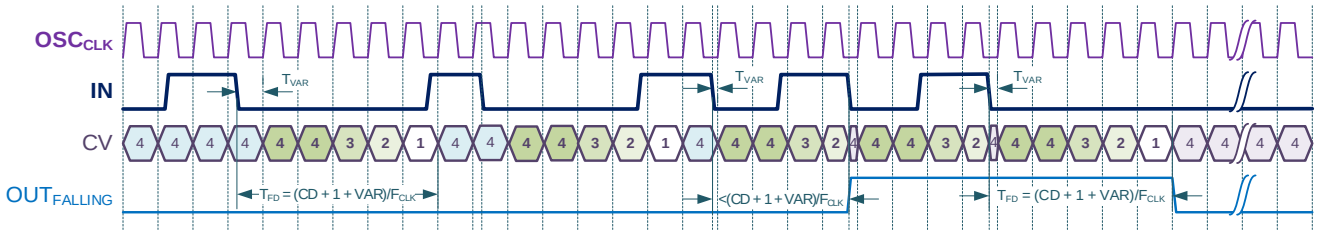


Figure 9.21. Frequency Detector Mode Timing Diagram (Falling Edge, Forced OSC)

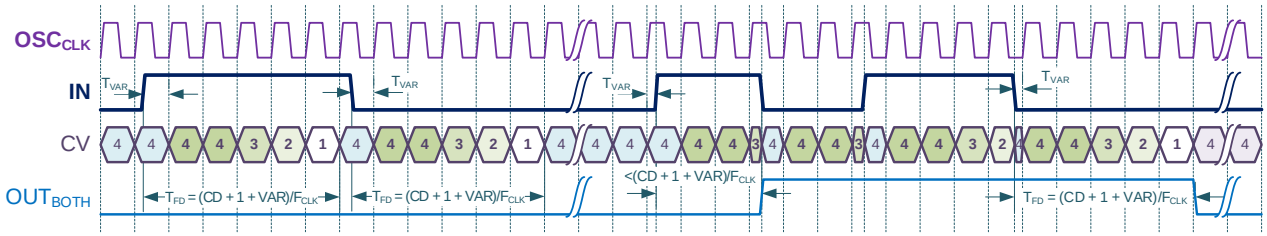


Figure 9.22. Frequency Detector Mode Timing Diagram (Both Edge, Forced OSC)

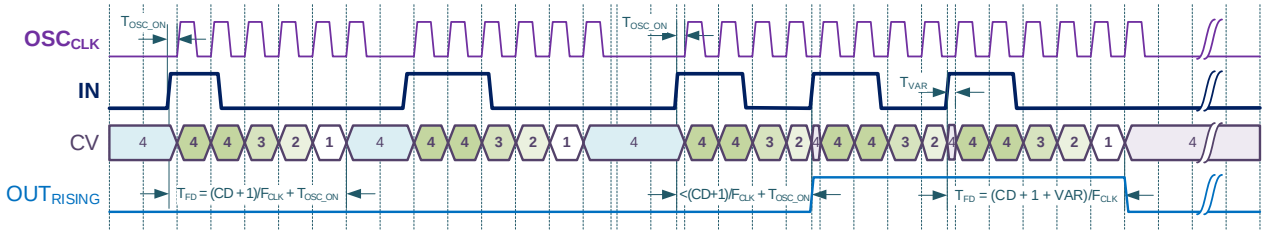


Figure 9.23. Frequency Detector Mode Timing Diagram (Rising Edge, Auto OSC)

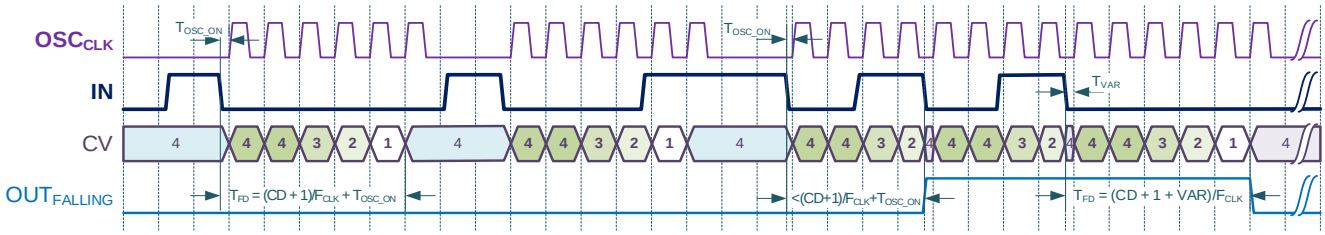


Figure 9.24. Frequency Detector Mode Timing Diagram (Falling Edge, Auto OSC)

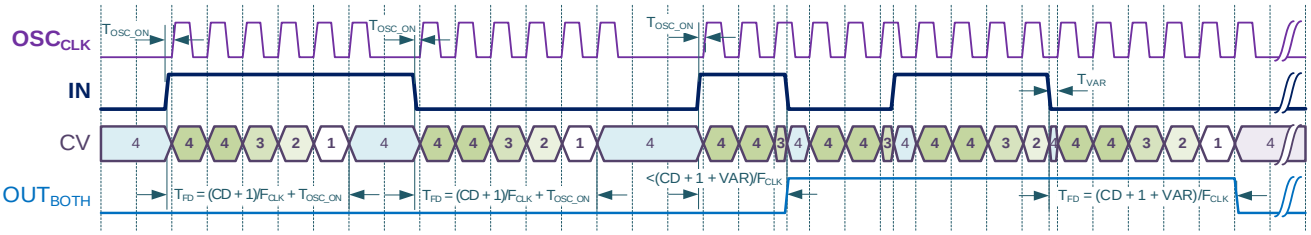


Figure 9.25. Frequency Detector Mode Timing Diagram (Both Edge, Auto OSC)

9.1.5. Edge Detector Mode TMR0, TMR1, TMR3 (EDGE out)

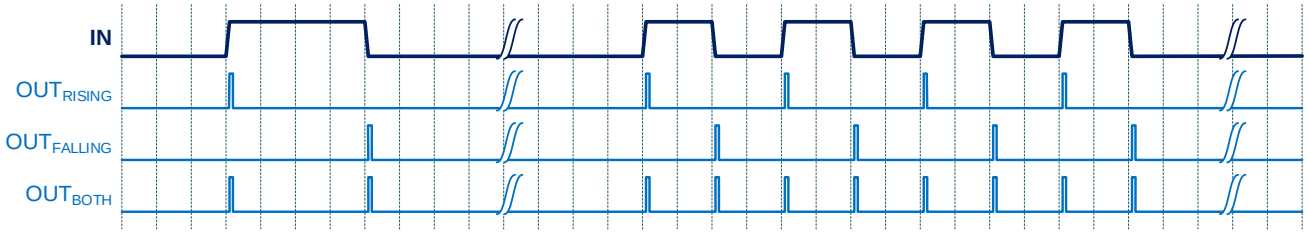


Figure 9.26. Edge Detector Mode Timing Diagram

9.1.6. Counter Mode TMR2 (Control Data: 4)

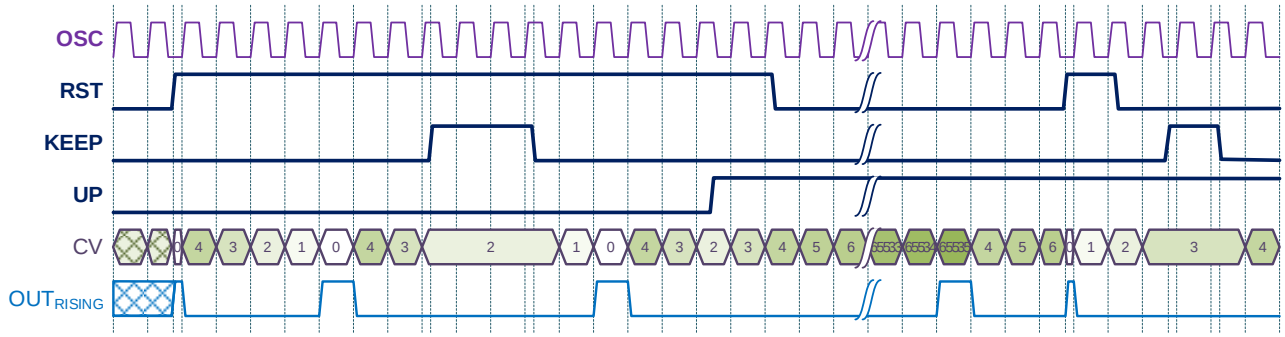


Figure 9.27. TMR2 Counter Mode Timing Diagram (Rising Reset, Forced OSC)

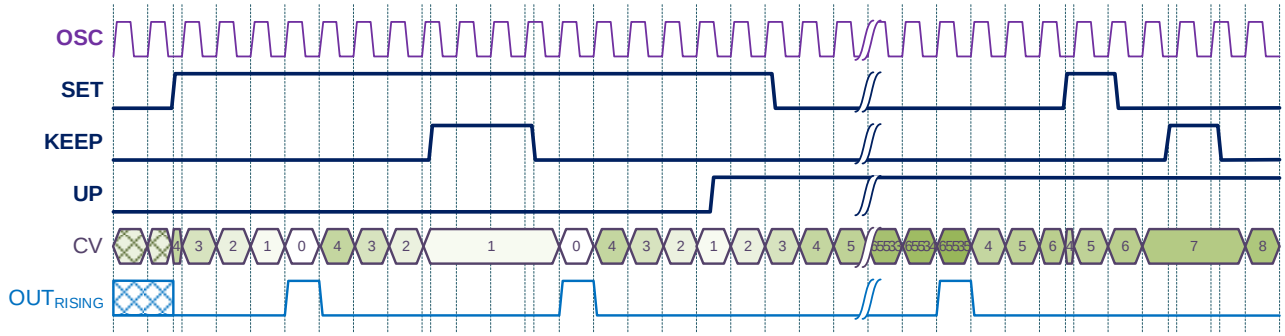


Figure 9.28. TMR2 Counter Mode Timing Diagram (Rising Set, Forced OSC)

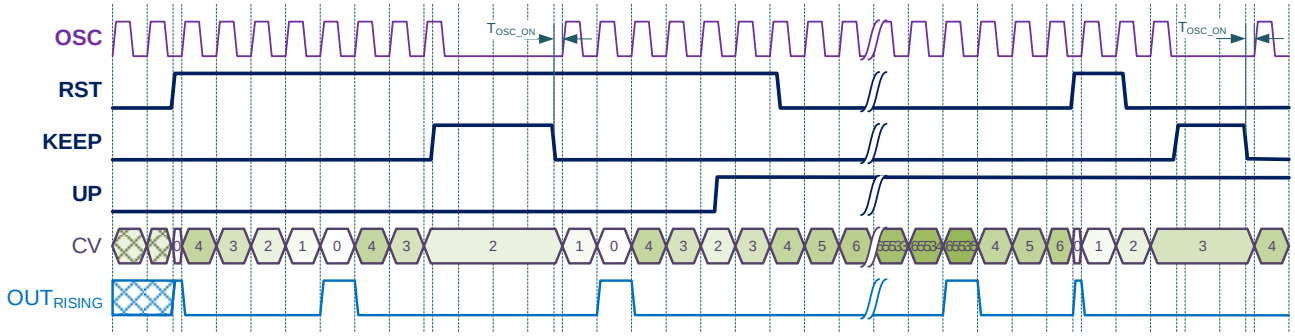


Figure 9.29. TMR2 Counter Mode Timing Diagram (Rising Reset, Auto OSC)

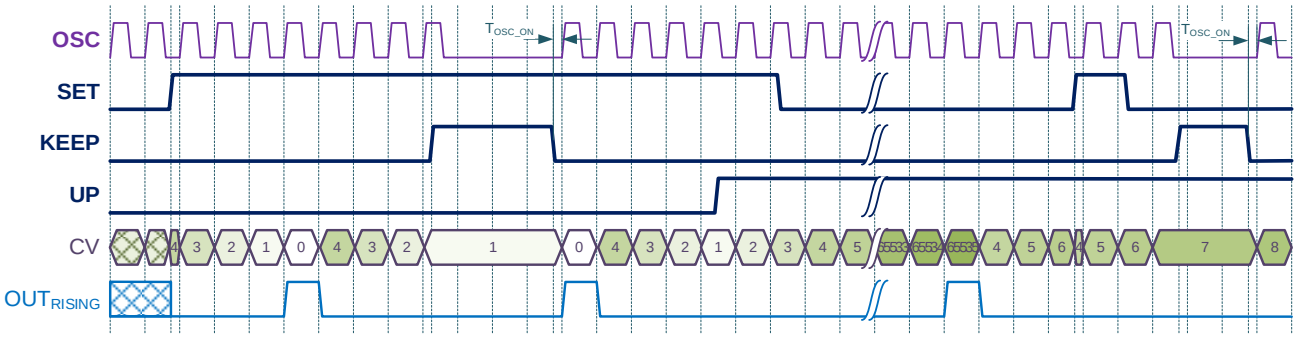


Figure 9.30. TMR2 Counter Mode Timing Diagram (Rising Set, Auto OSC)

9.2. 8-bit TMR0

Schematic diagram of TMR0 macrocell is shown in Figure 9.1. Its register settings set out in Table 9.1.

Table 9.1. TMR0 Register Settings

Signal Function	Register Bit Address	Register Definition
TMR Control Data	<350:343>	1-255: (Delay Time = (Control Data +1) / Frequency)
TMR Mode selection	<352:351>	00: Delay Mode 01: One Shot 10: Frequency Detector 11: Counter mode

Signal Function	Register Bit Address	Register Definition
TMR Clock Source selection	<355:353>	000: OSC_{CLK} 001: OSC_{CLK}/4 010: OSC_{CLK}/8 011: OSC_{CLK}/16 100: OSC_{CLK}/64 101: OSC_{CLK}/128 110: External CLK 111: $TMR3_{OUT}$
TMR Trigger Event selection	<357:356>	00: On Both Falling and Rising Edges 01: On Falling Edge only 10: On Rising Edge only 11: No Delay on either Falling or Rising Edges for Delay Mode / High Level Reset for Counter Mode
TMR Edge Detector Output selection	<358>	0: Default Output 1: Edge Detector Output
TMR Output polarity selection	<359>	0: Non-Inverted (OUT) 1: Inverted (nOUT)

9.3. 8-bit TMR1

Schematic diagram of TMR1 macrocell is shown in Figure 9.1. Its register settings set out in Table 9.2.

Table 9.2. TMR1 Register Settings

Signal Function	Register Bit Address	Register Definition
TMR Control Data	<367:360>	1-255: (Delay Time = (Control Data +1) / Frequency)
TMR Mode selection	<379:378>	00: Delay Mode 01: One Shot 10: Frequency Detector 11: Counter Mode
TMR Clock Source selection	<382:380>	000: OSC_{CLK} 001: OSC_{CLK}/4 010: OSC_{CLK}/8 011: OSC_{CLK}/16 100: OSC_{CLK}/64 101: OSC_{CLK}/128 110: External CLK 111: $TMR0_{OUT}$
TMR Trigger Event selection	<384:383>	00: On Both Falling and Rising Edges 01: On Falling Edge only 10: On Rising Edge only 11: No Delay on either Falling or Rising Edges for Delay Mode / High Level Reset for Counter Mode
TMR Edge Detector Output selection	<385>	0: Default Output 1: Edge Detector Output
TMR Output polarity selection	<386>	0: Non-Inverted (OUT) 1: Inverted (nOUT)

9.4. 8-bit TMR3

Schematic diagram of TMR3 macrocell is shown on Figure 9.31. Its register settings set out in

Table 9.3.

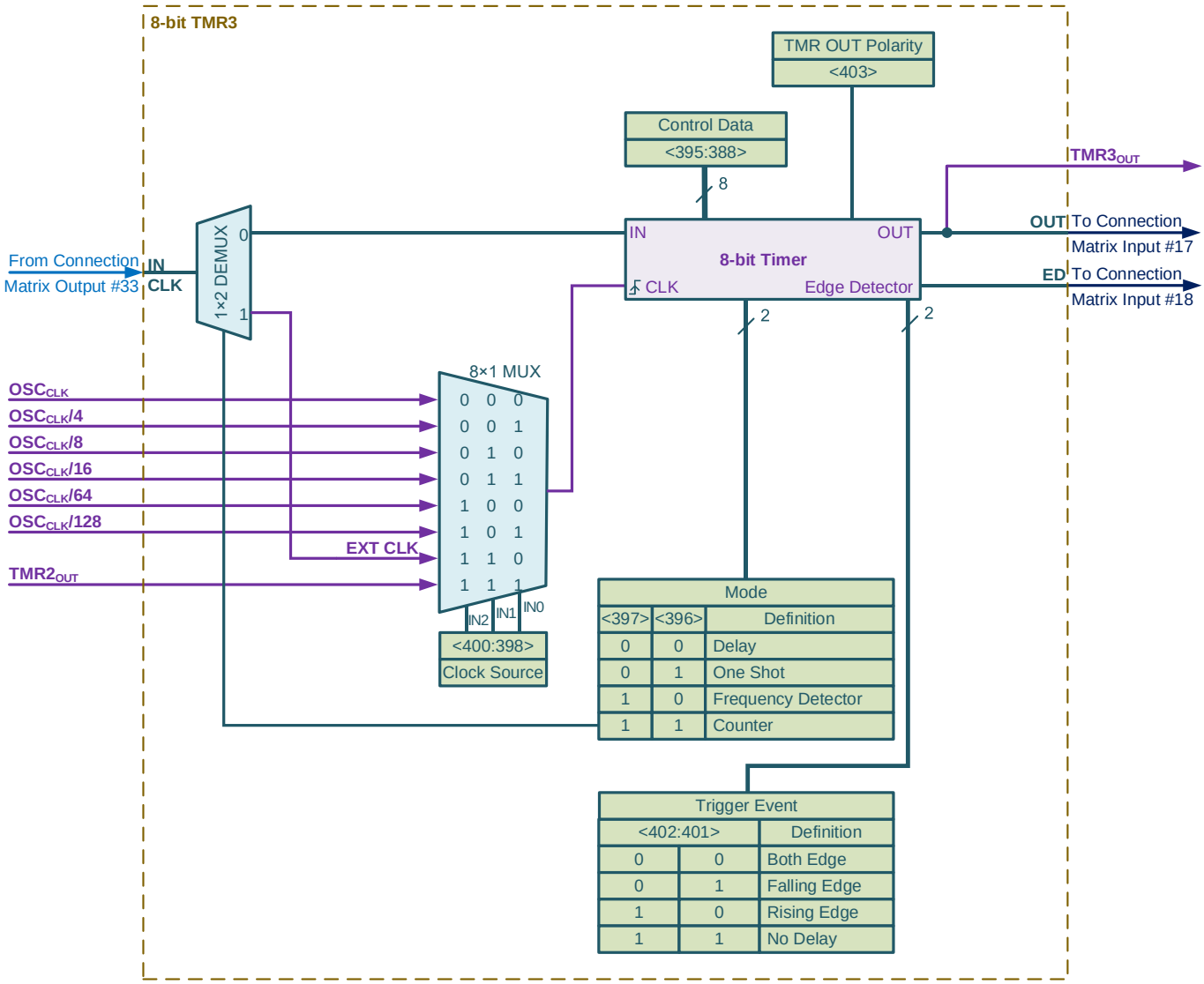


Figure 9.31. TMR3

Table 9.3. TMR3 Register Settings

Signal Function	Register Bit Address	Register Definition
TMR Control Data	<395:388>	1-255: (Delay Time = (Control Data +1) / Frequency)
TMR Mode selection	<397:396>	00: Delay Mode 01: One Shot 10: Frequency Detector 11: Counter Mode
TMR Clock Source selection	<400:398>	000: OSC_{CLK} 001: OSC_{CLK}/4 010: OSC_{CLK}/8 011: OSC_{CLK}/16 100: OSC_{CLK}/64 101: OSC_{CLK}/128 110: External CLK 111: $TMR2_{OUT}$
TMR Edge selection	<402:401>	00: Delay on Both Falling and Rising Edges for Delay Mode 01: Delay on Falling Edge only for Delay Mode 10: Delay on Rising Edge only for Delay Mode 11: No Delay on either Falling or Rising Edges for Delay Mode
TMR Output polarity selection	<403>	0: Non-Inverted (OUT) 1: Inverted (nOUT)

10. Memory Architecture

The Memory of µASIC consists of two main parts: non-volatile memory (NVM) and registers. The configuration of the µASIC is stored in the NVM and is loaded to the volatile registers during device power on. The registers' values define macrocells configuration, matrix connections setting (signal routing), IO configuration etc., which allows desired functionality for the user's application (see Figure 10.1).

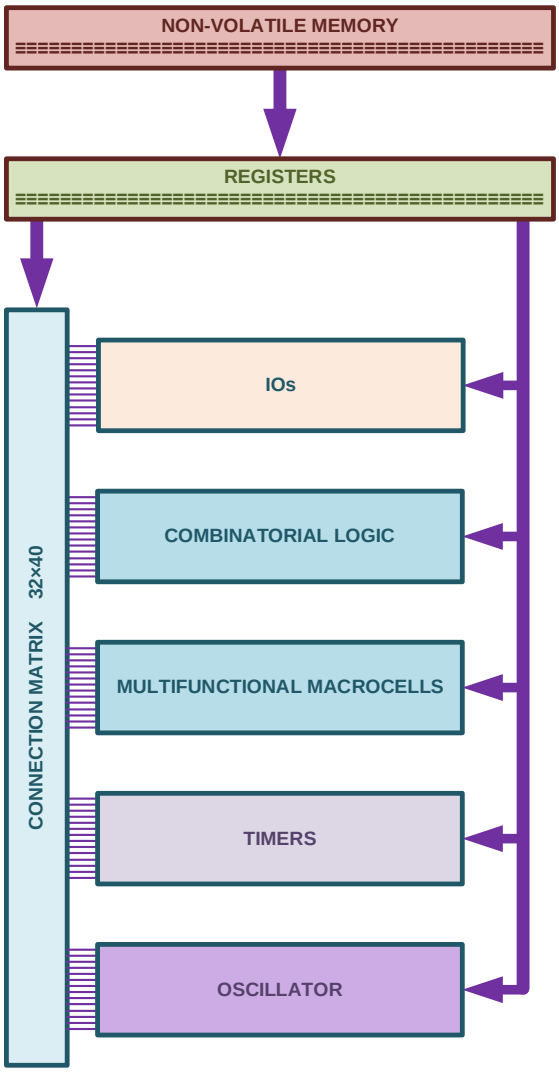


Figure 10.1. Memory Architecture

11. Data Protection

The ALM1108 has two stages of data protection, which is provided by CRC-8 and CRV.

11.1. CRC-8

Validity of correct NVM programming and NVM loading to the registers is checked by CRC-8. So, if the CRC-8 is Enabled and no errors are detected, the ALM1108 starts working. Otherwise, the chip will restart. Used CRC polynomial is $x^8 + x^6 + x^3 + 1$

Table 11.1. CRC-8 Register Settings

Signal Function	Register Bit Address	Register Definition
CRC-8 Enable	<457>	0: Disable 1: Enable
CRC-8	<214:207>	CRC polynomial is $x^8 + x^6 + x^3 + 1$

11.2. CRV

Continuous Registers Verification (CRV) is provided by a continuous comparison of the register bits <501, 411, 377, 376, 368, 342, 327, 219, 191, 140, 84, 43, 42, 41, 15> with hardcoded value 15'b011001100001101. If the comparison shows a mismatch, the ALM1108 automatically restarts.

Table 11.2. CRV Register Settings

Signal Function	Register Bit Address	Register Definition
Continuous Registers Verification Enable	<456>	0: Disable 1: Enable

12. Oscillator (OSC)

12.1. Oscillator Overview

ALM1108 has an internal Oscillator with two selectable frequencies: 25 kHz and 2 MHz. OSC macrocell can be sourced from internal oscillator or by external frequency from IO8.

The OSC has two prescaler stages that give user flexibility for introducing clock signals on the Connection Matrix Input lines. The first stage ($CLK_{Prescale}$) allows to divide the fundamental frequency by **/1**, **/2**, **/4**, or **/8**. The two independent second stage prescaler allow to divide the frequency from the first stage divider by **/1**, **/4**, **/8**, **/16, /32, /64**, or **/128**, and outputs this frequency on the Connection Matrix Input #20 and #21 (See Figure 12.1 for more details).

When internal OSC is used, there is a choice between “Force Power On”, meaning that the OSC will always run, or “Auto Power On”, meaning that the OSC will run only on demand of internal logics (TMRs) and consequently have an associated startup and settling time.

The oscillator is turned on when the PWRDWN signal is LOW and turned off when the PWRDWN signal is HIGH. The PWRDWN signal has the highest priority.

12.2. OSC (25kHz / 2MHz)

Schematic diagram of the OSC macrocell is shown in Figure 12.1. Its register settings set out in Table 12.1.

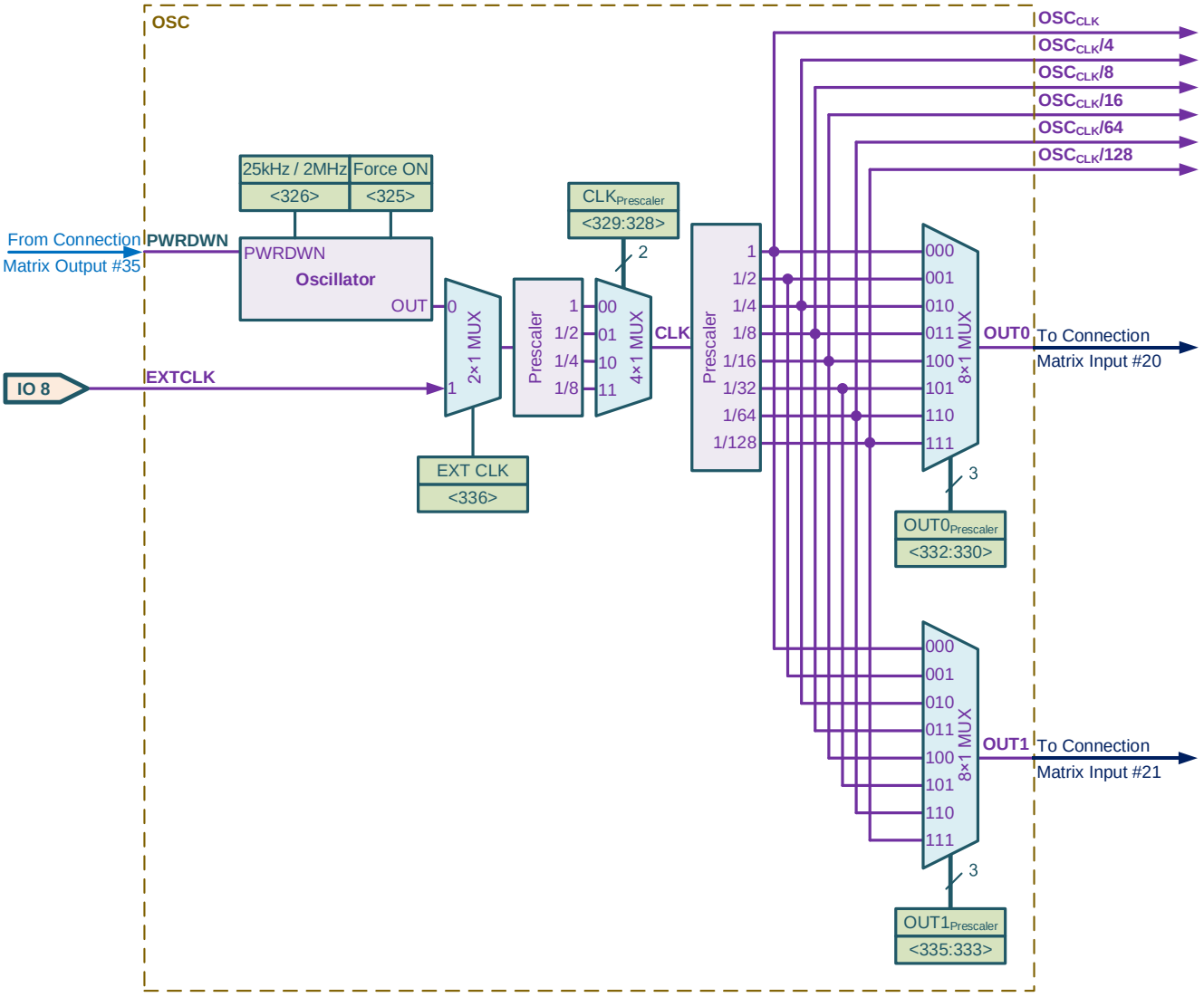


Figure 12.1. OSC Block Diagram

Table 12.1. OSC Register Settings

Signal Function	Register Bit Address	Register Definition
Frequency selection	<326>	0: 25kHz 1: 2MHz
Force ON	<325>	0: Auto power on 1: Force on
Clock Source selection	<336>	0: Inner oscillator 1: External CLK (IO8)
$CLK_{Prescale}$ selection	<329:328>	00: 1 01: 1/2 10: 1/4 11: 1/8
$OUT0_{Prescaler}$ selection	<332:330>	000: 1 001: 1/2 010: 1/4 011: 1/8 100: 1/16 101: 1/32 110: 1/64 111: 1/128
$OUT0_{Prescaler}$ selection	<335:333>	000: 1 001: 1/2 010: 1/4 011: 1/8 100: 1/16 101: 1/32 110: 1/64 111: 1/128

13. Power On Reset (POR)

To ensure correct device initialization and operation of all macrocells in the device, the µASIC has a Power-On Reset (POR) circuit. The POR circuit achieves consistent behavior and predictable results during VDD power ramp up and power down. To accomplish this goal, the POR circuit releases a defined Power-Up sequence of internal events that initialize different macrocells inside the device.

13.1. POR General Operation

To start the Power-Up sequence, the voltage applied on the VDD should be higher than the POWER ON threshold (which can vary by PVT, but typical is 1.6 V). The operational V_{DD} range for the ALM1108 is 1.71V…3.60V. Therefore, the Power-Up sequence will start earlier, as soon as the V_{DD} rises to the POWER ON threshold, but the VDD voltage itself must continue to ramp up to the operational voltage value. After the POR sequence has started, ALM1108 will have a period of time to go through all the steps in the sequence and will be ready and completely operational after the Power-Up sequence is completed.

ALM1108 is powered down and non-operational when the VDD voltage is between 0.6 V and -0.6 V. Another essential condition for the chip to be powered down is that no voltage higher than the VDD voltage is applied to any other pin (although there is a 0.5 V margin due to forward drop voltage of the ESD protection diodes).

All pins are in HIGH IMPEDANCE state while the Power-Up sequence is taking place, and when the chip is powered down. The last step in the Power-Up sequence releases the I/O structures from the HIGH IMPEDANCE state making the device operational. The design programmed into the chip defines the pin configuration of the device when operational. (The voltage on pins can't be higher than the VDD and this rule does apply to when the chip is powered on).

13.2. Power-Up Sequence

The Power-Up sequence of signals is shown in Figure 13.1.

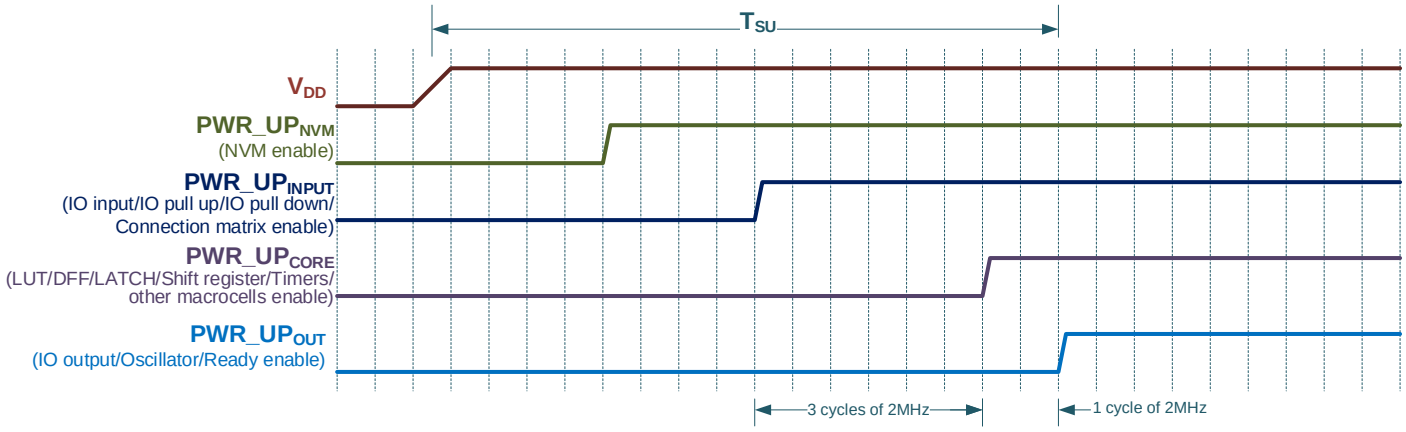


Figure 13.1. POR sequence

As demonstrated by Figure 13.1 after the V_{DD} starts ramping up and crosses the POWER ON threshold, the on-chip NVM memory is enabled. After that, Input pins and Connection Matrix are enabled and all traces between all macrocells are routed. The macrocells like LUT, DFF, LATCH, Shift Register, Timers and others are initialized and stabilized for the next 3 cycles of 2MHz oscillator. After another one cycle, READY signal and OSC outputs are enabled and outputs start to run. The output pins transition from HIGH IMPEDANCE to active at this point.

The completion time for the POR sequence varies by device type in the µASIC family. The completion time also depends on many environmental factors, such as: slew rate, V_{DD} value, and temperature to a degree that the times will even vary from chip to chip due to process influence.

13.3. Macrocells Output States During Power-Up Sequence

First, all macrocells have their output set to logic LOW, except the output pins which are in HIGH IMPEDANCE state, before the NVM is enabled. Then until the NVM is ready, all macrocell outputs are unpredictable except the IOs. On the next step Input pins determined by external signals, LOGIC 1 is high, LOGIC 0 is low, LUTs and PDLY macrocell configured as edge detector work according to their inputs. All other macrocells are initialized in the next step. Lastly, READY signal, oscillator and the output pins become active as determined by the input signals. (Figure 13.2 describes the macrocell output signal states during the Power-Up sequence).

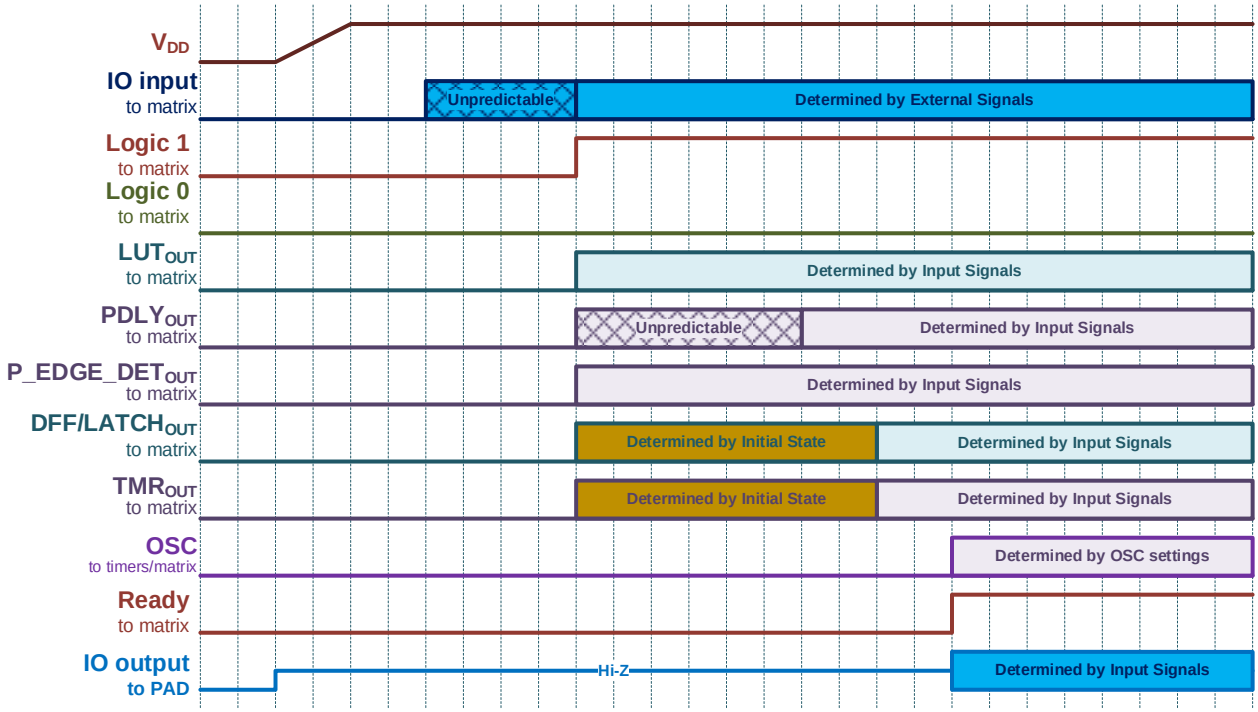


Figure 13.2. Internal Macrocell States during POR sequence

13.4. Reset Events

There are a number of reset events for ALM1108:

- POR;
- CRC-8;
- CRV;
- IO2 Reset.

The CRC-8 (see section 11.1), CRV (see section 11.2), and IO2 Reset can be enabled or disabled by register bits (Table 13.1). Keep in mind that IO2 should be configured as Digital IN (any of the input modes) as long as IO2 Reset is enabled.

Table 13.1. IO2 Reset Register Settings

Signal Function	Register Bit Address	Register Definition
IO2 Reset Trigger Event selection	<498:497>	00: Rising Edge 01: Falling Edge 10: High Level 11: Reserved
IO2 Reset Enable	<499>	0: Disable 1: Enable

14. Abbreviations

ADJ	Adjustable
ASIC	Application-Specific Integrated Circuit
CLK	Clock
CLK/L	Clock/Latch
CRC	Cyclic Redundancy Code
CRV	Continuous Registers Verification
CM	Connection Matrix
CMI	Connection Matrix Inputs
CMO	Connection Matrix Outputs
CV	Counted Value
D	Data
DC	Direct Current
DFF	D Flip-Flop
DI	Digital Input
DIR	Direction
DILV	Digital Input Low Voltage
DIO	Digital Input/Output
ED	Edge Detector
ESD	Electrostatic Discharge
EXTCLK	External Clock
FSM	Finite State Machine
GND	Ground
IC	Integrated Circuit
IMC	Input Mode Control
IN	Input
I/O	Input/Output
Logic 0	Low Logic Level
Logic 1	High Logic Level
LSB	Least Significant Bit
LUT	Look Up Table
LV	Low Voltage
MF	Multi-Functional
MSB	Most Significant Bit
MUX	Multiplexer
N/A	Not Applicable
N/C	Not Connected
NMOS	N channel Metal Oxide Semiconductor
NVM	Non-Volatile Memory
OD	Open Drain
OSC	Oscillator
OSG	One Shot Generator
OUT	Output
PDLY	Programmable Delay
PMOS	P channel Metal Oxide Semiconductor
POD	Power On Delay
POR	Power On Reset
PP	Push Pull
PROP	Propagation
PW	Pulse Width
PWRDWN	Power Down
REG	Register
RST	Reset
SHR	Shift Register
ST	Schmitt Trigger
TMR	Timer
TQFN	Thin Quad Flat No Leads
VDD	Voltage Drain-Drain
VSS	Voltage Source-Source
w/	With
w/o	Without

15. Appendix A – ALM1108 Register Definition

Register Bit Address	Signal Function	Register Definition
<4:0>	Matrix Output Number 0	IO3 DIN
<9:5>	Matrix Output Number 1	IO4 DIN
<14:10>	Matrix Output Number 2	IO4 Output EN
<15>	Bit 0 CRV	1
<20:16>	Matrix Output Number 3	IN0 of 2-bit LUT0 or CLK of DFF0 or L of LATCH0
<25:21>	Matrix Output Number 4	IN1 of 2-bit LUT0 or D of DFF0/LATCH0
<30:26>	Matrix Output Number 5	IN0 of 2-bit LUT1 or CLK of DFF1 or L of LATCH1
<35:31>	Matrix Output Number 6	IN1 of 2-bit LUT1 or D of DFF1/LATCH1
<40:36>	Matrix Output Number 7	IN0 of 2-bit LUT2
<41>	Bit 1 CRV	0
<42>	Bit 2 CRV	1
<43>	Bit 3 CRV	1
<48:44>	Matrix Output Number 8	IN1 of 2-bit LUT2
<53:49>	Matrix Output Number 9	IN0 of 2-bit LUT3
<58:54>	Matrix Output Number 10	IN1 of 2-bit LUT3
<63:59>	Matrix Output Number 11	IN0 of 3-bit LUT0 or CLK of DFF2 or L of LATCH2
<68:64>	Matrix Output Number 12	IN1 of 3-bit LUT0 or D of DFF2/LATCH2
<73:69>	Matrix Output Number 13	IN2 of 3-bit LUT0 or nRST(nSET) of DFF2/LATCH2
<78:74>	Matrix Output Number 14	IN0 of 3-bit LUT1 or CLK of DFF3 or L of LATCH3
<83:79>	Matrix Output Number 15	IN1 of 3-bit LUT1 or D of DFF3/LATCH3
<84>	Bit 4 CRV	0
<89:85>	Matrix Output Number 16	IN2 of 3-bit LUT1 or nRST(nSET) of DFF3/LATCH3
<94:90>	Matrix Output Number 17	IN0 of 3-bit LUT2 or CLK of DFF4 or L of LATCH4
<99:95>	Matrix Output Number 18	IN1 of 3-bit LUT2 or D of DFF4/LATCH4
<104:100>	Matrix Output Number 19	IN2 of 3-bit LUT2 or nRST(nSET) of DFF4/LATCH4
<109:105>	Matrix Output Number 20	IN0 of 3-bit LUT3 or CLK of DFF5 or L of LATCH5
<114:110>	Matrix Output Number 21	IN1 of 3-bit LUT3 or D of DFF5/LATCH5
<119:115>	Matrix Output Number 22	IN2 of 3-bit LUT3 or nRST(nSET) of DFF5/LATCH5
<124:120>	Matrix Output Number 23	IN0 of 3-bit LUT4 or D of Shift Register
<129:125>	Matrix Output Number 24	IN1 of 3-bit LUT4 or nRST of Shift Register
<134:130>	Matrix Output Number 25	IN2 of 3-bit LUT4 or CLK of Shift Register
<139:135>	Matrix Output Number 26	IN0 of 4-bit LUT0 or CLK of TMR2
<140>	Bit 5 CRV	0
<145:141>	Matrix Output Number 27	IN1 of 4-bit LUT0 or IN of TMR2 (RST for Counter Mode)
<150:146>	Matrix Output Number 28	IN2 of 4-bit LUT0 or KEEP of TMR2
<155:151>	Matrix Output Number 29	IN3 of 4-bit LUT0 or UP of TMR2
<160:156>	Matrix Output Number 30	IN of TMR0 (RST for Counter Mode)
<165:161>	Matrix Output Number 31	IN of TMR1 (RST for Counter Mode)
<170:166>	Matrix Output Number 32	CLK of TMR0/TMR1
<175:171>	Matrix Output Number 33	IN of TMR3 (RST for Counter Mode)
<180:176>	Matrix Output Number 34	IN of PDLY
<185:181>	Matrix Output Number 35	PWRDWN of OSC (Higher Priority) (HIGH is Power Down)
<190:186>	Matrix Output Number 36	IO6 DIN
<191>	Bit 6 CRV	0
<196:192>	Matrix Output Number 37	IO7 DIN
<201:197>	Matrix Output Number 38	IO8 DIN
<206:202>	Matrix Output Number 39	IO8 Output EN
CRC		
<214:207>	CRC-8	
LUT / DFF/LATCH		
<215>	DFF0 or LATCH0 selection / 2-bit LUT0 <0>	0: DFF function 1: LATCH function
<216>	2-bit LUT0 <1>	

Register Bit Address	Signal Function	Register Definition
<217>	DFF0/LATCH0 initial state selection / 2-bit LUT0 <2>	0: LOW 1: HIGH
<218>	2-bit LUT0 <3>	
<219>	Bit 7 CRV	0
<220>	DFF1 or LATCH1 selection / 2-bit LUT1 <0>	0: DFF function 1: LATCH function
<221>	2-bit LUT1 <1>	
<222>	DFF1/LATCH1 initial state selection / 2-bit LUT1 <2>	0: LOW 1: HIGH
<223>	2-bit LUT1 <3>	
<226:224>	Reserved	
<230:227>	2-bit LUT2 data	
<234:231>	2-bit LUT3 data	
<235>	2-bit LUT0 or DFF0/LATCH0 selection	0: LUT 1: DFF/LATCH
<236>	2-bit LUT1 or DFF1/LATCH1 selection	0: LUT 1: DFF/LATCH
<237>	DFF2 or LATCH2 selection / 3-bit LUT0 OUT0 <0>	0: DFF function 1: LATCH function
<238>	3-bit LUT0 OUT0 <1>	
<239>	DFF2/LATCH2 nRST/nSET selection / 3-bit LUT0 OUT0 <2>	0: nRST from matrix output 1: nSET from matrix output
<240>	DFF2/LATCH2 initial state selection / 3-bit LUT0 OUT0 <3>	0: Low 1: High
<244:241>	3-bit LUT0 OUT0 <7:4>	
<252:245>	3-bit LUT0 OUT1 <7:0>	
<253>	DFF3 or LATCH3 selection / 3-bit LUT1 OUT0 <0>	0: DFF function 1: LATCH function
<254>	3-bit LUT1 OUT0 <1>	
<255>	DFF3/LATCH3 nRST/nSET selection / 3-bit LUT1 OUT0 <2>	0: nRST from matrix output 1: nSET from matrix output
<256>	DFF3/LATCH3 initial state selection / 3-bit LUT 3 OUT0 <3>	0: LOW 1: HIGH
<260:257>	3-bit LUT1 OUT0 <7:4>	
<268:261>	3-bit LUT1 OUT1 <7:0>	
<269>	DFF4 or LATCH4 selection / 3-bit LUT2 <0>	0: DFF function 1: LATCH function
<270>	DFF4/LATCH4 Output selection / 3-bit LUT2 <1>	0: Q output 1: nQ output
<271>	DFF4/LATCH4 nRST/nSET selection / 3-bit LUT2 <2>	0: nRST from matrix output 1: nSET from matrix output
<272>	DFF4/LATCH4 initial state selection / 3-bit LUT2 <3>	0: LOW 1: HIGH
<276:273>	3-bit LUT2 <7:4>	
<277>	DFF5 or LATCH5 selection / 3-bit LUT3 <0>	0: DFF function 1: LATCH function
<278>	DFF5/LATCH5 Output selection / 3-bit LUT3 <1>	0: Q output 1: nQ output
<279>	DFF5/LATCH5 nRST/nSET selection / 3-bit LUT3 <2>	0: nRST from matrix output 1: nSET from matrix output
<280>	DFF5/LATCH5 initial state selection / 3-bit LUT3 <3>	0: LOW 1: HIGH
<284:281>	3-bit LUT3 <7:4>	
3-bit LUT4 / Shift Register		
<288:285>	3-bit LUT4 <3:0> / Shift Register OUT0 selection	
<292:289>	3-bit LUT4 <7:4> / Shift Register OUT1 selection	
<293>	3-bit LUT0 or DFF2/LATCH2 selection	0: LUT 1: DFF
<294>	3-bit LUT1 or DFF3/LATCH3 selection	0: LUT 1: DFF
<295>	3-bit LUT2 or DFF4/LATCH4 selection	0: LUT 1: DFF
<296>	3-bit LUT3 or DFF5/LATCH5 selection	0: LUT 1: DFF

Register Bit Address	Signal Function	Register Definition
<297>	3-bit LUT4 or Shift Register selection	0: LUT 1: Shift Register
<298>	Shift Register OUT1 polarity selection	0: Non-Inverted 1: Inverted
4-bit LUT0 / 16-bit TMR2		
<314:299>	4-bit LUT0 <15:0> or TMR2 Control Data selection	1 – 65535 Delay Time = (Control Data +1)/Freq
<316:315>	TMR2 mode selection	00: Delay Mode 01: One Shot 10: Frequency Detector 11: Counter Mode
<319:317>	TMR2 Clock Source selection	000: OSC_{CLK} 001: OSC_{CLK}/4 010: OSC_{CLK}/8 011: OSC_{CLK}/16 100: OSC_{CLK}/64 101: OSC_{CLK}/128 110: External CLK 111: $TMR1_{OUT}$
<321:320>	TMR2 Trigger Event selection	00: On Both Falling and Rising Edges 01: On Falling Edge only 10: On Rising Edge only 11: No Delay on either Falling or Rising Edges for Delay Mode / High Level Reset for Counter Mode
<322>	SET/RST selection (for Counter mode)	0: Reset to 0 1: Set to Data
<323>	TMR2 Output polarity selection	0: Non-Inverted 1: Inverted
<324>	4-bit LUT0 or TMR2 selection	0: LUT 1: TMR
OSC		
<325>	Force Oscillator On	0: Auto Power On 1: Force Power On
<326>	Oscillator Frequency Control	0: 25 kHz 1: 2 MHz
<327>	Bit 8 CRV	1
<329:328>	OSC $CLK_{Prerscaler}$	00: 1 01: 1/2 10: 1/4 11: 1/8
<332:330>	OSC $OUT0_{Prescaler}$	000: OSC_{CLK} 001: OSC_{CLK}/2 010: OSC_{CLK}/4 011: OSC_{CLK}/8 100: OSC_{CLK}/16 101: OSC_{CLK}/32 110: OSC_{CLK}/64 111: OSC_{CLK}/128
<335:333>	OSC $OUT1_{Prescaler}$	000: OSC_{CLK}/1 001: OSC_{CLK}/2 010: OSC_{CLK}/4 011: OSC_{CLK}/8 100: OSC_{CLK}/16 101: OSC_{CLK}/32 110: OSC_{CLK}/64 111: OSC_{CLK}/128
<336>	External Clock Source selection	0: Internal Oscillator 1: EXTCLK from IO8
IOs		
<337>	IO3 Driver Strength selection	0: ×1 Driver Strength 1: ×2 Driver Strength
<338>	IO4 Driver Strength selection	0: ×1 Driver Strength 1: ×2 Driver Strength

Register Bit Address	Signal Function	Register Definition
<339>	IO6 Driver Strength selection	0: ×1 Driver Strength 1: ×2 Driver Strength
<340>	IO7 Driver Strength selection	0: ×1 Driver Strength 1: ×2 Driver Strength
<341>	IO8 Driver Strength selection	0: ×1 Driver Strength 1: ×2 Driver Strength
<342>	Bit 9 CRV	1
TIMERs		
<350:343>	TMR0 Control Data	1 – 255 Delay Time = (Control Data +1)/Freq
<352:351>	TMR0 Mode selection	00: Delay Mode 01: One Shot 10: Frequency Detector 11: Counter Mode
<355:353>	TMR0 Clock Source selection	000: OSC_{CLK} 001: OSC_{CLK}/4 010: OSC_{CLK}/8 011: OSC_{CLK}/16 100: OSC_{CLK}/64 101: OSC_{CLK}/128 110: External CLK 111: $TMR3_{OUT}$
<357:356>	TMR0 Trigger Event selection	00: On Both Falling and Rising Edges 01: On Falling Edge only 10: On Rising Edge only 11: No Delay on either Falling or Rising Edges for Delay Mode / High Level Reset for Counter Mode
<358>	TMR0 Edge Detect Output selection	0: Default Output 1: Edge Detect Output
<359>	TMR0 Output polarity selection	0: Non-Inverted 1: Inverted
<367:360>	TMR1 Control Data	1 – 255 Delay Time = (Control Data +1)/Freq
<368>	Bit 10 CRV	0
IOs Force Input Enable		
<369>	IO3 Force Input Enable	0: Disable 1: Enable (Input is always ON)
<370>	IO4 Force Input Enable	0: Disable 1: Enable (Input is always ON)
<371>	IO6 Force Input Enable	0: Disable 1: Enable (Input is always ON)
<372>	IO7 Force Input Enable	0: Disable 1: Enable (Input is always ON)
<373>	IO8 Force Input Enable	0: Disable 1: Enable (Input is always ON)
<374>	Reserved	
<375>	Reserved	
<376>	Bit 11 CRV	0
<377>	Bit 12 CRV	1
TIMERs		
<379:378>	TMR1 mode selection	00: Delay Mode 01: One Shot 10: Frequency Detector 11: Counter Mode
<382:380>	TMR1 Clock Source selection	000: OSC_{CLK} 001: OSC_{CLK}/4 010: OSC_{CLK}/8 011: OSC_{CLK}/32 100: OSC_{CLK}/16 101: OSC_{CLK}/128 110: External CLK 111: $TMR0_{OUT}$

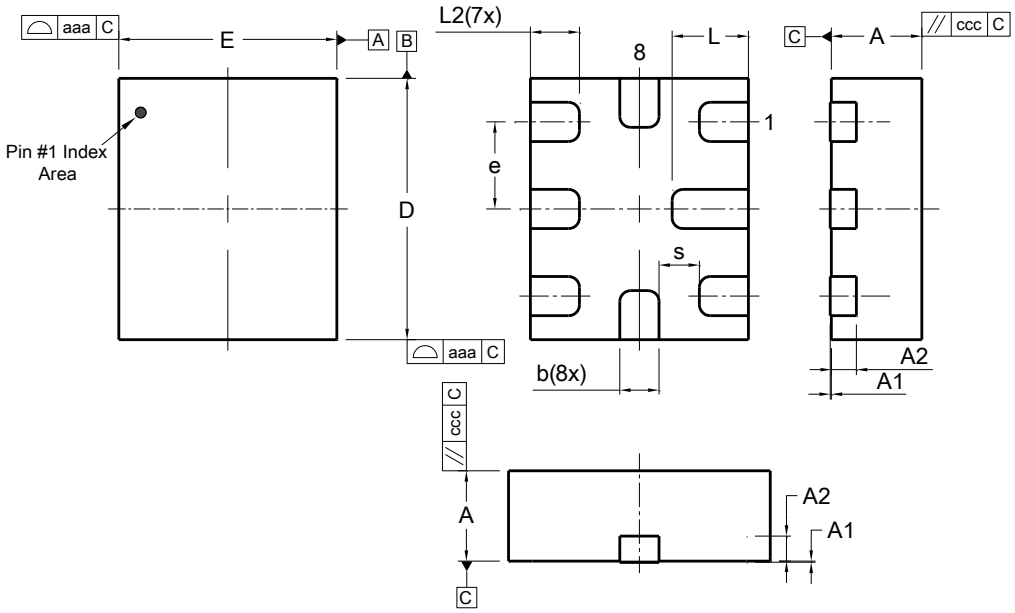
Register Bit Address	Signal Function	Register Definition
<384:383>	TMR1 Trigger Event selection	00: On Both Falling and Rising Edges 01: On Falling Edge only 10: On Rising Edge only 11: No Delay on either Falling or Rising Edges for Delay Mode / High Level Reset for Counter Mode
<385>	TMR1 Edge Detect Output selection	0: Default Output 1: Edge Detect Output
<386>	TMR1 Output polarity selection	0: Non-Inverted 1: Inverted
<387>	Reserved	
<395:388>	TMR3 Control Data	1 – 255 Delay Time = (Control Data +1)/Freq)
<397:396>	TMR3 mode selection	00: Delay Mode 01: One Shot 10: Frequency Detector 11: Counter Mode
<400:398>	TMR3 Clock Source selection	000: OSC_{CLK} 001: OSC_{CLK}/4 010: OSC_{CLK}/8 011: OSC_{CLK}/16 100: OSC_{CLK}/64 101: OSC_{CLK}/128 110: External CLK 111: $TMR2_{OUT}$
<402:401>	TMR3 Edge selection	00: Delay on Both Falling and Rising Edges for Delay Mode 01: Delay on Falling Edge only for Delay Mode 10: Delay on Rising Edge only for Delay Mode 11: No Delay on either Falling or Rising Edges for Delay Mode
<403>	TMR3 Output polarity selection	0: Non-Inverted 1: Inverted
IOs Output Enable		
<404>	IO3 Output Enable	0: Input Mode 1: Output Mode
<405>	IO6 Output Enable	0: Input Mode 1: Output Mode
<406>	IO7 Output Enable	0: Input Mode 1: Output Mode
IO2		
<408:407>	IO2 Input Mode Control	00: Digital Input w/o Schmitt Trigger 01: Digital Input w/ Schmitt Trigger 10: Digital Input Low Voltage 11: Reserved
<410:409>	IO2 Pull Down Resistor Value Selection	00: Floating 01: 10 kΩ 10: 100 kΩ 11: 1 MΩ
<411>	Bit 13 CRV	1
IO3		
<413:412>	IO3 Input Mode Control	00: Digital Input without Schmitt trigger 01: Digital Input with Schmitt trigger 10: Digital Input Low Voltage 11: Reserved
<415:414>	IO3 Output Mode Control	00: Push Pull 01: Open Drain NMOS 10: Open Drain PMOS 11: Reserved
<417:416>	IO3 Pull Up/Down Resistor Value selection	00: Floating 01: 10 kΩ 10: 100 kΩ 11: 1 MΩ
<418>	IO3 Pull Up/Down Resistor Enable	0: Pull Down Resistor Enable 1: Pull Up Resistor Enable

Register Bit Address	Signal Function	Register Definition
IO4		
<420:419>	IO4 Input Mode Control (DIR is LOW)	00: Digital Input w/o Schmitt Trigger 01: Digital Input w/ Schmitt Trigger 10: Digital Input Low Voltage 11: Reserved
<422:421>	IO4 Output Mode Control (DIR is HIGH)	00: Push Pull 01: Open Drain NMOS 10: Open Drain PMOS 11: Reserved
<424:423>	IO4 Pull Up/Down Resistor Value selection	00: Floating 01: 10 kΩ 10: 100 kΩ 11: 1 MΩ
<425>	IO4 Pull Up/Down Resistor Enable	0: Pull Down Resistor Enable 1: Pull Up Resistor Enable
IO6		
<427:426>	IO6 Input Mode Control	00: Digital Input without Schmitt trigger 01: Digital Input with Schmitt trigger 10: Digital Input Low Voltage 11: Reserved
<429:428>	IO6 Output Mode Control	00: Push Pull 01: Open Drain NMOS 10: Open Drain PMOS 11: Reserved
<431:430>	IO6 Pull Up/Down Resistor Value selection	00: Floating 01: 10 kΩ 10: 100 kΩ 11: 1 MΩ
<432>	IO6 Pull Up/Down Resistor Enable	0: Pull Down Resistor Enable 1: Pull Up Resistor Enable
IO7		
<434:433>	IO7 Input Mode Control	00: Digital Input without Schmitt trigger 01: Digital Input with Schmitt trigger 10: Digital Input Low Voltage 11: Reserved
<436:435>	IO7 Output Mode Control	00: Push Pull 01: Open Drain NMOS 10: Open Drain PMOS 11: Reserved
<438:437>	IO7 Pull Up/Down Resistor Value selection	00: Floating 01: 10 kΩ 10: 100 kΩ 11: 1 MΩ
<439>	IO7 Pull Up/Down Resistor Enable	0: Pull Down Resistor Enable 1: Pull Up Resistor Enable
IO8		
<441:440>	IO8 Input Mode Control	00: Digital Input w/o Schmitt Trigger 01: Digital Input w/ Schmitt Trigger 10: Digital Input Low Voltage 11: Reserved
<443:442>	IO8 Output Mode Control	00: Push Pull 01: Open Drain NMOS 10: Open Drain PMOS 11: Reserved
<445:444>	IO8 Pull Up/Down Resistor Value selection	00: Floating 01: 10 kΩ 10: 100 kΩ 11: 1 MΩ
<446>	IO8 Pull Up/Down Resistor Enable	0: Pull Down Resistor Enable 1: Pull Up Resistor Enable
Pattern ID		
<454:447>	8-bit Pattern ID	
Protection		
<455>	Reserved	

Register Bit Address	Signal Function	Register Definition
<456>	Continuous Registers Verification	0: Disable 1: Enable
<457>	CRC-8 Enable	0: Disable 1: Enable
Programmable Delay and Edge Detector		
<458>	Programmable Delay OUT polarity selection	0: Non-Inverted 1: Inverted
<460:459>	Edge Mode of PDLY & Edge Detector selection	00: Rising Edge Detector 01: Falling Edge Detector 10: Both Edge Detector 11: Both Edge Delay
<462:461>	Delay value selection for programmable delay & edge detector (V_{DD} = 3.3 V, typical condition)	00: 140 ns 01: 280 ns 10: 420 ns 11: 560 ns
<470:463>	Reserved	
<476:471>	Reserved	
<477>	Reserved	
<478>	Reserved	
<480:479>	Reserved	
<488:481>	Reserved	
<496:489>	Reserved	
RESET		
<498:497>	IO2 Reset Trigger Event selection	00: Rising Edge 01: Falling Edge 10: High Level 11: Reserved
<499>	IO2 Reset Enable	0: Disable 1: Enable
<500>	Reserved	
<501>	Bit 14 CRV	0
<509:502>	Reserved	
<510>	Reserved	
<511>	Reserved	

16. Package Drawing and Dimensions

X1-QFN1012-8 (Type AX)



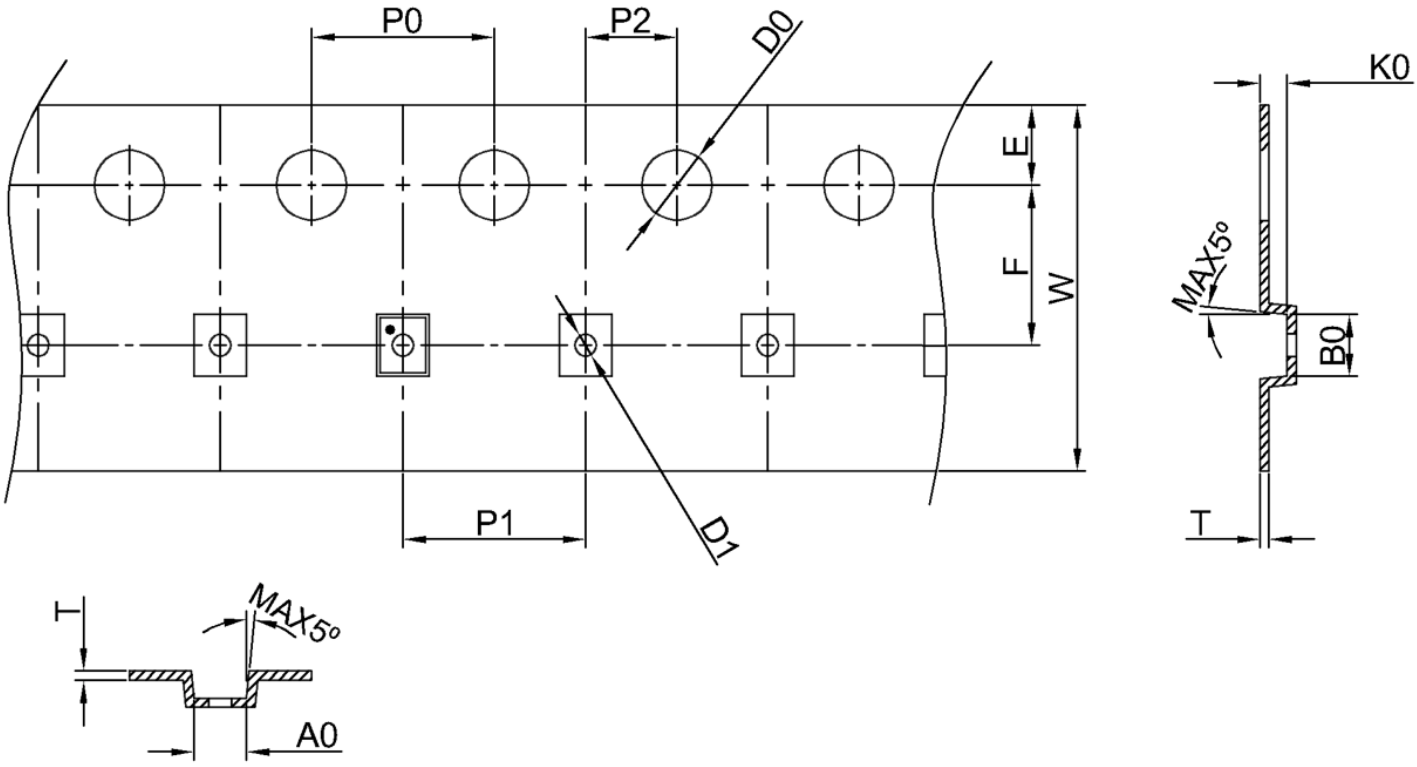
X1-QFN1012-8 (Type AX)			
Dim	**Min**	**Max**	**Typ**
A	0.37	0.47	0.42
A1	-0.005	0.03	--
A2	0.10	0.14	0.12
b	--	--	0.18
D	1.15	1.25	1.20
E	0.95	1.05	1.00
e	0.40 BSC		
s	0.185 REF		
L	--	--	0.350
L2	--	--	0.225
aaa	0.05		
ccc	0.05		
All Dimensions in mm			

17. Tape and Reel Specifications

Package Type	# of Pins	Nominal Package Size, mm	Max Units		per Reel & Hub Size, mm	Leader (min)		Trailer (min)		Tape Width, mm	Part Pitch, mm
			per Reel	per Box		Pockets	Length, mm	Pockets	Length, mm		
X1-QFN1012-8 (Type AX)	8	1.0× 1.2× 0.42	3000	3000	178/60	100	400	100	400	8	4

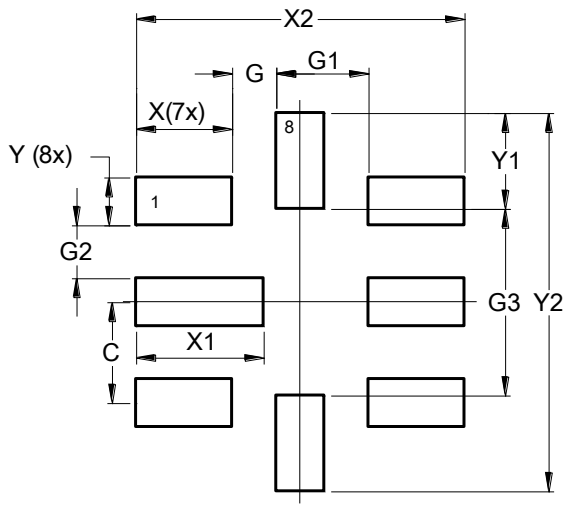
17.1. Carrier Tape Drawing and Dimensions

Package Type	A0	B0	K0	P0	P1	P2	T	E	F	D0	D1	W
X1-QFN1012-8 (Type AX)	1.15	1.35	0.60	4.00	4.00	2.00	0.20	1.75	3.50	1.55	0.50	8.00



18. Recommended Land Pattern

X1-QFN1012-8 (Type AX)



Dimensions	Value (in mm)
C	0.400
G	0.175
G1	0.365
G2	0.210
G3	0.740
X	0.380
X1	0.505
X2	1.300
Y	0.190
Y1	0.380
Y2	1.500

19. Mechanical Data

- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals: Finish – NiPdAu. Solderable per MIL-STD-202, Method 208 e4
- Weight: 0.0012 grams (Approximate)

20. Recommended Reflow Soldering Profile

Please see IPC/JEDEC J-STD-020: latest revision for reflow profile based on package volume of 0.66 mm^3 (nominal). More information can be found at www.jedec.org.

21. Revision History

Date	Version	Change
August 11, 2024	1	Initial release

22. Legal Statement

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