60V N-CHANNEL ENHANCEMENT MODE MOSFET

Product Summary

BV_{DSS}	$R_{DS(ON)}$ MAX	I_D T_A = +25°C
60V	85mΩ @ V_{GS} = 4.5V	3.68A
	90mΩ @ V_{GS} = 3.3V	3.58A
	95mΩ @ V_{GS} = 2.5V	3.48A
	250mΩ @ V_{GS} = 1.5V	2.21A

Features and Benefits

- Low On-Resistance
- Small 1.48mm x 0.98mm Package
- Ultra-Thin 0.3mm Package
- Low Input Capacitance
- Fast Switching Speed
- ESD Protected
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**
- **For automotive applications requiring specific change control (i.e. parts qualified to AEC-Q100/101/104/200, PPAP capable, and manufactured in IATF 16949 certified facilities), please contact us or your local Diodes representative. https://www.diodes.com/quality/product-definitions/**

Mechanical Data

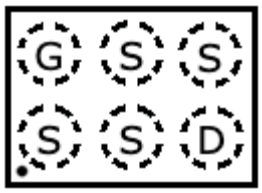
- Package: X2-TSN1510-6
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminal Connections: See Diagram Below
- Terminals: Finish —NiAu Solderable per MIL-STD202, Method 208 e4
- UBM Size: Gate Pad: 230µm
- Weight: 0.995mg (Approximate)

Description and Applications

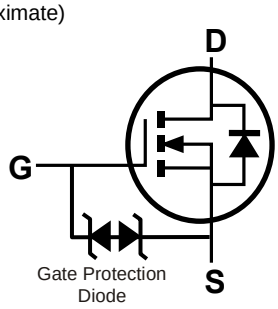
This new generation MOSFET is designed to minimize the footprint in handheld and mobile application. It can be used to replace many small-signals MOSFET with really small footprint.

- Load switches
- DC-DC primary switches

X2-TSN1510-6 (Note 4)



Top View



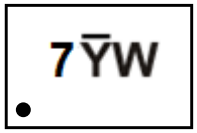
Equivalent Circuit

Ordering Information (Note 5)

Part Number	Package	Packing	
		Qty.	Carrier
DMN6070LCA6-7	X2-TSN1510-6	3,000	Tape & Reel

Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
4. Device with exposed silicon sidewall is non-isolated area.
5. For packaging details, go to our website at https://www.diodes.com/design/support/packaging/diodes-packaging/.

Marking Information



7 = Product Type Marking Code
YW = Date Code Marking
Y = Year (ex: 4 = 2024)
W = Week (ex: a = Week 27; z Represents Week 52 and 53)

Date Code Key

Year	2024	2025	2026	2027	2028	2029	2030	2031	2032	2033	2034	2035
Code	4	5	6	7	8	9	0	1	2	3	4	5

Week	1-26	27-52	53
Code	A-Z	a-z	z

Maximum Ratings (@T_A = +25°C, unless otherwise specified.)

Characteristic		Symbol	Value	Unit
Drain-Source Voltage		V_{DSS}	60	V
Gate-Source Voltage		V_{GSS}	±8	V
Continuous Drain Current (Note 7) V_{GS} = 4.5V	T_A = +25°C T_A = +70°C	I_D	3.68 2.95	A
Continuous Drain Current (Note 7) V_{GS} = 3.3V	T_A = +25°C T_A = +70°C	I_D	3.58 2.86	A
Continuous Drain Current (Note 7) V_{GS} = 2.5V	T_A = +25°C T_A = +70°C	I_D	3.48 2.79	A
Pulsed Drain Current (Note 7)		I_{DM}	23	A
Maximum Body Diode Continuous Current (Note 7)		I_S	3.68	A
Pulsed Body Diode Continuous Current (10µs Pulse, Duty Cycle = 1%)		I_{SM}	23	A

Thermal Characteristics (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Value	Unit
Power Dissipation (Note 6)	P_D	0.6	W
Thermal Resistance, Junction to Ambient (Note 6)	$R_{\theta JA}$	205	°C/W
Power Dissipation (Note 7)	P_D	1.8	W
Thermal Resistance, Junction to Ambient (Note 7)	$R_{\theta JA}$	70	°C/W
Operating and Storage Temperature Range	T_J, T_{STG}	-55 to +150	°C

Notes: 6. Device mounted on FR-4 PCB, with minimum recommended pad layout.
7. Device mounted on FR-4 material with 1inch^2 (6.45cm^2), 2oz. (0.071mm thick) Cu.

Electrical Characteristics (@T_A = +25°C, unless otherwise specified.)

Characteristic		Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 8)							
Drain-Source Breakdown Voltage		BV_{DSS}	60	—	—	V	V_{GS} = 0V, I_D = 250μA
Zero Gate Voltage Drain Current		I_{DSS}	—	—	1.0	μA	V_{DS} = 60V, V_{GS} = 0V
Gate-Body Leakage		I_{GSS}	—	—	±10	μA	V_{GS} = ±8V, V_{DS} = 0V
ON CHARACTERISTICS (Note 8)							
Gate Threshold Voltage		$V_{GS(TH)}$	0.4	—	1.0	V	V_{DS} = V_{GS}, I_D = 250μA
Static Drain-Source On-Resistance	@ T_J = +25°C @ T_J = +150°C (Note 10)	$R_{DS(ON)}$	—	55 85	85 150	mΩ	V_{GS} = 4.5V, I_D = 3A
	@ T_J = +25°C			56	90		V_{GS} = 3.3V, I_D = 3A
	@ T_J = +25°C			58	95		V_{GS} = 2.5V, I_D = 3A
	@ T_J = +25°C			70	250		V_{GS} = 1.5V, I_D = 3A
Body Diode Forward Voltage		V_{SD}	—	0.6	1.2	V	V_{GS} = 0V, I_S = 1A
DYNAMIC CHARACTERISTICS (Note 9)							
Input Capacitance		C_{iss}	—	1613	—	pF	V_{DS} = 30V, V_{GS} = 0V, f = 1.0MHz
Output Capacitance		C_{oss}	—	51	—	pF	
Reverse Transfer Capacitance		C_{rss}	—	39	—	pF	
Series Gate Resistance		R_g	—	11.5	—	Ω	V_{DS} = 0V, V_{GS} = 0V, f = 1.0MHz
Total Gate Charge		Q_g	—	18.7	—	nC	V_{DS} = 30V, V_{GS} = 4.5V, I_D = 3A
Gate-Source Charge		Q_{gs}	—	1.7	—	nC	
Gate-Drain Charge		Q_{gd}	—	1.4	—	nC	
Turn-On Delay Time		$t_{D(ON)}$	—	8.7	—	ns	V_{DS} = 30V, I_D = 3A, V_{GEN} = 4.5V, R_G = 6.0Ω
Turn-On Rise Time		t_R	—	42	—	ns	
Turn-Off Delay Time		$t_{D(OFF)}$	—	158	—	ns	
Turn-Off Fall Time		t_F	—	95	—	ns	
Reverse Recovery Charge		Q_{RR}	—	11.1	—	nC	I_F = 3A, di/dt = 300A/μs
Reverse Recovery Time		t_{RR}	—	11.5	—	ns	I_F = 3A, di/dt = 300A/μs

Notes: 8. Short duration pulse test used to minimize self-heating effect.
9. Guaranteed by design. Not subject to production testing.

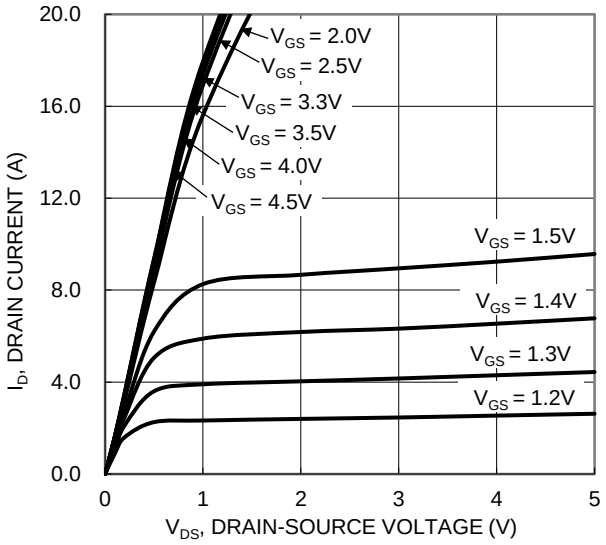


Figure 1. Typical Output Characteristic

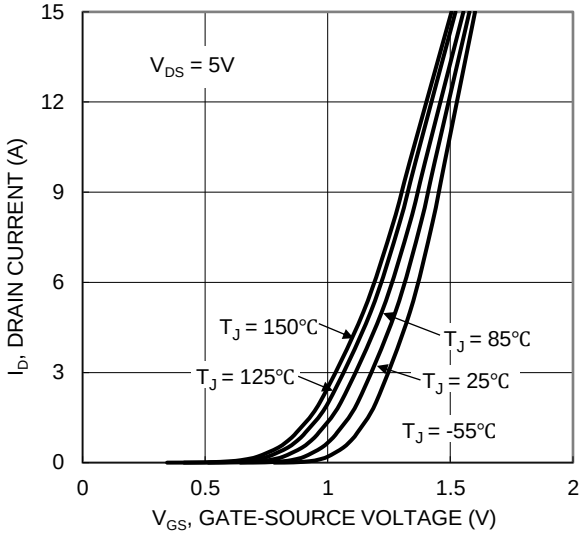


Figure 2. Typical Transfer Characteristic

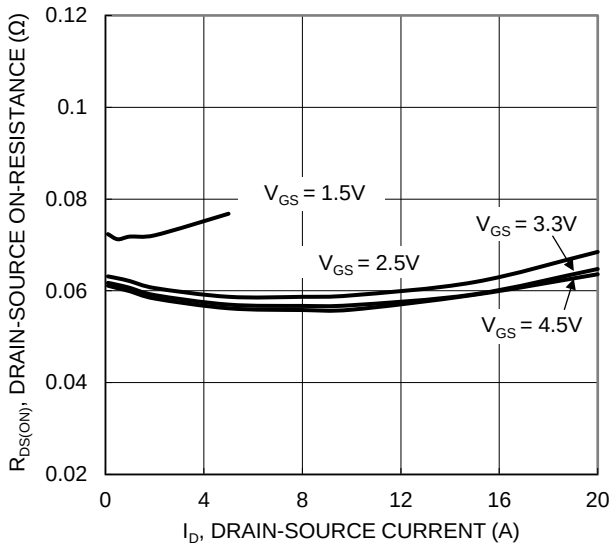


Figure 3. Typical On-Resistance vs. Drain Current and Gate Voltage

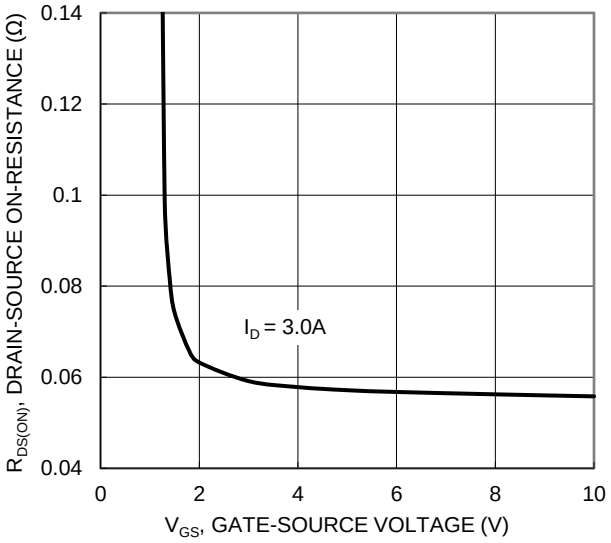


Figure 4. Typical Transfer Characteristic

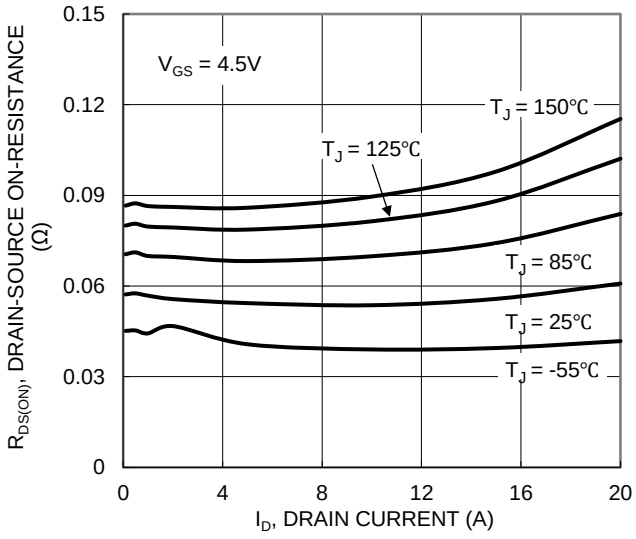


Figure 5. Typical On-Resistance vs. Drain Current and Temperature

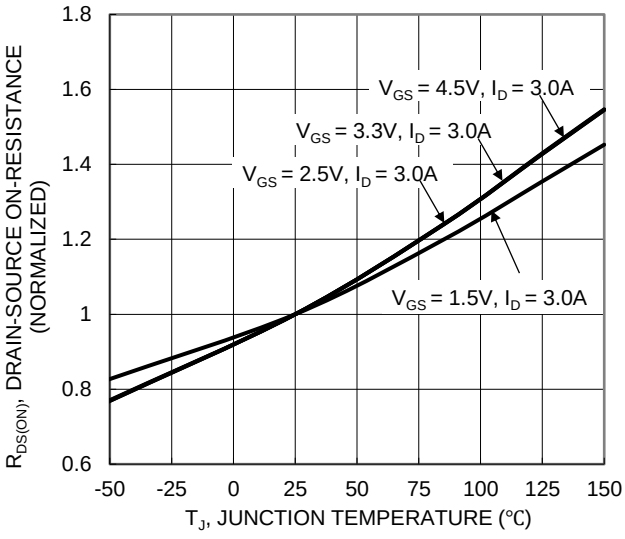


Figure 6. On-Resistance Variation with Temperature

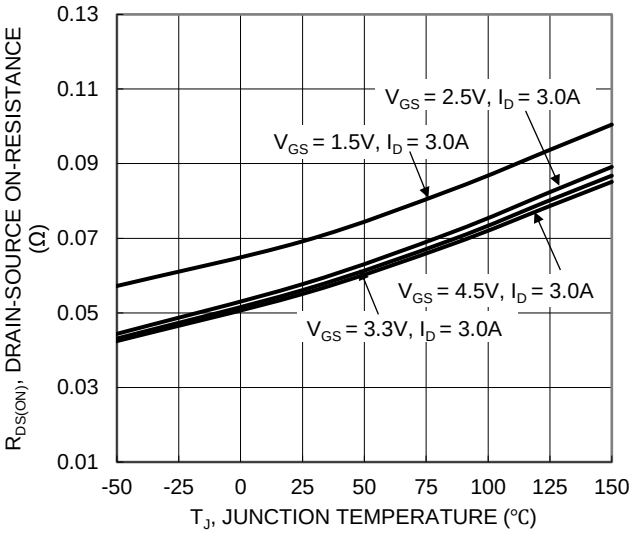


Figure 7. On-Resistance Variation with Temperature

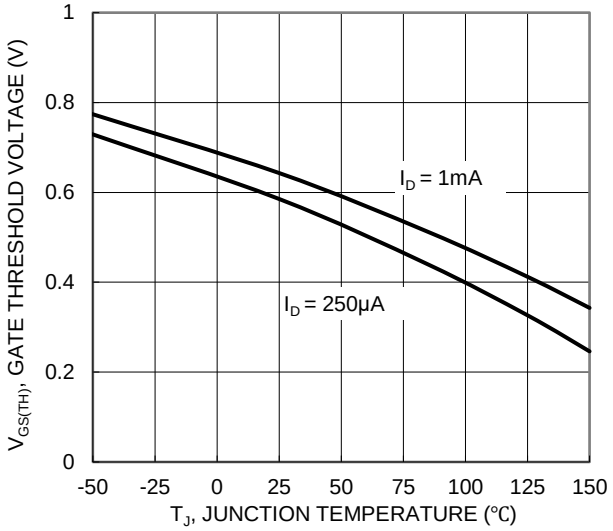


Figure 8. Gate Threshold Variation vs. Junction Temperature

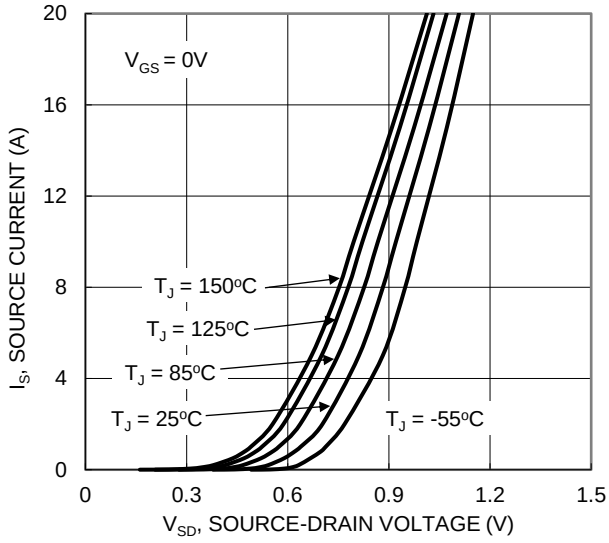


Figure 9. Diode Forward Voltage vs. Current

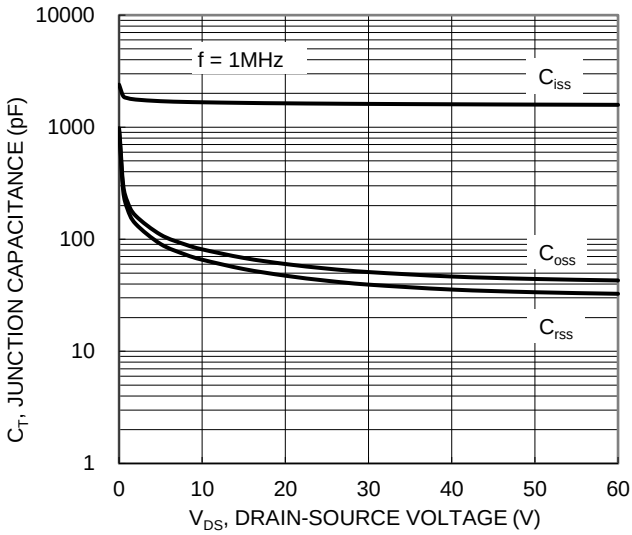


Figure 10. Typical Junction Capacitance

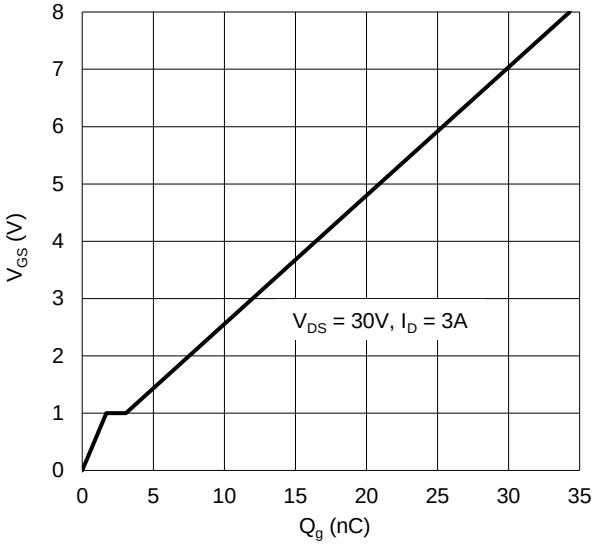


Figure 11. Gate Charge

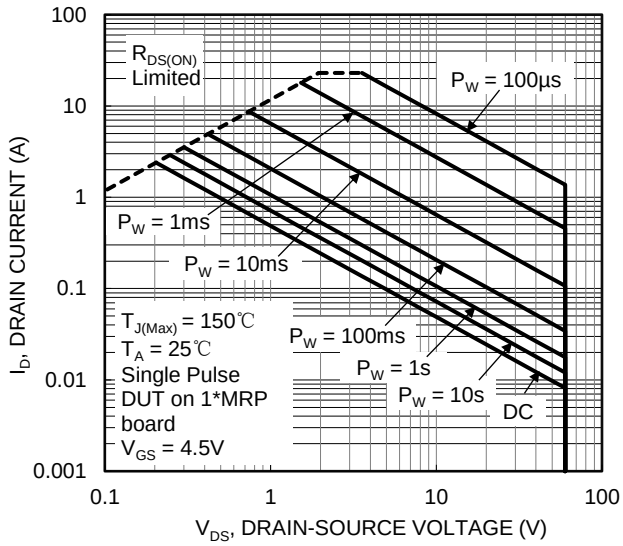


Figure 12. SOA, Safe Operation Area

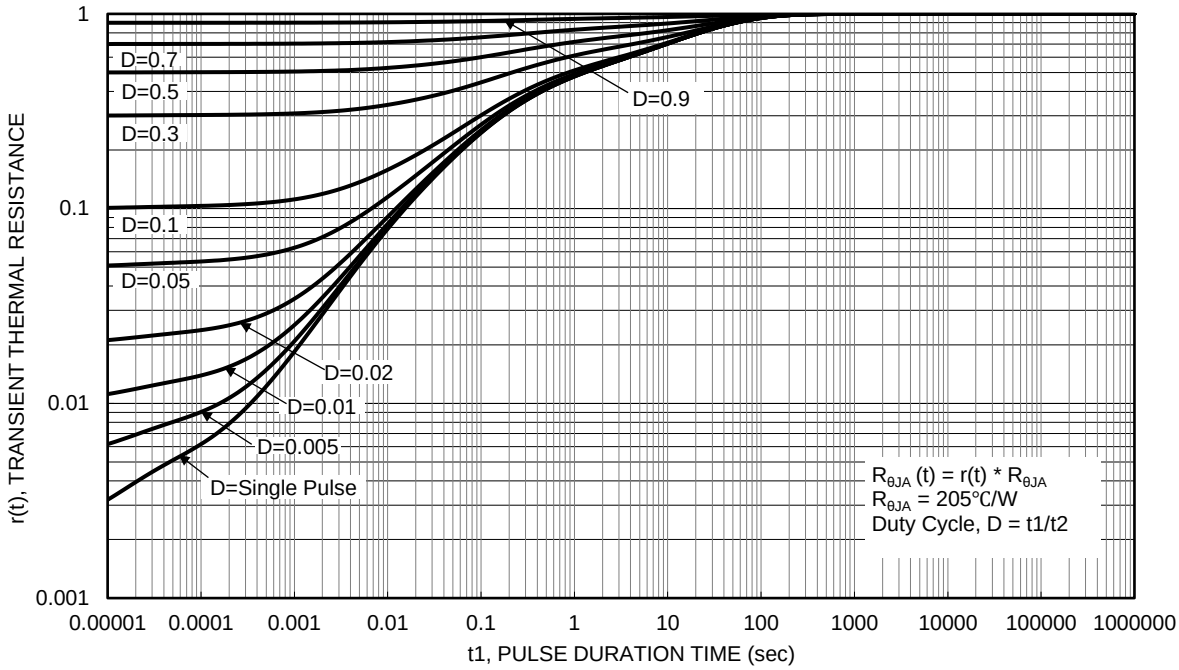
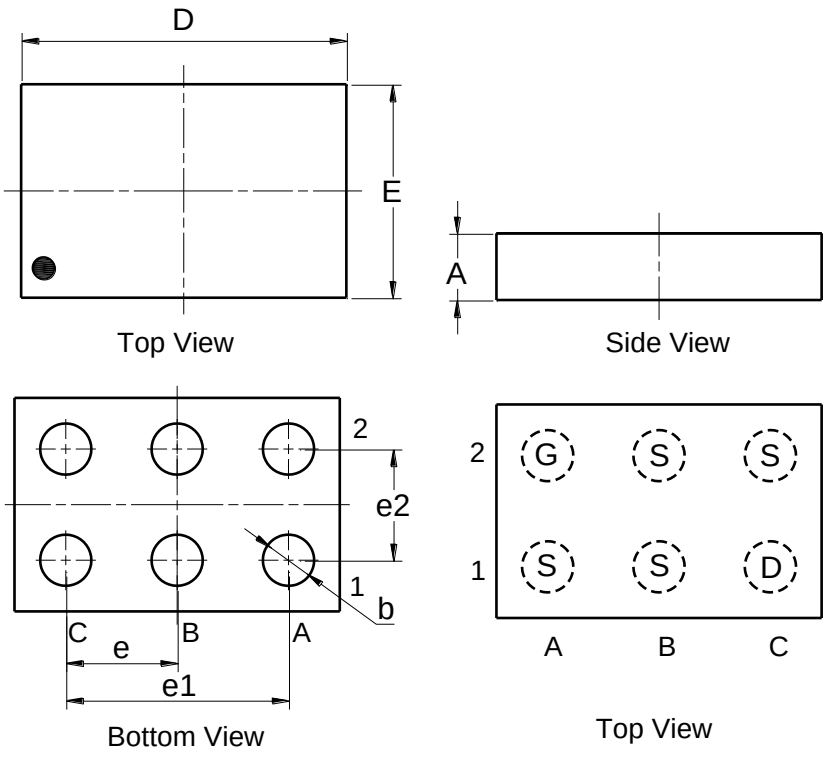


Figure 13. Transient Thermal Resistance

Package Outline Dimensions

Please see http://www.diodes.com/package-outlines.html for the latest version.

X2-TSN1510-6



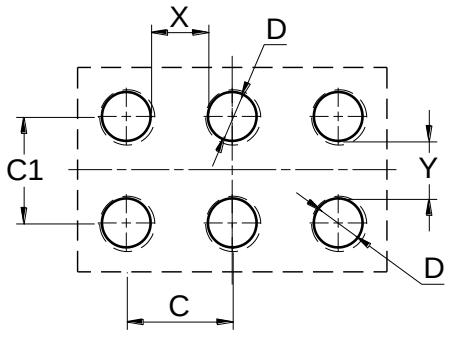
X2-TSN1510-6			
Dim	**Min**	**Max**	**Typ**
A	0.27	0.33	0.30
b	0.20	0.26	0.23
D	1.45	1.51	1.48
E	0.95	1.01	0.98
e	--	--	0.50
e1	--	--	1.00
e2	--	--	0.50
All Dimensions in mm			

Pin Assignment	
A1	S
A2	G
B1	S
B2	S
C1	D
C2	S

Suggested Pad Layout

Please see http://www.diodes.com/package-outlines.html for the latest version.

X2-TSN1510-6



Dimensions	Value (in mm)
C	0.50
C1	0.50
D	0.23
X	0.27
Y	0.27

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