



P-CHANNEL ENHANCEMENT MODE MOSFET PowerDI5060-8

Product Summary

BV _{DSS}	Rds(on) max	ID MAX $T_C = +25^{\circ}C$	
40)/	10mΩ @ V _{GS} = -10V	-76A	
-40V	14mΩ @ V _{GS} = -4.5V	-58A	

Description and Applications

This new generation MOSFET is designed to minimize the on-state resistance (R_{DS(ON)}) yet maintain superior switching performance, making it ideal for high-efficiency power-management applications.

- DC-DC converters
- Power-management functions
- Analog switches

Features and Benefits

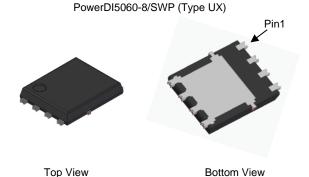
- 100% Unclamped Inductive Switch (UIS) Test in Production
- Low On-Resistance
- Fast Switching Speed
- Lead-Free Finish; RoHS Compliant (Notes 1 & 2)
- Halogen and Antimony Free. "Green" Device (Note 3)
- This part is qualified to JEDEC standards (as references in AEC-Q) for High Reliability.

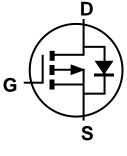
https://www.diodes.com/quality/product-definitions/

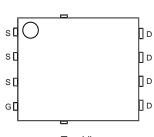
 An automotive-compliant part is available under separate datasheet (<u>DMP4011SPSWQ</u>)

Mechanical Data

- Package: PowerDI[®]5060-8
- Package Material: Molded Plastic, "Green" Molding Compound.
 UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminal Connections: See Diagram
- Terminals: Finish—100% Matte Tin Annealed over Copper Leadframe. Solderable per MIL-STD-202, Method 208 (3)
- Weight: 0.097 grams (Approximate)







Internal Schematic

Top View Pin Configuration

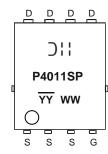
Ordering Information (Note 4)

Port Number	Packago	Packing		
Part Number	Раскаде	Qty.	Carrier	
DMP4011SPSW-13	PowerDI5060-8/SWP (Type UX)	2,500	Tape & Reel	

Notes:

- 1. EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant. All applicable RoHS exemptions applied.
- 2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
- 3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
- 4. For packaging details, go to our website at https://www.diodes.com/design/support/packaging/diodes-packaging/.

Marking Information



);; = Manufacturer's Marking
P4011SP = Product Type Marking Code
YYWW = Date Code Marking
YY = Year (ex: 24 = 2024)
WW = Week (01 to 53)



Maximum Ratings (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Value	Unit		
Drain-Source Voltage	VDSS	-40	V		
Gate-Source Voltage	V_{GSS}	±20	V		
Continuous Proin Current (Note 7) Vos - 10V	Steady	Tc = +25°C	-	-76	- A
Continuous Drain Current (Note 7) V _{GS} = -10V	State	T _C = +70°C	l _D	-61	
Continuous Drain Current (Note C) Vac. 10V	Steady State	T _A = +25°C	_	-11.7	
Continuous Drain Current (Note 6) Vgs = -10V		T _A = +70°C	lσ	-9.4	Α
Pulsed Drain Current (10µs Pulse, Duty Cycle = 1%		I _{DM}	-300	Α	
Maximum Body Diode Continuous Current (Note 6)	Is	-8.9	Α		
Pulsed Source Current (10µs Pulse, Duty Cycle = 1	Ism	-300	Α		
Avalanche Current (Note 8) L = 1mH	las	-22	Α		
Avalanche Energy (Note 8) L = 1mH	Eas	250	mJ		

Thermal Characteristics ($@T_A = +25^{\circ}C$, unless otherwise specified.)

Characteristic		Symbol	Value	Unit
Total Power Dissipation (Note 5)	T _A = +25°C	PD	1.3	W
Thermal Resistance, Junction to Ambient (Note 5)	Steady State	Reja	96.4	°C/W
Total Power Dissipation (Note 6)	T _A = +25°C	Pp	2.3	W
Thermal Resistance, Junction to Ambient (Note 6)	Steady State	R _{0JA}	55	°C/W
Thermal Resistance, Junction to Case (Note 7)		Rejc	1.3	°C/W
Operating and Storage Temperature Range		TJ, TSTG	-55 to +150	°C

Electrical Characteristics (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Min	Тур	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 9)						
Drain-Source Breakdown Voltage	BV _{DSS}	-40	_	_	V	$V_{GS} = 0V, I_{D} = -250\mu A$
Zero Gate Voltage Drain Current	IDSS	_	_	-1	μΑ	V _{DS} = -32V, V _{GS} = 0V
Gate-Source Leakage	Igss	_	_	±100	nA	$V_{GS} = \pm 20V$, $V_{DS} = 0V$
ON CHARACTERISTICS (Note 9)						
Gate Threshold Voltage	V _{GS(TH)}	-1.0	-2.0	-2.5	V	$V_{DS} = V_{GS}$, $I_D = -250\mu A$
Static Drain-Source On-Resistance	Dagger		6	10	mΩ	$V_{GS} = -10V, I_D = -9.8A$
Static Drain-Source On-Resistance	Rds(on)	_	10	14	11177	$V_{GS} = -4.5V, I_{D} = -9.8A$
Diode Forward Voltage	VsD	_	-0.7	-1	V	$V_{GS} = 0V$, $I_{S} = -1A$
DYNAMIC CHARACTERISTICS (Note 10)						
Input Capacitance	Ciss	1	2747	_		V _{DS} = -20V, V _{GS} = 0V f = 1MHz
Output Capacitance	Coss	l	508	_	pF	
Reverse Transfer Capacitance	Crss		222	_		
Gate Resistance	R_g		21.4	_	Ω	$V_{DS} = 0V$, $V_{GS} = 0V$, $f = 1MHz$
Total Gate Charge (V _{GS} = -4.5V)	Qg	_	25	_		
Total Gate Charge (V _{GS} = -10V)	Qg	_	52	_	nC	V _{DS} = -20V
Gate-Source Charge	Qgs	_	8.5	_	IIC	I _D = -9.8A
Gate-Drain Charge	Q_{gd}	_	11.8	_		
Turn-On Delay Time	t _{D(ON)}	_	6.6	_		
Turn-On Rise Time	t _R	_	6.5	_		$V_{GS} = -10V, V_{DD} = -20V,$
Turn-Off Delay Time	tD(OFF)	_	222	_	ns	$R_q = 6\Omega$, $I_D = -1A$
Turn-Off Fall Time	tF	_	138	_		
Reverse-Recovery Time	t _{RR}	_	25	_	ns	IF = -9.8A, di/dt = -100A/µs
Reverse-Recovery Charge	Q _{RR}	_	17	_	nC	I _F = -9.8A, di/dt = -100A/µs

5. Device mounted on FR-4 substrate PC board, 2oz copper, with minimum recommended pad layout.
6. Device mounted on FR-4 substrate PC board, 2oz copper, with 1inch square copper plate.

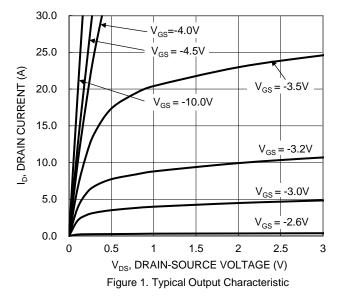
7. Thermal resistance from junction to soldering point (on the exposed drain pad).

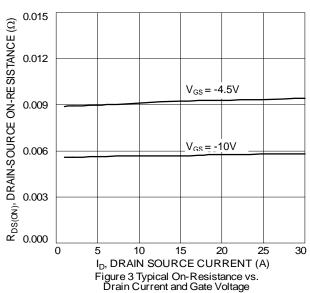
8. I_{AS} and E_{AS} ratings are based on low frequency and duty cycles to keep $T_J = +25^{\circ}C$.

9. Short duration pulse test used to minimize self-heating effect.

10. Guaranteed by design. Not subject to product testing.







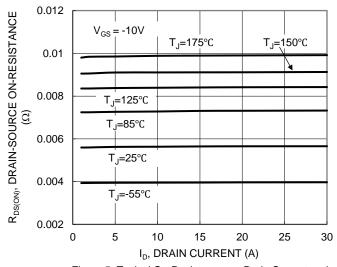


Figure 5. Typical On-Resistance vs. Drain Current and Temperature

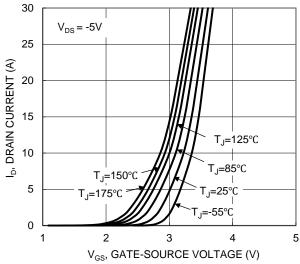


Figure 2. Typical Transfer Characteristic

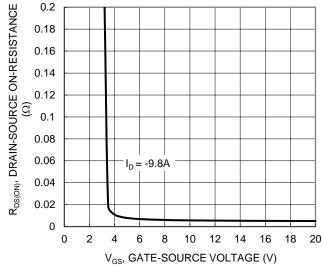


Figure 4. Typical Transfer Characteristic

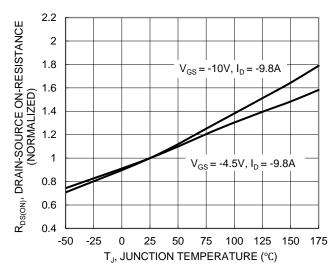
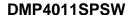


Figure 6. On-Resistance Variation with Temperature





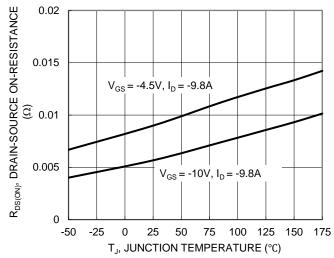


Figure 7. On-Resistance Variation with Temperature

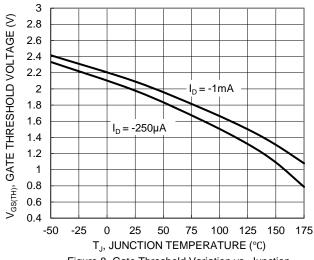


Figure 8. Gate Threshold Variation vs. Junction Temperature

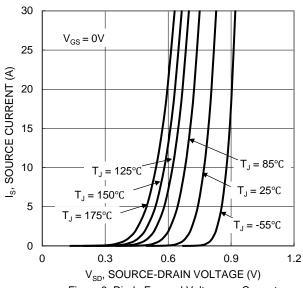
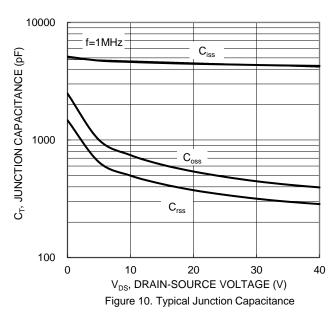


Figure 9. Diode Forward Voltage vs. Current



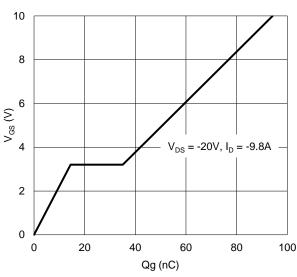


Figure 11. Gate Charge

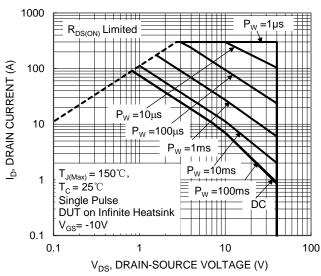


Figure 12. SOA, Safe Operation Area



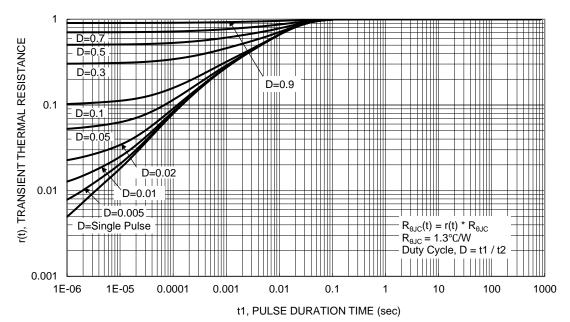


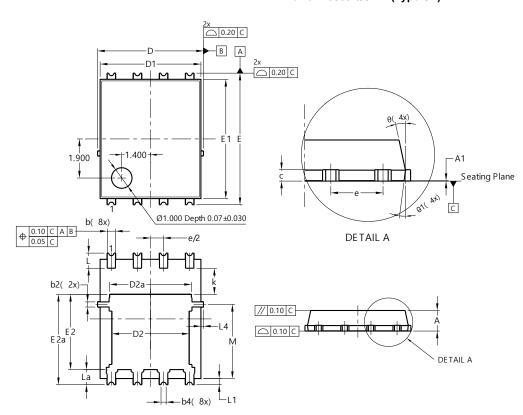
Figure 13. Transient Thermal Resistance



Package Outline Dimensions

Please see http://www.diodes.com/package-outlines.html for the latest version.

PowerDI5060-8/SWP (Type UX)

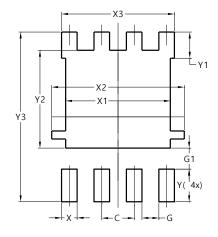


PowerDI5060-8/SWP (Type UX)						
Dim	Min	Max	Тур			
Α	0.90	1.10	1.00			
A1	0	0.05				
b	0.30	0.50	0.41			
b2	0.20	0.35	0.25			
b4	().25REF	-			
С	0.230	0.330	0.277			
D	5	.15 BS0	2			
D1	4.70	5.10	4.90			
D2	3.56	3.96	3.76			
D2a	3.78	4.18	3.98			
E	6	.40 BS0				
E1	5.60	5.60 6.00				
E2	3.46	3.86	3.66			
E2a	4.195	4.595	4.395			
е	1	.27BSC				
k	1.05					
١	0.635	0.835	0.735			
La	0.635	0.835	0.735			
L1	0.200	0.400	0.300			
L4	0.025	0.225	0.125			
M	3.205	4.005	3.605			
θ	10°	12°	11°			
θ1	6°	8°	7°			
All Dimensions in mm						

Suggested Pad Layout

Please see http://www.diodes.com/package-outlines.html for the latest version.

PowerDI5060-8/SWP (Type UX)



Dimensions	Value		
Dilliensions	(in mm)		
С	1.270		
G	0.660		
G1	0.820		
X	0.610		
X1	4.100		
X2	5.190		
Х3	4.420		
Y	1.270		
Y1	1.020		
Y2	3.810		
Y3	6.610		



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