

Product Summary

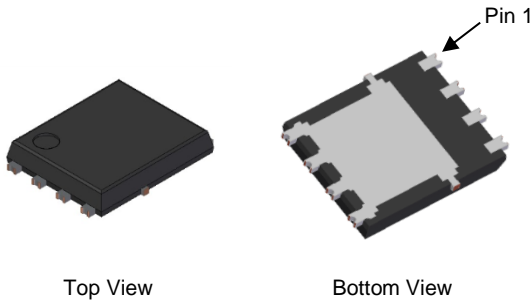
BV_{DSS}	$R_{DS(ON)}$ Max	I_D $T_c = +25^\circ C$
-40V	15m Ω @ $V_{GS} = -10V$	-61A
	23m Ω @ $V_{GS} = -4.5V$	-49A

Description and Applications

This new generation MOSFET has been designed to minimize the on-state resistance ($R_{DS(ON)}$) yet maintain superior switching performance, making it ideal for high-efficiency power-management applications.

- Reverse-polarity protections
- BLDC motor controls
- Power-management functions

PowerDI5060-8/SWP (Type UX)

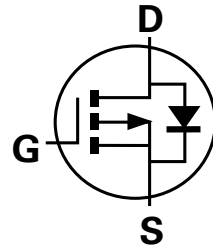


Features and Benefits

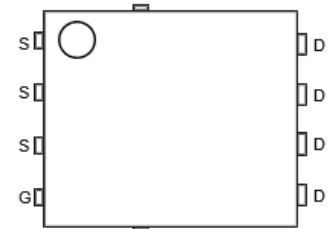
- 100% Unclamped Inductive Switch (UIS) Test in Production
- Low On-Resistance
- Fast Switching Speed
- **Lead-Free Finish; RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**
- **This part is qualified to JEDEC standards (as references in AEC-Q) for High Reliability.**
<https://www.diodes.com/quality/product-definitions/>
- **An automotive-compliant part is available under separate datasheet (DMP4013SPSWQ)**

Mechanical Data

- Package: PowerDI[®]5060-8
- Package Material: Molded Plastic, "Green" Molding Compound. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminal Connections: See Diagram
- Terminals: Finish – 100% Matte Tin Annealed over Copper Leadframe. Solderable per MIL-STD-202, Method 208 (E3)
- Weight: 0.097 grams (Approximate)



Internal Schematic



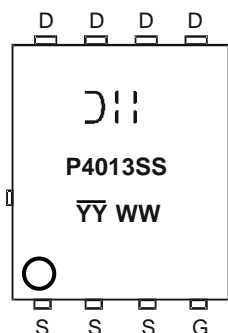
Top View
Pin Configuration

Ordering Information (Note 4)

Part Number	Package	Packing	
		Qty.	Carrier
DMP4013SPSW-13	PowerDI5060-8/SWP (Type UX)	2500	Tape & Reel

- Notes:
1. EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant. All applicable RoHS exemptions applied.
 2. See <https://www.diodes.com/quality/lead-free/> for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
 3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
 4. For packaging details, go to our website at <https://www.diodes.com/design/support/packaging/diodes-packaging/>.

Marking Information



- $\text{D}|||$ = Manufacturer's Marking
 P4013SS = Product Type Marking Code
 YYWW = Date Code Marking
 YY = Year (ex: 24 = 2024)
 WW = Week (01 to 53)

Maximum Ratings (@T_A = +25°C, unless otherwise specified.)

Characteristic			Symbol	Value	Unit
Drain-Source Voltage			V _{DSS}	-40	V
Gate-Source Voltage			V _{GSS}	±20	V
Continuous Drain Current V _{GS} = -10V (Note 7)	Steady State	T _C = +25°C T _C = +70°C	I _D	-61 -49	A
Continuous Drain Current V _{GS} = -10V (Note 6)	Steady State	T _A = +25°C T _A = +70°C	I _D	-11 -9	A
Pulsed Drain Current (10µs Pulse, Duty Cycle = 1%)			I _{DM}	-244	A
Maximum Body Diode Continuous Current (Note 7)			I _S	-61	A
Pulsed Source Current (10µs Pulse, Duty Cycle = 1%)			I _{SM}	-244	A
Avalanche Current (Note 8) L = 1mH			I _{AS}	-16	A
Avalanche Energy (Note 8) L = 1mH			E _{AS}	176	mJ

Thermal Characteristics (@T_A = +25°C, unless otherwise specified.)

Characteristic		Symbol	Value	Unit
Total Power Dissipation (Note 5)	T _A = +25°C	P _D	1.6	W
Thermal Resistance, Junction to Ambient (Note 5)	Steady State	R _{θJA}	96	°C/W
Total Power Dissipation (Note 6)	T _A = +25°C	P _D	3.4	W
Thermal Resistance, Junction to Ambient (Note 6)	Steady State	R _{θJA}	44	°C/W
Thermal Resistance, Junction to Case (Note 7)		R _{θJC}	1.5	°C/W
Operating and Storage Temperature Range		T _J , T _{STG}	-55 to +150	°C

- Notes:
5. Device mounted on FR-4 PC board, with minimum recommended pad layout, single sided.
 6. Device mounted on FR-4 substrate PC board, 2oz copper, with thermal bias to bottom layer 1 inch square copper plate.
 7. Thermal resistance from junction to soldering point (on the exposed drain pad).
 8. I_{AS} and E_{AS} ratings are based on low frequency and duty cycles to keep T_J = +25°C.

Electrical Characteristics (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 9)						
Drain-Source Breakdown Voltage	BV _{DSS}	-40	—	—	V	V _{GS} = 0, I _D = -250µA
Zero Gate Voltage Drain Current	I _{DSS}	—	—	-1	µA	V _{DS} = -40V, V _{GS} = 0
Gate-Source Leakage	I _{GSS}	—	—	±100	nA	V _{GS} = ±20V, V _{DS} = 0
ON CHARACTERISTICS (Note 9)						
Gate Threshold Voltage	V _{GS(TH)}	-1	—	-3	V	V _{DS} = V _{GS} , I _D = -250µA
Static Drain-Source On-Resistance	R _{DS(ON)}	—	9.6	15	mΩ	V _{GS} = -10V, I _D = -10A
		—	13.4	23		V _{GS} = -4.5V, I _D = -8A
Diode Forward Voltage	V _{SD}	—	-0.7	-1.2	V	V _{GS} = 0, I _S = -1A
DYNAMIC CHARACTERISTICS (Note 10)						
Input Capacitance	C _{iss}	—	4004	—	pF	V _{DS} = -20V, V _{GS} = 0, f = 1MHz
Output Capacitance	C _{oss}	—	309	—		
Reverse Transfer Capacitance	C _{rss}	—	229	—		
Gate Resistance	R _g	—	3.5	—	Ω	V _{DS} = 0, V _{GS} = 0, f = 1MHz
Total Gate Charge (V _{GS} = -4.5V)	Q _g	—	31	—	nC	V _{DS} = -20V, I _D = -10A
Total Gate Charge (V _{GS} = -10V)	Q _g	—	67	—		
Gate-Source Charge	Q _{gs}	—	13.2	—		
Gate-Drain Charge	Q _{gd}	—	11	—		
Turn-On Delay Time	t _{D(ON)}	—	9.9	—	ns	V _{GS} = -10V, V _{DD} = -20V, R _G = 3Ω, I _D = -10A
Turn-On Rise Time	t _R	—	32	—		
Turn-Off Delay Time	t _{D(OFF)}	—	46	—		
Turn-Off Fall Time	t _F	—	53	—		
Reverse-Recovery Time	t _{RR}	—	19.5	—	ns	I _F = -10A, di/dt = -100A/µs
Reverse-Recovery Charge	Q _{RR}	—	11.6	—	nC	I _F = -10A, di/dt = -100A/µs

- Notes:
9. Short duration pulse test used to minimize self-heating effect.
 10. Guaranteed by design. Not subject to product testing.

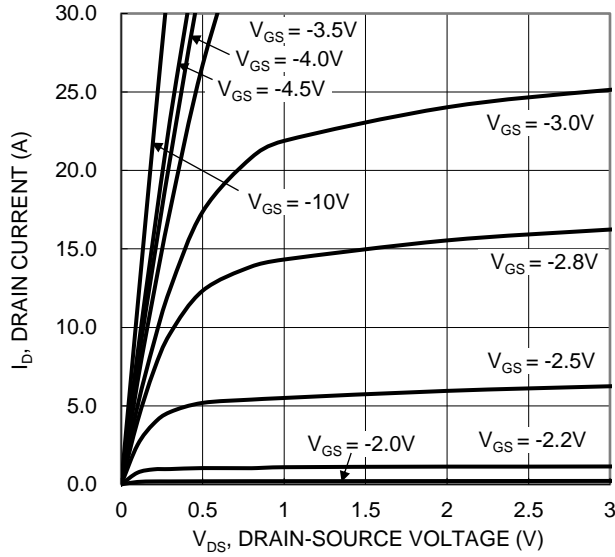


Figure 1. Typical Output Characteristic

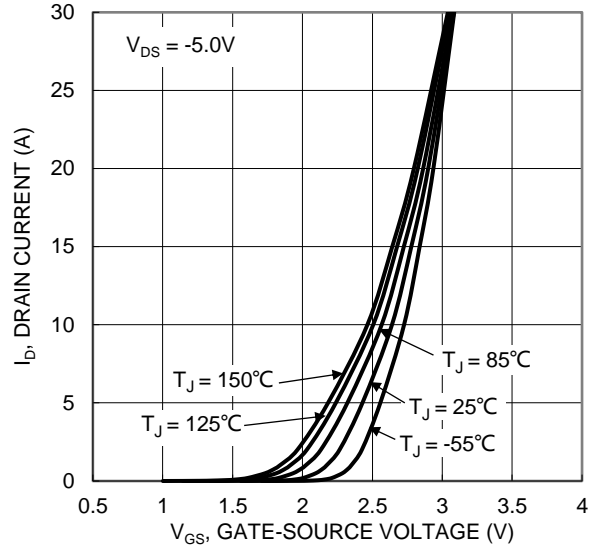


Figure 2. Typical Transfer Characteristic

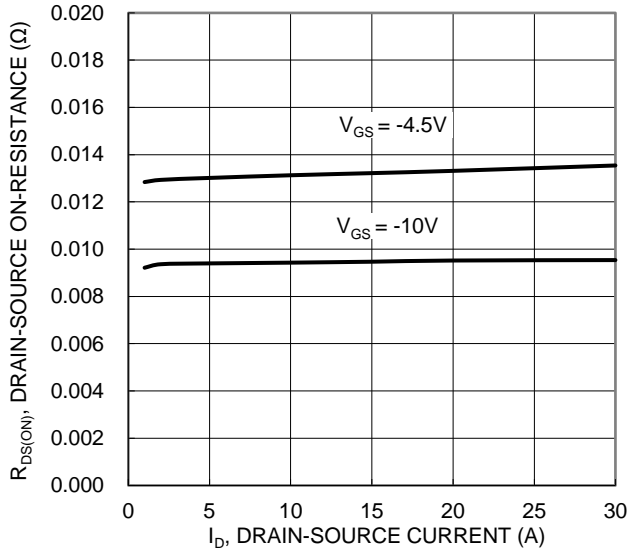


Figure 3. Typical On-Resistance vs. Drain Current and Gate Voltage

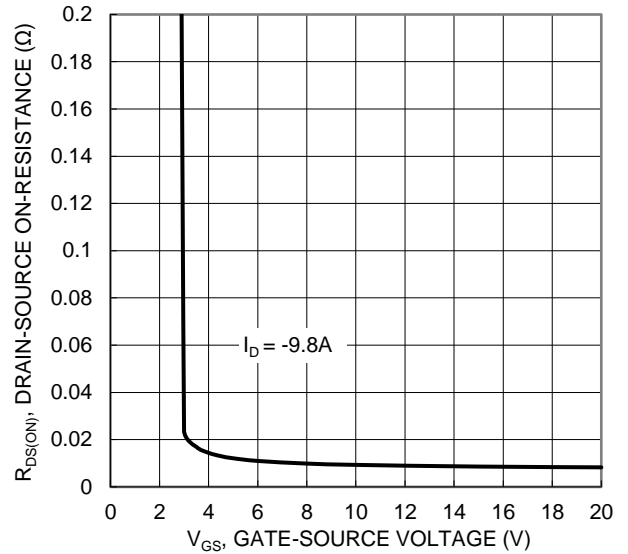


Figure 4. Typical Transfer Characteristic

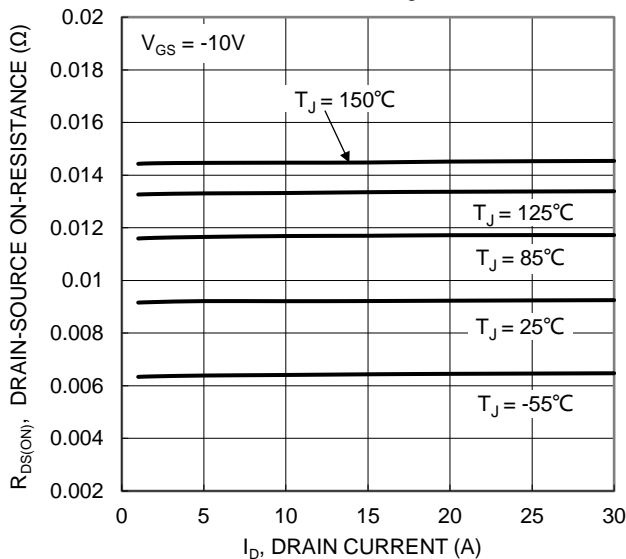


Figure 5. Typical On-Resistance vs. Drain Current and Temperature

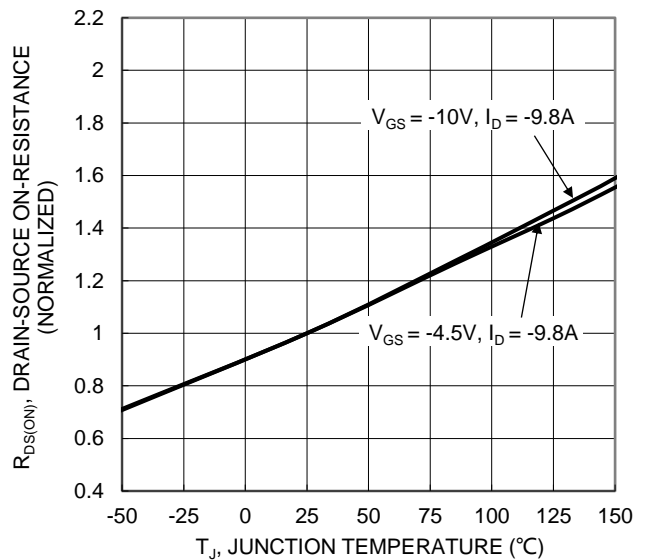


Figure 6. On-Resistance Variation with Temperature

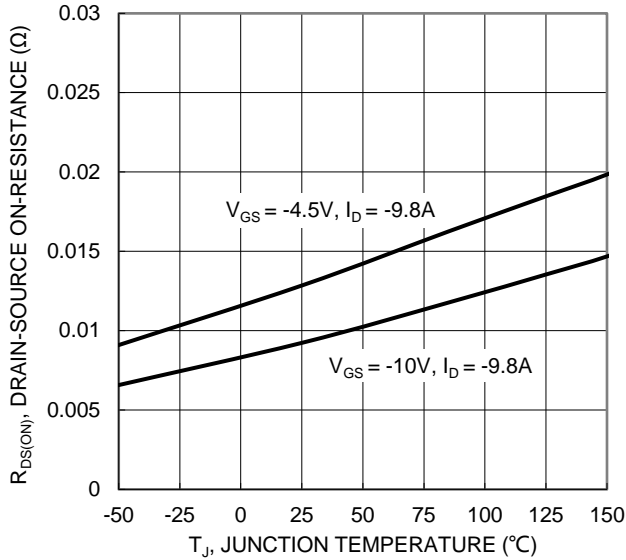


Figure 7. On-Resistance Variation with Temperature

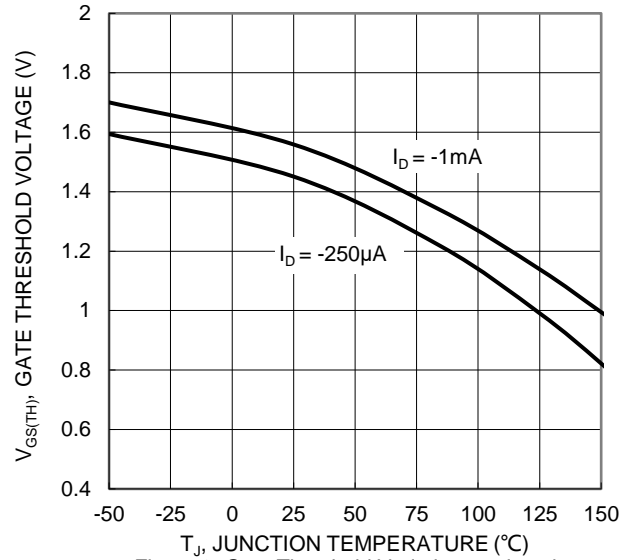


Figure 8. Gate Threshold Variation vs. Junction Temperature

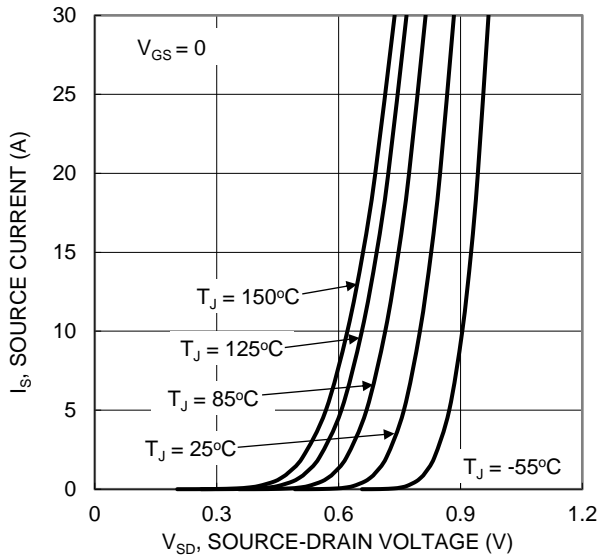


Figure 9. Diode Forward Voltage vs. Current

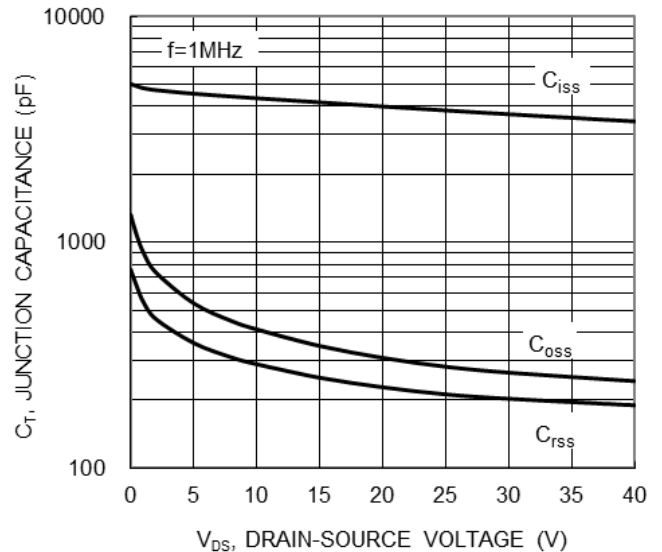


Figure 10. Typical Junction Capacitance

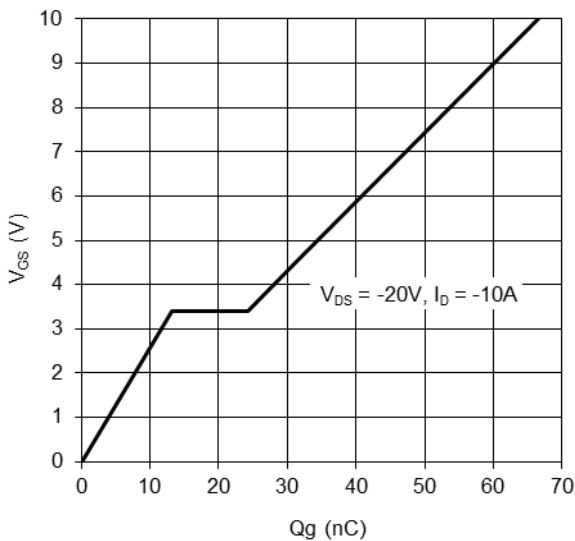


Figure 11. Gate Charge

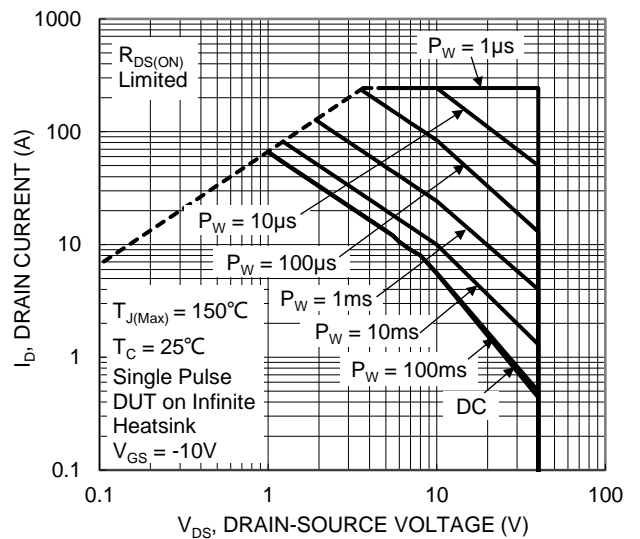


Figure 12. SOA, Safe Operation Area

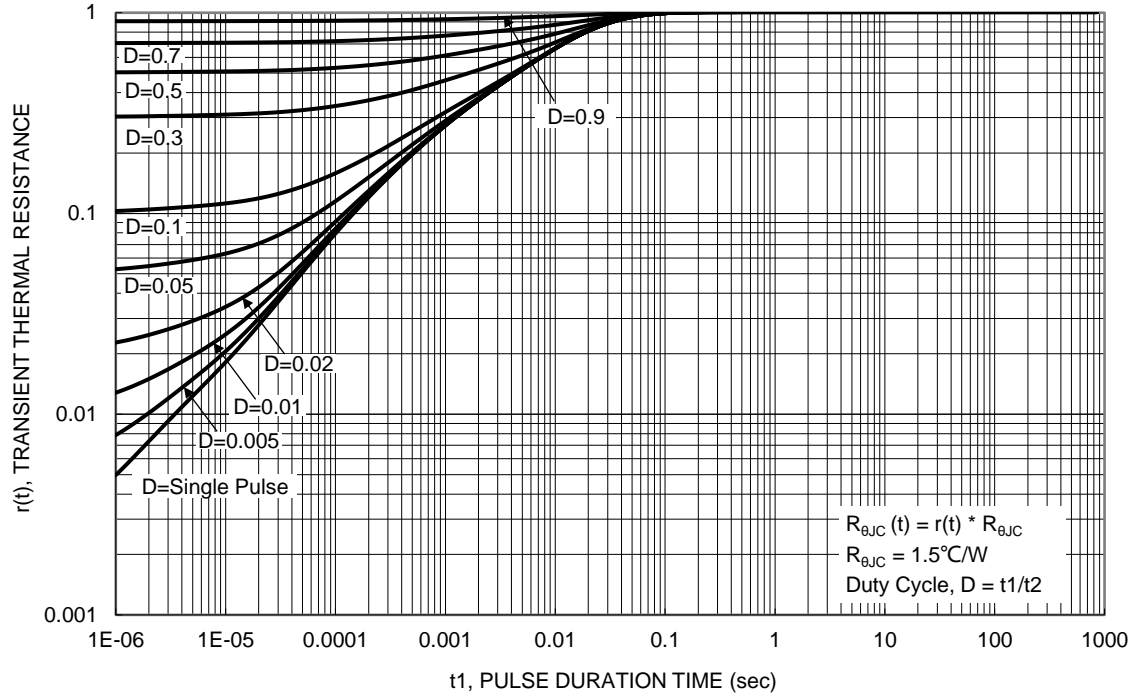
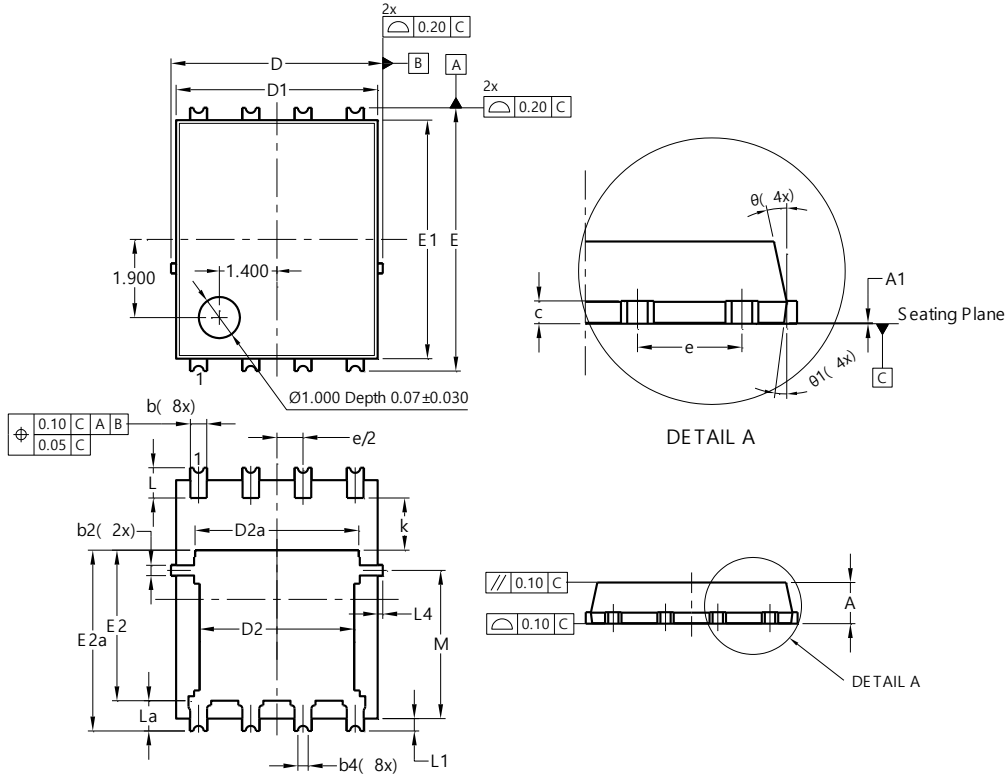


Figure 13. Transient Thermal Resistance

Package Outline Dimensions

Please see <http://www.diodes.com/package-outlines.html> for the latest version.

PowerDI5060-8/SWP (Type UX)

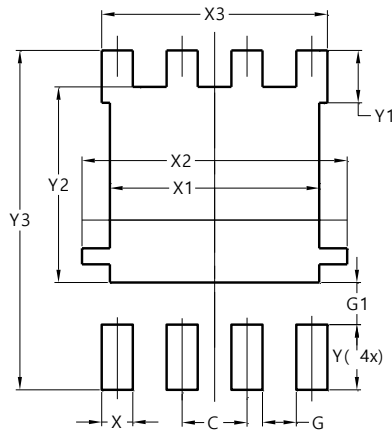


PowerDI5060-8/SWP (Type UX)			
Dim	Min	Max	Typ
A	0.90	1.10	1.00
A1	0	0.05	--
b	0.30	0.50	0.41
b2	0.20	0.35	0.25
b4	0.25REF		
c	0.230	0.330	0.277
D	5.15 BSC		
D1	4.70	5.10	4.90
D2	3.56	3.96	3.76
D2a	3.78	4.18	3.98
E	6.40 BSC		
E1	5.60	6.00	5.80
E2	3.46	3.86	3.66
E2a	4.195	4.595	4.395
e	1.27BSC		
k	1.05	--	--
L	0.635	0.835	0.735
La	0.635	0.835	0.735
L1	0.200	0.400	0.300
L4	0.025	0.225	0.125
M	3.205	4.005	3.605
θ	10°	12°	11°
θ1	6°	8°	7°
All Dimensions in mm			

Suggested Pad Layout

Please see <http://www.diodes.com/package-outlines.html> for the latest version.

PowerDI5060-8/SWP (Type UX)



Dimensions	Value (in mm)
C	1.270
G	0.660
G1	0.820
X	0.610
X1	4.100
X2	5.190
X3	4.420
Y	1.270
Y1	1.020
Y2	3.810
Y3	6.610

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