Description

The LSF0106Q/0108Q is 6/8-CH bi-directional multi-voltage level translator for open-drain and push-pull applications. This device is a universal level translator with A port operating from 0.65V to 4.5V (Vref_A) and B port 1.5V to 5.5V (Vref_B). This range allows for bi-directional voltage translations between 0.65V and 5.0V. Meanwhile, Vref_B is recommended to be at 1V higher than Vref_A for best signal integrity.

The EN pin is used to activate the device. When EN is HIGH, the translator switch is on. Otherwise, EN is LOW, the translator switch is off, and a high-impedance state exists between ports. The EN input must be connected to Vref_B and both pins pulled to HIGH through a pullup resistor (typically 200kΩ). EN must be LOW to ensure the high-impedance state during power-up or power-down.

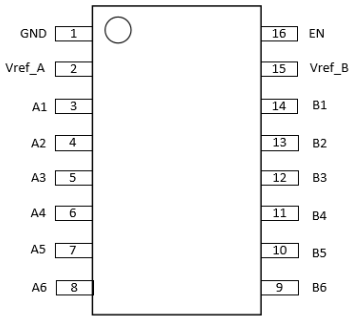
Be aware that external Rpu (pullup resistor) is required on each signal in both A and B ports for push-pull application because a pull-high state can avoid misoperation during power-up or power-down. As same as open-drain application, the smaller Rpu results in the larger driving current. For bi-directional signal flows, there is no need for a direction pin to minimize system effort. This device supports 5V tolerant I/O pins in a variety of applications which require different voltage translation levels.

Features

- Bi-directional level shifter for both push-pull and open-drain
- Maximum data rate is dominated by the system capacitance and pullup resistors
  - ≤ 100MHz; C_L = 15pF, 30pF, Rpu ≤ 300Ω
  - ≤ 50MHz; C_L = 50pF, Rpu ≤ 300Ω
- Bi-directional voltage level translation between:
  - 0.65V and 1.5V, 1.8V, 2.5V, 3.3V and 5.0V
  - 1.2V and 1.8V, 2.5V, 3.3V and 5.0V
  - 1.8V and 2.5V, 3.3V and 5.0V
  - 2.5V and 3.3V and 5.0V
  - 3.3V and 5.0V
- ESD protection exceeds JESD 22
  - 3500V HBM (A114)
  - 1500V CDM (C101)
- Latchup exceeds 100mA per JESD 17
- 5V tolerant I/O pins to support TTL
- Specified from -40°C to +125°C
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**
- **The LSF0106Q/0108Q is suitable for automotive applications requiring specific change control; this part is AEC-Q100 qualified, PPAP capable, and manufactured in IATF16949 certified facilities.**
  https://www.diodes.com/quality/product-definitions/

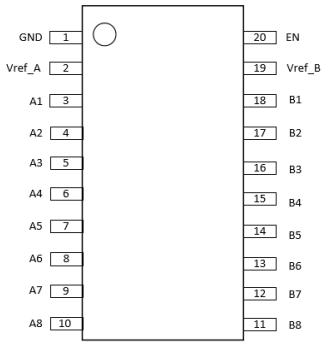
Pin Assignments

LSF0106Q Package

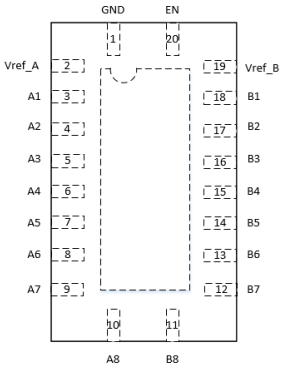


TSSOP-16

LSF0108Q Packages



TSSOP-20 (Future Package)



V-QFN4525-20

Applications

- GPIO, MDIO, SDIO, SVID, UART
- PMBus, SMBus, I2C, and other interfaces
- Telecom infrastructures
- Industrials
- High-performance computing
- Wide array of products such as:
  - PCs, networking, notebooks
  - Smart phones
  - Tablets

Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

Pin Descriptions

LSF0106Q Pin Descriptions

Pin Name	Pin Number	Function
	TSSOP-16	
GND	1	Ground
Vref_A	2	Reference supply voltage; A port
A1	3	Input/output 1
A2	4	Input/output 2
A3	5	Input/output 3
A4	6	Input/output 4
A5	7	Input/output 5
A6	8	Input/output 6
B6	9	Output/input 6
B5	10	Output/input 5
B4	11	Output/input 4
B3	12	Output/input 3
B2	13	Output/input 2
B1	14	Output/input 1
Vref_B	15	Reference supply voltage; B port
EN	16	Enable input (Active HIGH)

LSF0108Q Pin Descriptions

Pin Name	Pin Number		Function
	TSSOP-20	V-QFN4525-20	
GND	1	1	Ground
Vref_A	2	2	Reference supply voltage; A port
A1	3	3	Input/output 1
A2	4	4	Input/output 2
A3	5	5	Input/output 3
A4	6	6	Input/output 4
A5	7	7	Input/output 5
A6	8	8	Input/output 6
A7	9	9	Input/output 7
A8	10	10	Input/output 8
B8	11	11	Output/input 8
B7	12	12	Output/input 7
B6	13	13	Output/input 6
B5	14	14	Output/input 5
B4	15	15	Output/input 4
B3	16	16	Output/input 3
B2	17	17	Output/input 2
B1	18	18	Output/input 1
Vref_B	19	19	Reference supply voltage; B port
EN	20	20	Enable input (Active HIGH)

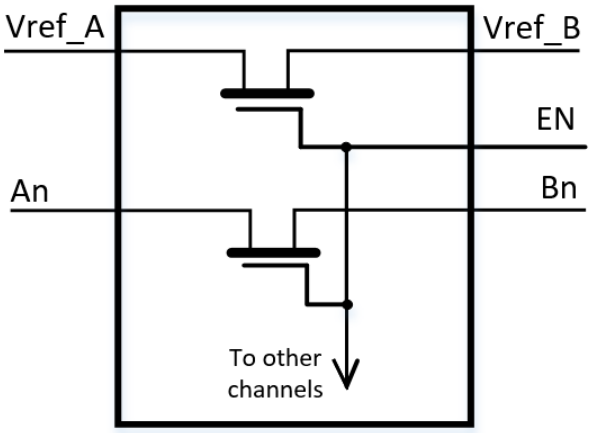
Absolute Maximum Ratings (Note 4)

Symbol	Parameter	Rating	Unit
ESD HBM	Human Body Model ESD Protection	±3.5	kV
ESD CDM	Charged Device Model ESD Protection	±1.5	kV
V_{REF}	Supply Reference Voltage Range	-0.5 to +7.0	V
$V_{I/O}$	Input-Output Voltage Range	-0.5 to +7.0	V
I_{CH}	Continuous Channel Current	128	mA
I_{IK}	Input Clamp Current, $V_I < 0$	-50	mA
T_J	Junction Temperature	+150	°C
T_{STG}	Storage Temperature	-65 to +150	°C

Note: 4. Stresses greater than those listed under *Absolute Maximum Ratings* can cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to *Absolute Maximum Ratings* for extended periods can affect device reliability.

Functional Diagram

NOTE:
See Load Circuit
Suggest to connect EN to Vref_B and both pins pulled to HIGH through a pullup resistor (typically 200kΩ)



Recommended Operating Conditions

Symbol	Parameter	Min	Max	Unit
Vref_A	Reference Voltage, A Port	0.65	4.5	V
Vref_B	Reference Voltage, B Port, when Vref_A ≥ 1V	Vref_A + 0.6	5.5	V
	Reference Voltage, B Port, when Vref_A < 1V	Vref_A + 0.8	5.5	V
$V_{I/O}$	Input/Output Voltage	0	5.5	V
V_{EN}	Enable Voltage when Vref_A ≥ 1V	Vref_A + 0.6	5.5	V
	Enable Voltage when Vref_A < 1V	Vref_A + 0.8	5.5	V
I_{PASS}	Pass Transistor Current	—	64	mA
T_A	Operating Free-Air Temperature	-40	+125	°C

Electrical Characteristics (Over operating free-air temperature range, unless otherwise specified.)

Symbol	Parameter	Test Conditions		Min	Typ (Note 5)	Max	Unit
Vref_A	A port supply voltage	What if config to be low voltage side		0.65	—	4.5	V
Vref_B	B port supply voltage	What if config to be high voltage side		1.5	—	5.5	V
V_{IK}	Input clamping voltage	I_I = -18mA, V_{EN} = 0		-1.2	—	0	V
I_L	Leakage current	Pins An, Bn, Vref_A, Vref_B and EN; V_I = GND to 5.0V		0.001	0.1	3	μA
I_{CC}	Supply current	Vref_B = EN = 5.5V, Vref_A = 4.5V, I_O = 0, V_I = 0V or V_{CC}		—	0.05	5	μA
C_I(Vref_A/B/EN)		V_I = 3V or 0		—	10	—	pF
$C_{IO(off)}$		V_O = 3V or 0, EN = 0		—	5	6	pF
$C_{IO(on)}$		V_O = 3V or 0, EN = 3V		—	10	13	pF
R_{on} (Note 6)		V_I = 0, I_O = 64mA	Vref_A = 3.3V; Vref_B = EN = 5V	—	3	—	Ω
			Vref_A = 2.5V; Vref_B = EN = 5V	—	3	—	
			Vref_A = 1.8V; Vref_B = EN = 5V	—	4	—	
			Vref_A = 1.0V; Vref_B = EN = 5V	—	5	—	
		V_I = 0, I_O = 32mA	Vref_A = 3.3V; Vref_B = EN = 5V	—	3	—	
			Vref_A = 2.5V; Vref_B = EN = 5V	—	3	—	
			Vref_A = 1.8V; Vref_B = EN = 5V	—	4	—	
			Vref_A = 1.0V; Vref_B = EN = 5V	—	5	—	
		V_I = 0, I_O = 20mA	Vref_A = 0.65V; Vref_B = EN = 5V	—	15	—	
		V_I = 1.8V, I_O = 15mA, Vref_A = 3.3V; Vref_B = EN = 5V		—	4	—	
		V_I = 1.0V, I_O = 10mA, Vref_A = 1.8V; Vref_B = EN = 3.3V		—	7	—	
		V_I = 0V, I_O = 10mA	Vref_A = 1.0V; Vref_B = EN = 3.3V	—	5	—	
			Vref_A = 0.65V; Vref_B = EN = 3.3V	—	15	—	
			Vref_A = 1.0V; Vref_B = EN = 1.8V	—	6	—	
			Vref_A = 0.65V; Vref_B = EN = 1.8V	—	15	—	

Notes: 5. All typical values are measured at T_A = +25°C.
6. Measured by the voltage drop between the A and B pins at the indicated current through the switch. On-state resistance is determined by the lowest voltage of the two (A or B) pins.

Translating Down Switching Characteristics (Note 7, T_A = +25°C, unless otherwise specified.)

Translating Down, 5.0V to 1.8V

Parameter	From (Input)	To (Output)	C_L = 50pF	C_L = 30pF	C_L = 15pF	Unit
			Typ	Typ	Typ	
t_{PLH}	B	A	0.5	0.3	0.2	ns
t_{PHL}			0.9	0.7	0.5	ns
Test conditions: V_{ref_A} = 1.8V, V_{PU} = V_{IH} = 5.0V, V_M = 0.9V, PRR = 10MHz (unless otherwise noted, see load circuit)						

Translating Down, 3.3V to 1.8V

Parameter	From (Input)	To (Output)	C_L = 50pF	C_L = 30pF	C_L = 15pF	Unit
			Typ	Typ	Typ	
t_{PLH}	B	A	0.4	0.2	0.1	ns
t_{PHL}			1.0	0.7	0.4	ns
Test conditions: V_{ref_A} = 1.8V, V_{PU} = V_{IH} = 3.3V, V_M = 0.9V, PRR = 10MHz (unless otherwise noted, see load circuit)						

Translating Down, 3.3V to 1.2V

Parameter	From (Input)	To (Output)	C_L = 50pF	C_L = 30pF	C_L = 15pF	Unit
			Typ	Typ	Typ	
t_{PLH}	B	A	0.6	0.4	0.2	ns
t_{PHL}			1.1	0.8	0.6	ns
Test conditions: V_{ref_A} = 1.2V, V_{PU} = V_{IH} = 3.3V, V_M = 0.6V, PRR = 10MHz (unless otherwise noted, see load circuit)						

Translating Down, 1.8V to 1.2V

Parameter	From (Input)	To (Output)	C_L = 50pF	C_L = 30pF	C_L = 15pF	Unit
			Typ	Typ	Typ	
t_{PLH}	B	A	0.5	0.3	0.1	ns
t_{PHL}			1.8	1.4	1.1	ns
Test conditions: V_{ref_A} = 1.2V, V_{PU} = V_{IH} = 1.8V, V_M = 0.6V, PRR = 10MHz (unless otherwise noted, see load circuit)						

Translating Down, 1.8V to 0.8V

Parameter	From (Input)	To (Output)	C_L = 50pF	C_L = 30pF	C_L = 15pF	Unit
			Typ	Typ	Typ	
t_{PLH}	B	A	0.7	0.4	0.2	ns
t_{PHL}			1.5	1.2	0.9	ns
Test conditions: V_{ref_A} = 0.8V, V_{PU} = V_{IH} = 1.8V, V_M = 0.4V, PRR = 10MHz (unless otherwise noted, see load circuit)						

Translating Down, 1.8V to 0.65V

Parameter	From (Input)	To (Output)	C_L = 50pF	C_L = 30pF	C_L = 15pF	Unit
			Typ	Typ	Typ	
t_{PLH}	B	A	0.8	0.5	0.3	ns
t_{PHL}			1.6	1.2	1.0	ns
Test conditions: V_{ref_A} = 0.65V, V_{PU} = V_{IH} = 1.5V, V_M = 0.32V, PRR = 10MHz (unless otherwise noted, see load circuit)						

Translating Down, 1.5V to 0.65V

Parameter	From (Input)	To (Output)	C_L = 50pF	C_L = 30pF	C_L = 15pF	Unit
			Typ	Typ	Typ	
t_{PLH}	B	A	1.0	0.6	0.4	ns
t_{PHL}			1.9	1.5	1.1	ns
Test conditions: V_{ref_A} = 0.65V, V_{PU} = V_{IH} = 1.5V, V_M = 0.4V, PRR = 10MHz (unless otherwise noted, see load circuit)						

Note: 7. All typical values are measured at T_A = +25°C. Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10MHz; ZO = 50Ω. Definitions test circuit: C_L = Load capacitance including jig and probe capacitance; R_L = Load resistance = 300Ω; Rpu = ext. pullup resistance = 200kΩ.

Translating Up Switching Characteristics (Note 7, T_A = +25°C, unless otherwise specified.)

Translating Up, 1.8V to 5.0V

Parameter	From (Input)	To (Output)	C_L = 50pF	C_L = 30pF	C_L = 15pF	Unit
			Typ	Typ	Typ	
t_{PLH}	A	B	0.4	0.3	0.3	ns
t_{PHL}			2.3	1.7	1.0	ns
Test conditions: V_{IH} = V_{ref_A} = 1.8V, V_{EXT} = V_{PU} = 5.0V, R_L = 300Ω, V_M = 0.9V, PRR = 10MHz (unless otherwise noted, see load circuit)						

Translating Up, 1.8V to 3.3V

Parameter	From (Input)	To (Output)	C_L = 50pF	C_L = 30pF	C_L = 15pF	Unit
			Typ	Typ	Typ	
t_{PLH}	A	B	0.4	0.3	0.3	ns
t_{PHL}			1.7	1.2	0.6	ns
Test conditions: V_{IH} = V_{ref_A} = 1.8V, V_{EXT} = V_{PU} = 3.3V, R_L = 300Ω, V_M = 0.9V, PRR = 10MHz (unless otherwise noted, see load circuit)						

Translating Up, 1.2V to 3.3V

Parameter	From (Input)	To (Output)	C_L = 50pF	C_L = 30pF	C_L = 15pF	Unit
			Typ	Typ	Typ	
t_{PLH}	A	B	0.4	0.3	0.2	ns
t_{PHL}			2.9	2.2	1.6	ns
Test conditions: V_{IH} = V_{ref_A} = 1.2V, V_{EXT} = V_{PU} = 3.3V, R_L = 300Ω, V_M = 0.6V, PRR = 10MHz (unless otherwise noted, see load circuit)						

Translating Up, 1.2V to 1.8V

Parameter	From (Input)	To (Output)	C_L = 50pF	C_L = 30pF	C_L = 15pF	Unit
			Typ	Typ	Typ	
t_{PLH}	A	B	0.6	0.3	0.2	ns
t_{PHL}			2.8	2.3	1.8	ns
Test conditions: V_{IH} = V_{ref_A} = 1.2V, V_{EXT} = V_{PU} = 1.8V, R_L = 300Ω, V_M = 0.6V, PRR = 10MHz (unless otherwise noted, see load circuit)						

Translating Up, 0.8V to 1.8V

Parameter	From (Input)	To (Output)	C_L = 50pF	C_L = 30pF	C_L = 15pF	Unit
			Typ	Typ	Typ	
t_{PLH}	A	B	0.6	0.3	0.2	ns
t_{PHL}			3.7	2.9	2.1	ns
Test conditions: V_{IH} = V_{ref_A} = 0.8V, V_{EXT} = V_{PU} = 1.8V, R_L = 300Ω, V_M = 0.4V, PRR = 10MHz (unless otherwise noted, see load circuit)						

Translating Up, 0.65V to 1.8V

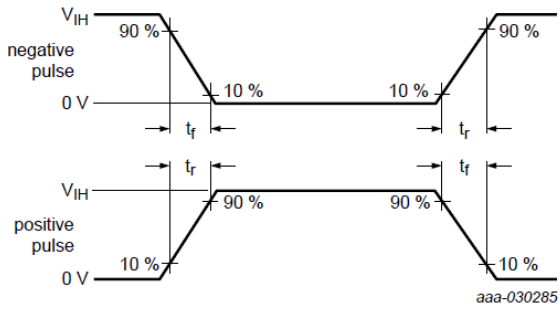
Parameter	From (Input)	To (Output)	C_L = 50pF	C_L = 30pF	C_L = 15pF	Unit
			Typ	Typ	Typ	
t_{PLH}	A	B	0.7	0.3	0.2	ns
t_{PHL}			5.0	3.8	2.7	ns
Test conditions: V_{IH} = V_{ref_A} = 0.65V, V_{EXT} = V_{PU} = 1.8V, R_L = 300Ω, V_M = 0.32V, PRR = 10MHz (unless otherwise noted, see load circuit)						

Translating Up, 0.65V to 1.5V

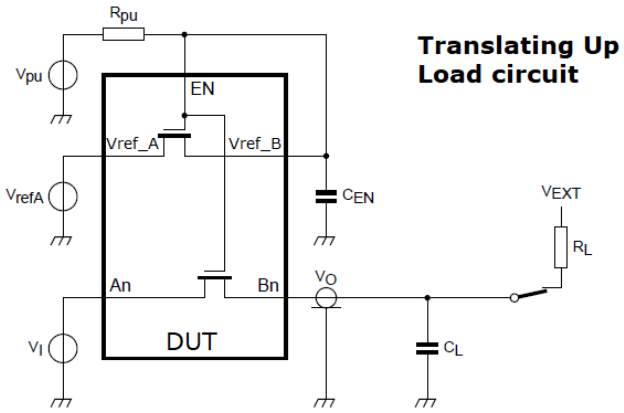
Parameter	From (Input)	To (Output)	C_L = 50pF	C_L = 30pF	C_L = 15pF	Unit
			Typ	Typ	Typ	
t_{PLH}	A	B	0.7	0.3	0.2	ns
t_{PHL}			5.0	3.8	2.7	ns
Test conditions: V_{IH} = V_{ref_A} = 0.65V, V_{EXT} = V_{PU} = 1.8V, R_L = 300Ω, V_M = 0.32V, PRR = 10MHz (unless otherwise noted, see load circuit)						

Note: 7. All typical values are measured at T_A = +25°C. Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10MHz; ZO = 50Ω. Definitions test circuit: C_L = Load capacitance including jig and probe capacitance; R_L = Load resistance = 300Ω; Rpu = ext. pullup resistance = 200kΩ.

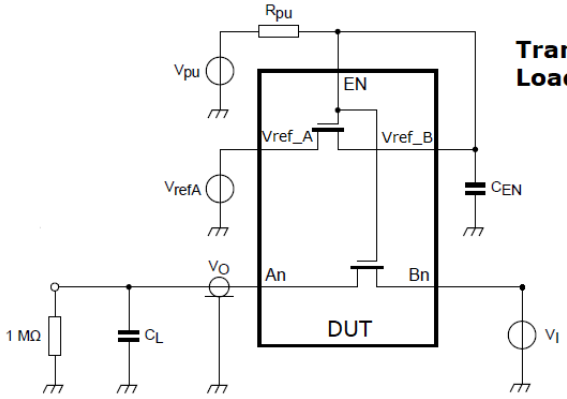
Parameter Measurement Information



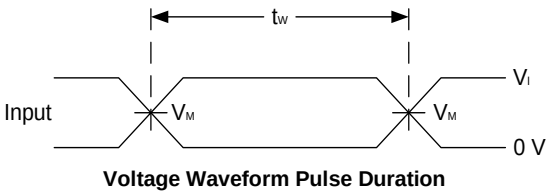
V_I source waveform



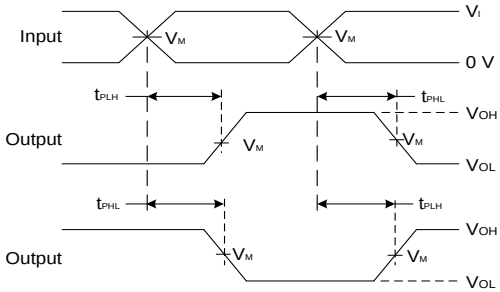
Translating Up Load circuit



Translating Down Load circuit



Voltage Waveform Pulse Duration



Voltage Waveform Propagation Delay Times
Inverting and Non-Inverting Outputs

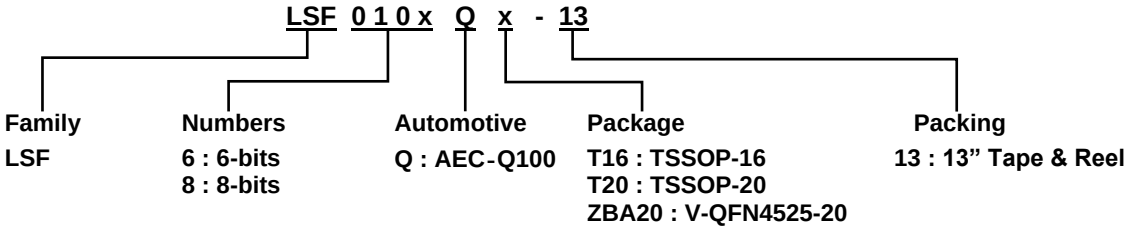
Figure 1. Load Circuit and Voltage Waveforms, Rpu = 200kΩ, C_{EN} = 0.1µF, R_L = 300Ω, C_L = 15pF, 30pF, 50pF

Package Characteristics

Symbol	Parameter	Package	Test Conditions	Min	Typ	Max	Unit
θ_{JA}	Thermal Resistance Junction-to-Ambient	TSSOP-16	Note 8	—	136	—	°C/W
		TSSOP-20		—	95	—	
		V-QFN4525-20		—	59	—	
θ_{JC}	Thermal Resistance Junction-to-Case	TSSOP-16	Note 8	—	57	—	
		TSSOP-20		—	22	—	
		V-QFN4525-20		—	22	—	

Note: 8. Test condition for each of the 3 package types: device mounted on JEDEC standard PCB per JESD51, with minimum recommended pad layout.

Ordering Information



Orderable Part Number	Part Number Suffix	Package Code	Package	Packing (Note 9)	
				Qty.	Carrier
LSF0106QT16-13	-13	T16	TSSOP-16	2500	13” Tape and Reel
LSF0108QT20-13	-13	T20	TSSOP-20 (Future Package)	4000	13” Tape and Reel
LSF0108QZBA20-13	-13	ZBA20	V-QFN4525-20	2500	13” Tape and Reel

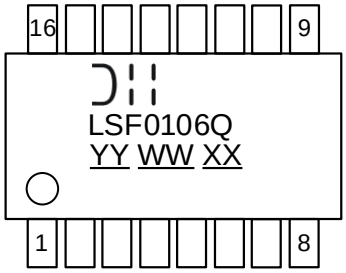
Notes: 9. The taping orientation is located on our website at https://www.diodes.com/assets/Packaging-Support-Docs/ap02007.pdf
10. For packaging details, go to our website at https://www.diodes.com/design/support/packaging/diodes-packaging/.
11. Pad layout as shown in Diodes Incorporated's package outline PDFs, which can be found on our website at http://www.diodes.com/package-outlines.html.

Marking Information

For LSF0106Q

(1) TSSOP-16

(Top View)



YY : Year (ex: 24 = 2024)
WW : Week : 01 to 52; 52 represents week 52 and 53
XX : Internal Code

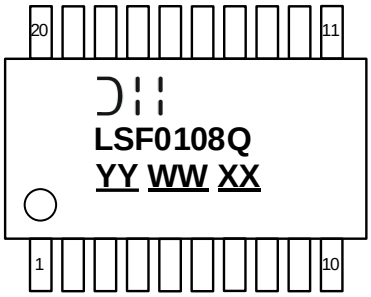
Orderable Part Number	Package	Identification Code
LSF0106QT16-13	TSSOP-16	LSF0106Q

Marking Information (continued)

For LSF0108Q

(1) TSSOP-20

(Top View)

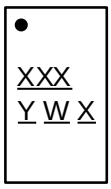


YY : Year (ex: 24 = 2024)
WW : Week : 01 to 52; 52 represents week 52 and 53
XX : Internal Code

Orderable Part Number	Package	Identification Code
LSF0108QT20-13	TSSOP-20	LSF0108Q

(2) V-QFN4525-20

(Top View)



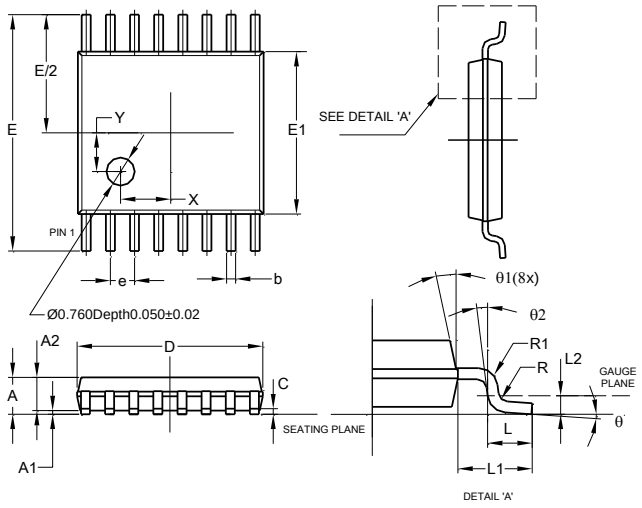
XXX : Identification Code
Y : Year : 0 to 9 (ex: 4 = 2024)
W : Week : A to Z : week 1 to 26; a to z : week 27 to 52; z represents week 52 and 53
X : Internal Code

Orderable Part Number	Package	Identification Code
LSF0108QZBA20-13	V-QFN4525-20	JHQ

Package Outline Dimensions (LSF0106Q)

Please see http://www.diodes.com/package-outlines.html for the latest version.

TSSOP-16

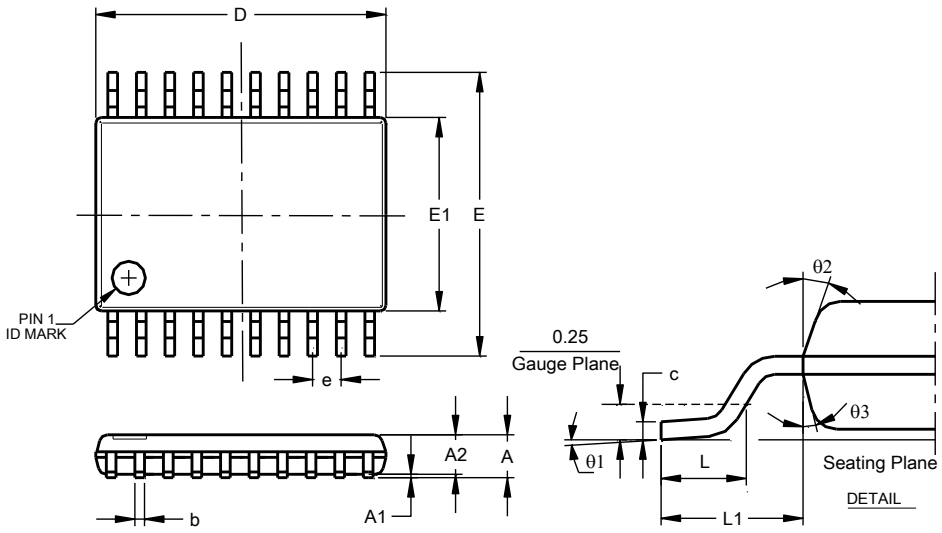


TSSOP-16			
Dim	**Min**	**Max**	**Typ**
A	-	1.08	-
A1	0.05	0.15	-
A2	0.80	0.93	-
b	0.19	0.30	-
c	0.09	0.20	-
D	4.90	5.10	-
E	6.40 BSC		
E1	4.30	4.50	-
e	0.65 BSC		
L	0.45	0.75	-
L1	1.00 REF		
L2	0.25 BSC		
R / R1	0.09	-	-
X	-	-	1.350
Y	-	-	1.050
θ	0°	8°	-
θ1	5°	15°	-
θ2	0°	-	-
All Dimensions in mm			

Package Outline Dimensions (LSF0108Q)

Please see http://www.diodes.com/package-outlines.html for the latest version.

TSSOP-20

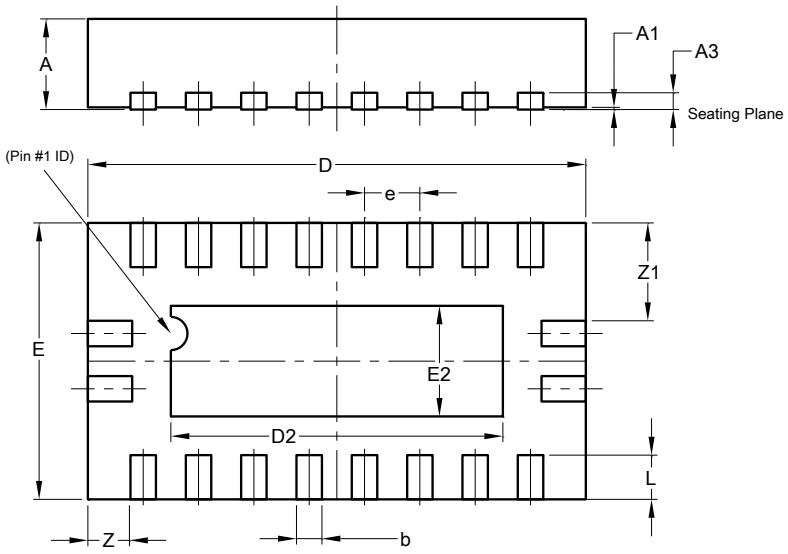


TSSOP-20			
Dim	**Min**	**Max**	**Typ**
A	-	1.20	-
A1	0.05	0.15	-
A2	0.80	1.05	-
b	0.19	0.30	-
c	0.09	0.20	-
D	6.40	6.60	6.50
E	6.20	6.60	6.40
E1	4.30	4.50	4.40
e	0.65 BSC		
L	0.45	0.75	0.60
L1	1.0 REF		
θ1	0°	8°	-
θ2	10°	14°	12°
θ3	10°	14°	12°
All Dimensions in mm			

Package Outline Dimensions (LSF0108Q) (continued)

Please see http://www.diodes.com/package-outlines.html for the latest version.

V-QFN4525-20

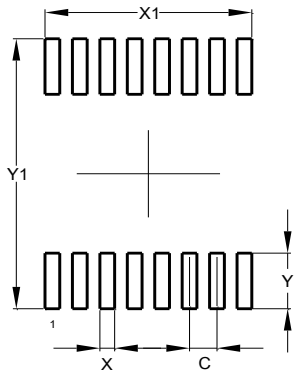


V-QFN4525-20			
Dim	**Min**	**Max**	**Typ**
A	0.75	0.85	0.80
A1	0.00	0.05	0.02
A3	-	-	0.15
b	0.18	0.30	0.23
D	4.45	4.55	4.50
D2	2.85	3.15	3.00
E	2.45	2.55	2.50
E2	0.85	1.15	1.00
e	0.50BSC		
L	0.30	0.50	0.40
Z	-	-	0.385
Z1	-	-	0.885
All Dimensions in mm			

Suggested Pad Layout (LSF0106Q)

Please see http://www.diodes.com/package-outlines.html for the latest version.

TSSOP-16

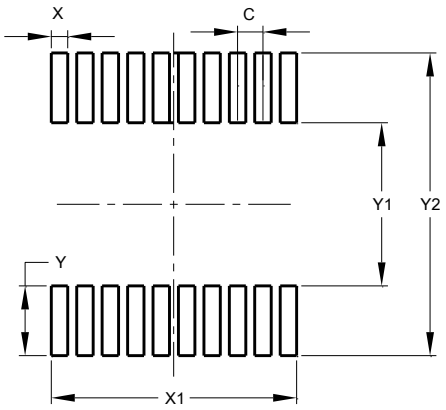


Dimensions	Value (in mm)
C	0.650
X	0.350
X1	4.900
Y	1.400
Y1	6.800

Suggested Pad Layout (LSF0108Q)

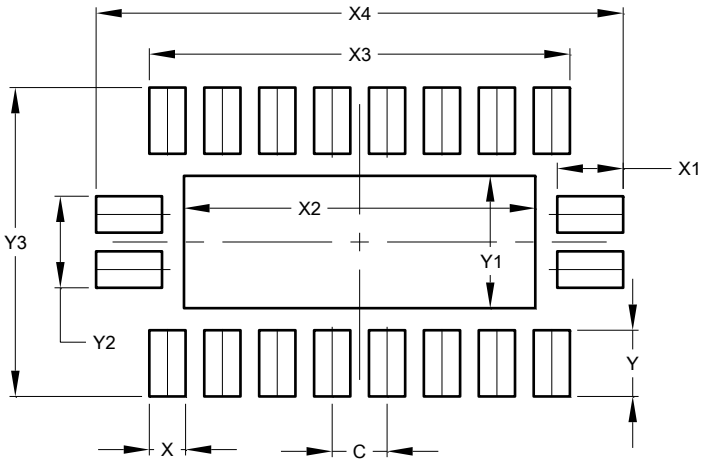
Please see http://www.diodes.com/package-outlines.html for the latest version.

TSSOP-20



Dimensions	Value (in mm)
C	0.650
X	0.420
X1	6.270
Y	1.780
Y1	4.160
Y2	7.720

V-QFN4525-20



Dimensions	Value (in mm)
C	0.500
X	0.330
X1	0.600
X2	3.200
X3	3.830
X4	4.800
Y	0.600
Y1	1.200
Y2	0.830
Y3	2.800

Mechanical Data

- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals: Finish – Matte Tin Plated Leads, Solderable per MIL-STD-202, Method 208 e3
- Max Soldering Temperature +260°C for 30 secs as per JEDEC J-STD-020
- Weight:
  - TSSOP-16: 0.054811 grams (Approximate)
  - TSSOP-20: 0.071 grams (Approximate)
  - V-QFN4525-20: 0.024 grams (Approximate)

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