

4W STEREO CLASS-D AUDIO AMPLIFIER AND CLASS-AB HEADPHONE DRIVER WITH ADJUSTABLE DC VOLUME CONTROL, NON-CLIP POWER LIMIT AND SSM
Description

The PAM8019E is a stereo 4W Class-D audio-power amplifier for driving bridged-tied speakers and includes a stereo Class-AB amplifier for driving headphones. With advanced 62 step DC volume control to minimize external components, PAM8019E is capable of allowing simple and accurate volume control over the gain range of +20dB (Volume = 0V) to -60dB (Volume = V_{DD}).

Integrated with spread spectrum modulation (SSM) design for EMI suppression, the PAM8019E enables the use of inexpensive ferrite bead filters. The integrated non-clip power limit (PLIM) technology suppresses output automatically with programmable power limit, while improving the sound quality and helping to protect the speakers.

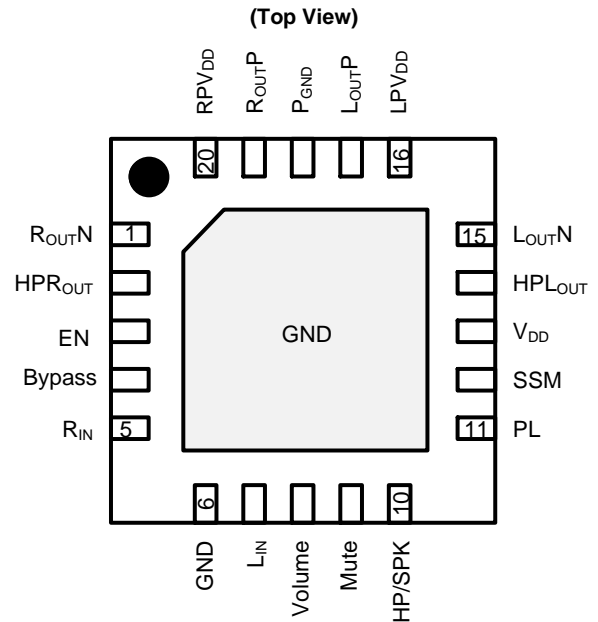
The PAM8019E supports speakers open short detection during startup to protect the whole audio system before normal operation starts. Protection features also include undervoltage protection, DC input protection, short-circuit protection on all audio outputs, and thermal shutdown of the entire system.

The PAM8019E is designed to be pop free for the Class-D amplifier and headphone driver under all kinds of operating conditions.

The PAM8019E is available in the power-efficient and space-saving U-QFN4040-20 and U-QFN3030-20 packages.

Features

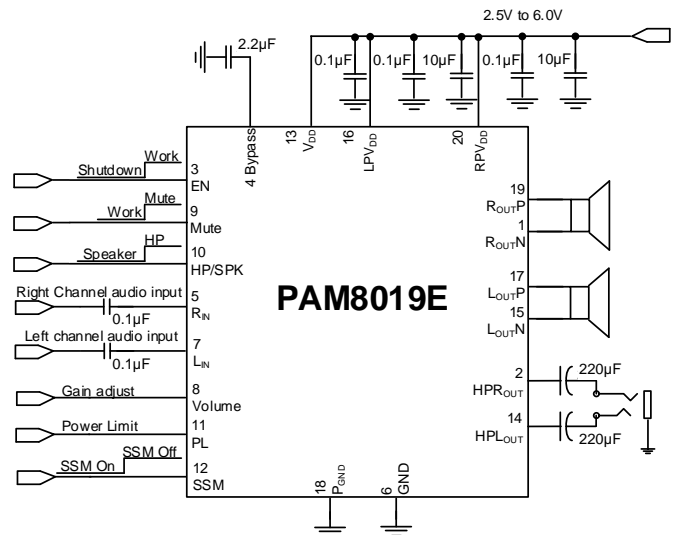
- Operating Voltage: 2.5V to 6.0V
- 4W Stereo Class D with 88mW Class-AB Headphone Driver
- Output Power
 - Class-D Amplifier THD+N = 10%
 $V_{DD} = 5V$: $R_L = 4\Omega$, $P_O = 3W$; $R_L = 8\Omega$, $P_O = 1.78W$
 $V_{DD} = 5.8V$: $R_L = 4\Omega$, $P_O = 4W$; $R_L = 8\Omega$, $P_O = 2.34W$
 - Class-D Amplifier THD+N = 1%
 $V_{DD} = 5V$: $R_L = 4\Omega$, $P_O = 2.41W$; $R_L = 8\Omega$, $P_O = 1.44W$
 $V_{DD} = 5.8V$: $R_L = 4\Omega$, $P_O = 3.27W$; $R_L = 8\Omega$, $P_O = 1.92W$
 - Class-AB Headphone Amplifier THD+N = 1%
 $V_{DD} = 5V$, $R_L = 32\Omega$, $P_O = 66mW$
 $V_{DD} = 5.8V$, $R_L = 32\Omega$, $P_O = 88mW$
- 40 μ Vrms Noise of Class-D Amplifier at the max Gain
- 90% Efficiency at $V_{DD} = 5V$, $P_O = 3W$ x 2ch, 4 Ω Loading
- 62 Step DC Volume Control with Hysteresis from -60dB to +20dB
- Non-Clip Power Limit (NCPL) and AGC Function
- Speaker Open Short Detection During Startup
- SSM Help Easily Pass EMI with Simple FB-C
- Thermal and Overcurrent Protection with Auto-Recovery
- Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- Halogen and Antimony Free. "Green" Device (Note 3)**
- For automotive applications requiring specific change control (i.e. parts qualified to AEC-Q100/101/104/200, PPAP capable, and manufactured in IATF 16949 certified facilities), please [contact us](mailto:contact@diodes.com) or your local Diodes representative. <https://www.diodes.com/quality/product-definitions/>**

Pin Assignments


U-QFN4040-20/U-QFN3030-20

Applications

- LCD monitors and TVs
- Projectors/all-in-one computers
- Portable/active speakers
- Bone conductive headphones
- DVD players

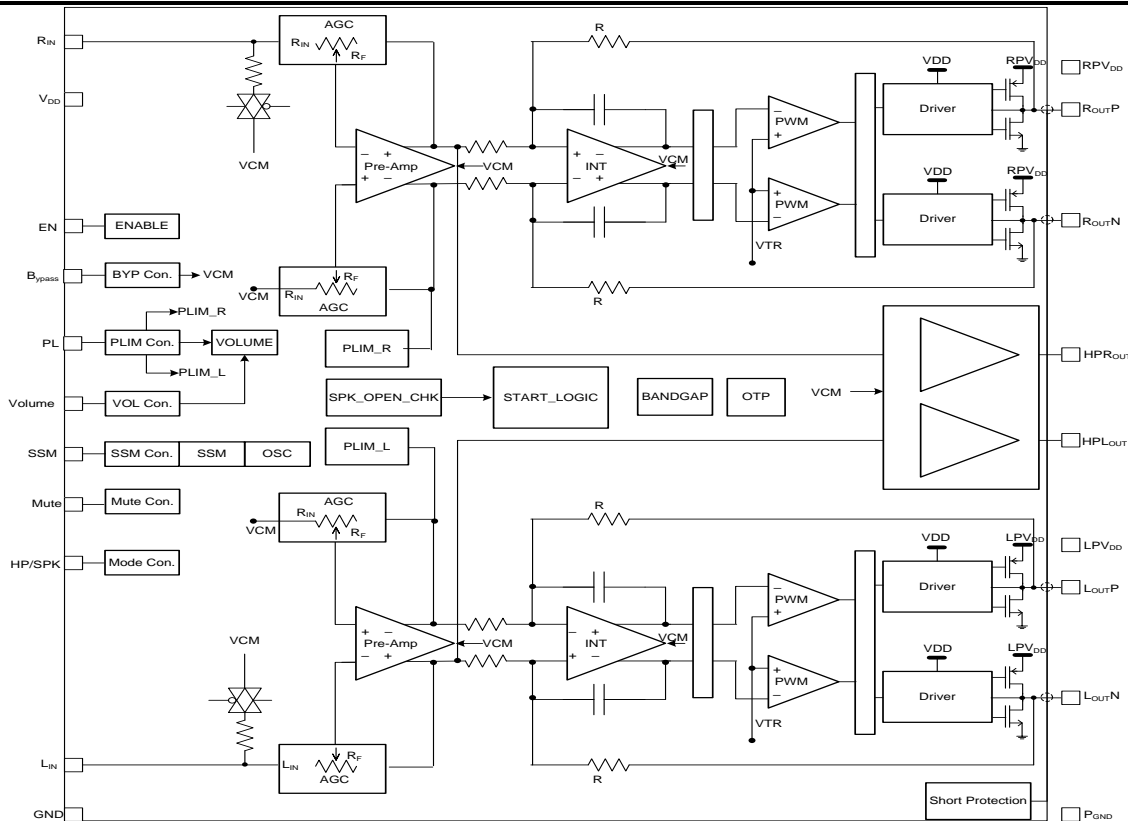
Typical Applications Circuit


Notes: 1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
 2. See <https://www.diodes.com/quality/lead-free/> for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
 3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

Pin Descriptions

Pin Number	Name	I/O/P	Function
3	EN	I	Low: chip shutdown with outputs Hi-Z, High: outputs enabled
4	Bypass	O	Bias Voltage for Power Amplifier
5	R _{IN}	I	Negative Input of Right Channel Power Amplifier
6	GND	—	Analog Ground Connection
18	P _{GND}	—	Power Ground Connection
7	L _{IN}	I	Negative Input of Left Channel Power Amplifier
8	Volume	I	Internal Gain Setting Input Connect to GND which set Class D and HP as the max Gain.
9	Mute	I/O	Mute Control Signal Input (High: outputs Hi-Z, Low: outputs enabled). During startup, Mute pin will set as high if speakers not good connect
10	HP/SPK	I	Output Mode Control Input High: Headphone Mode, Low: Speaker Mode
11	PL	I	Power limit reference voltage, see applications section for further details
12	SSM	I	Low: SSM ON, High: SSM OFF
13	V _{DD}	P	Analog Power Supply
16	LPV _{DD}	P	Left Channel Power Supply
20	RPV _{DD}	P	Right Channel Power Supply
14	HPL _{OUT}	O	Headphone — Left Channel Output
2	HPR _{OUT}	O	Headphone — Right Channel Output
15	L _{OUTN}	O	Power Amplifier — Left Channel Negative Output
17	L _{OUTP}	O	Power Amplifier — Left Channel Positive Output
19	R _{OUTP}	O	Power Amplifier — Right Channel Negative Output
1	R _{OUTN}	O	Power Amplifier — Right Channel Positive Output
Thermal PAD	GND	—	Connect to Power Ground (recommended)

Functional Block Diagram



Absolute Maximum Ratings (@T_A = +25°C, unless otherwise specified.) (Note 4)

Symbol	Parameter	Rating	Unit
V _{DD}	Supply Voltage (V _{DD} , LPV _{DD} , RPV _{DD})	-0.3 to 6.5	V
V _{IN}	Input Pin Voltage (EN, Mute, Volume, SSM, PL, HP/SPK, R _{IN} , L _{IN})	-0.3 to V _{DD}	
T _J	Maximum Junction Temperature	+150	°C
T _{STG}	Storage Temperature Range	-65 to +150	
T _{SDR}	Maximum Soldering Temperature Range, 5 Seconds	+300	

Notes: 4. Stresses greater than *Absolute Maximum Ratings* specified above can cause permanent damage to the device. These are stress ratings only; functional operation of the device at these or any other conditions exceeding those indicated in this specification is not implied. Device reliability can be affected by exposure to absolute maximum rating conditions for extended periods of time.

ESD Ratings

Symbol	Parameter	Rating	Unit
V _{ESD}	Human Body Model (HBM)	±2000	V
	Charged Device Model (CDM)	±1000	V
Latch up	Latch up (I Trigger)	±100	mA
	Latch up (Overvoltage Test)	8.4	V

Recommended Operating Conditions (@T_A = +25°C, unless otherwise specified.)

Symbol	Parameter	Max	Unit
V _{DD}	Supply Voltage Range	2.5 to 6.0	V
V _{IH}	High-Level Threshold Voltage	EN, Mute, SSM, HP/SPK	1.4 to V _{DD}
V _{IL}	Low-Level Threshold Voltage	EN, Mute, SSM, HP/SPK	0 to 0.5
V _{ICM}	Common Mode Input Voltage	1 to V _{DD} - 1	V
T _A	Ambient Operation Temperature Range	-40 to +85	°C
T _J	Junction Temperature Range	-40 to +125	

Thermal Information (@T_A = +25°C, unless otherwise specified.)

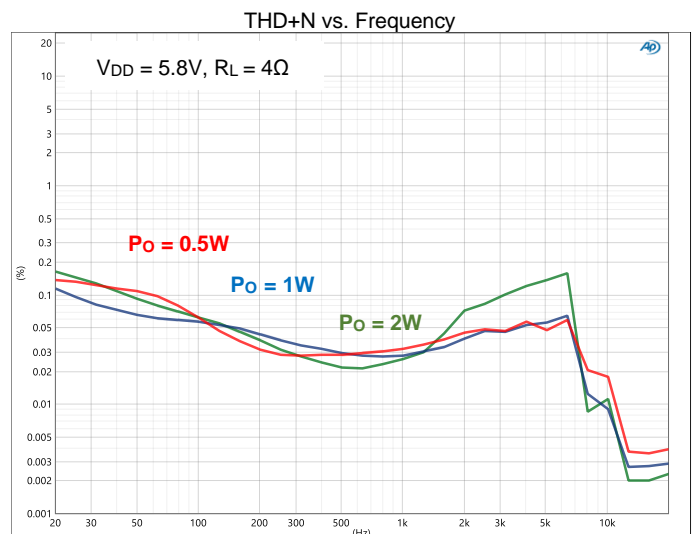
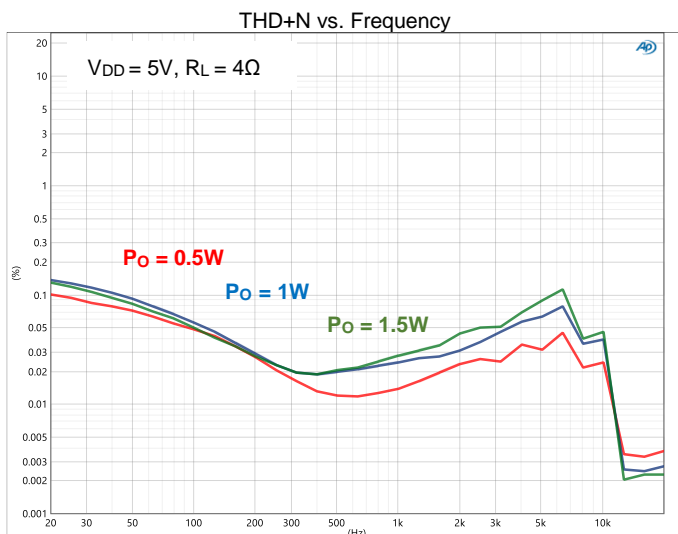
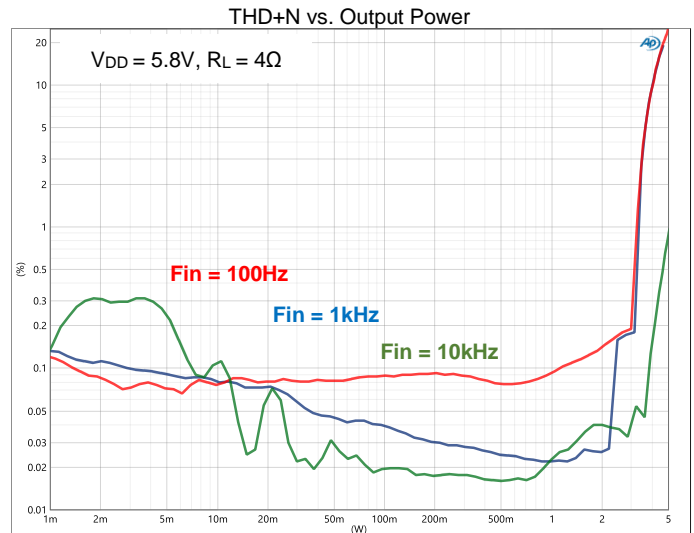
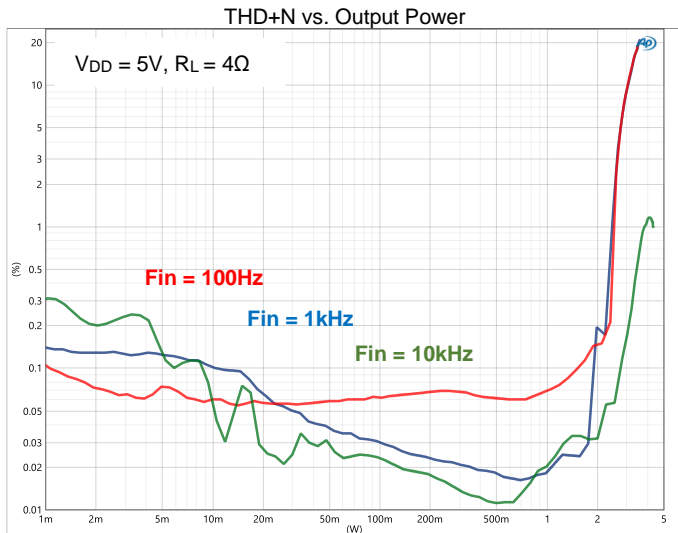
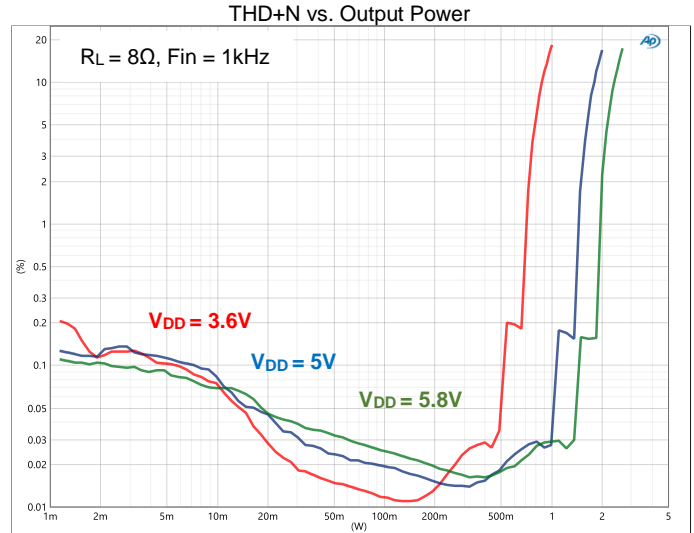
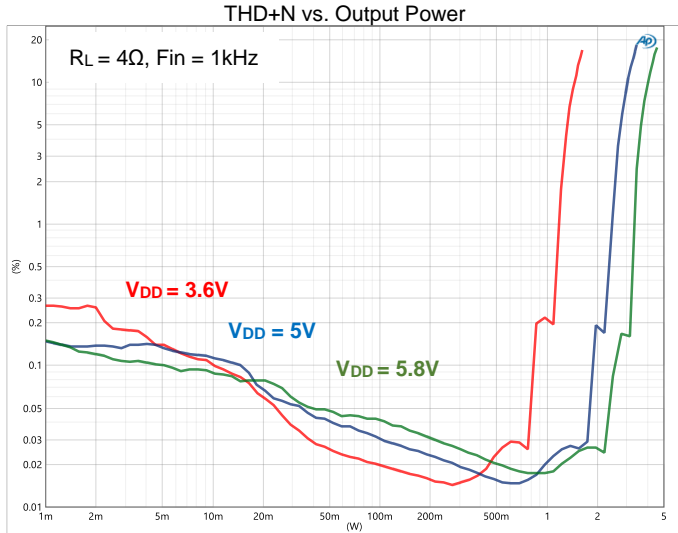
Symbol	Parameter	Package	Typical Value	Unit
θ _{JA}	Thermal Resistance — Junction to Ambient	U-QFN4040-20	41	°C/W
		U-QFN3030-20	43	°C/W
θ _{JC}	Ambient Operation Temperature Range	U-QFN4040-20	17	°C/W
		U-QFN3030-20	20	°C/W

Electrical Characteristics (@T_A = +25°C, V_{DD} = 5V, Gain = Max, R_L = 4Ω, PL = 5V, unless otherwise specified.)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Speaker Mode						
V _{DD}	Supply Voltage Range	—	2.5	—	6.0	V
I _Q	Quiescent Current (Speaker Mode)	V _{Mute} = 0, V _{DD} = 5V, 4Ω Load	—	6.4	12	mA
I _Q	Quiescent Current (HP Mode)	V _{Mute} = 0, V _{DD} = 5V, 32Ω Load	—	4.3	8	mA
I _{Mute}	Mute Current (Speaker Mode)	V _{Mute} = 5V, V _{DD} = 5V, 4Ω Load	—	2.8	6	mA
I _{Mute}	Mute Current (HP Mode)	V _{Mute} = 5V, V _{DD} = 5V, 32Ω Load	—	2.8	6	mA
I _{SD}	Shutdown Current	V _{SD} = 0, V _{DD} = 0, 4Ω Load	—	—	1	μA
f _{OSC}	Oscillator Frequency	SSM Off	234	384	534	kHz
R _i	Input Resistance (Speaker Mode)	Gain = 20dB	—	10	—	kΩ
R _i	Input Resistance (HP Mode)	Gain = 3.5dB	—	44	—	kΩ
V _{OS}	Output Offset Voltage	No Load	—	1	25	mV
R _{DS(on)}	Drain-Source On-State Resistance	V _{DD} = 5.0V, I _{DS} = 0.8A, pMOSFET	—	0.22	—	Ω
		V _{DD} = 5.0V, I _{DS} = 0.8A, nMOSFET	—	0.22	—	
T _{STARTUP}	Startup Time from Shutdown	Bypass Capacitor, C _b = 2.2μF	—	70	200	ms
P _O	Output Power	V _{DD} = 5V, f = 1kHz, R _L = 8Ω, THD+N = 1%	—	1.44	—	W
		V _{DD} = 5V, f = 1kHz, R _L = 8Ω, THD+N = 10%	—	1.78	—	
		V _{DD} = 5V, f = 1kHz, R _L = 4Ω, THD+N = 1%	—	2.41	—	
		V _{DD} = 5V, f = 1kHz, R _L = 4Ω, PL = 0	—	2.5	—	
		V _{DD} = 5V, f = 1kHz, R _L = 4Ω, THD+N = 10%	—	3.01	—	
		V _{DD} = 5.8V, f = 1kHz, R _L = 4Ω, THD+N = 1%	—	3.27	—	
		V _{DD} = 5.8V, f = 1kHz, R _L = 4Ω, PL = 0	—	3.5	—	
THD+N	Total Harmonic Distortion Plus Noise	R _L = 8Ω, P _O = 0.8W, f = 1kHz	—	0.032	—	%
		R _L = 4Ω, P _O = 1.6W, f = 1kHz	—	0.029	—	
PSRR	Power-Supply Ripple Rejection	Input AC-GND, f = 1kHz, V _{ripple} = 200mVpp	—	-60	—	dB
CS	Channel Separation	P _O = 1W, f = 1kHz	—	-105	—	Db
η	Efficiency	P _O = 1.7W x 2ch, f = 1kHz, R _L = 8Ω	—	92	—	%
		P _O = 3W x 2ch, f = 1kHz, R _L = 4Ω	—	90	—	
V _N	Noise	Max Gain, A-Weighting, SSM OFF	—	40	—	μV
		Max Gain, A-Weighting, SSM ON	—	48	—	
SNR	Signal Noise Ratio	f = 20 to 20kHz, THD = 1%	—	-97	—	dB
Headphone Mode						
V _{OS}	Output Offset Voltage	No Load	—	2.5	—	V
P _O	Output Power	V _{DD} = 5V, THD+N = 1%, R _L = 32Ω, f = 1kHz	—	66	—	mW
		V _{DD} = 5.8V, THD+N = 1%, R _L = 32Ω, f = 1kHz	—	88	—	
THD+N	Total Harmonic Distortion Plus Noise	V _{DD} = 5V, R _L = 32Ω, P _O = 50mW, f = 1kHz	—	0.024	—	%
PSRR	Power-Supply Ripple Rejection	Input AC-GND, f = 1kHz, V _{ripple} = 200mVpp	—	-66	—	dB
CS	Channel Separation	P _O = 1W, f = 1kHz	—	-89	—	dB
V _n	Noise	Input AC-GND, A-Weighting	—	15	—	μV
SNR	Signal Noise Ratio	f = 20 to 20kHz, THD = 1%	—	-98.2	—	dB
Control Section						
V _{IH}	EN/Mute/SSM Input High	—	1.4	—	—	V
V _{IL}	EN/Mute/SSM Input Low	—	—	—	0.5	V
OTP	Overtemperature Protection	—	—	+150	—	°C
OTH	Overtemperature Hysteresis	—	—	+30	—	°C

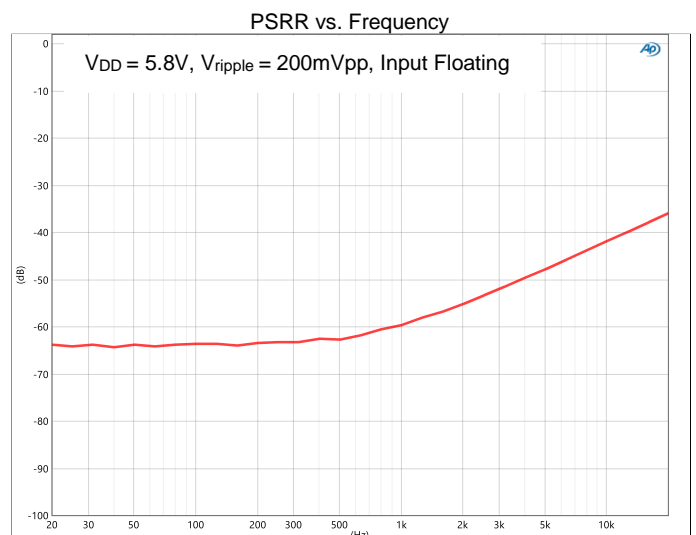
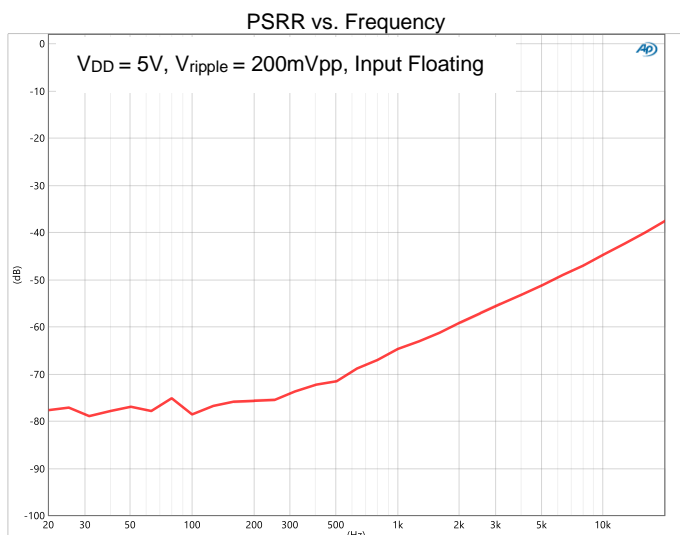
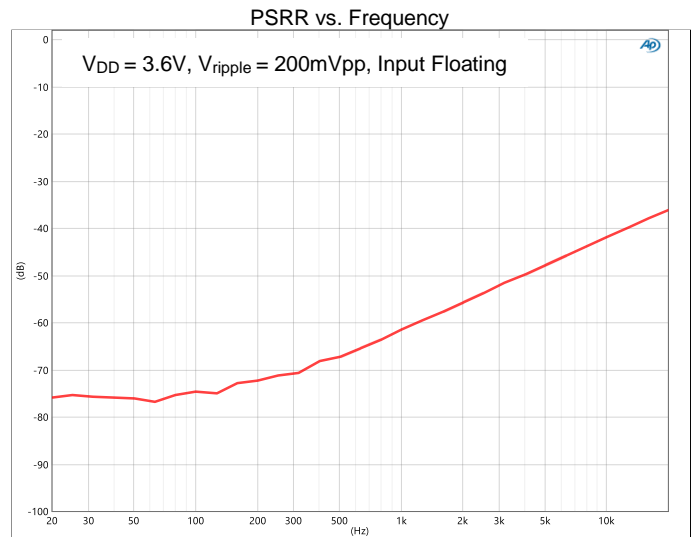
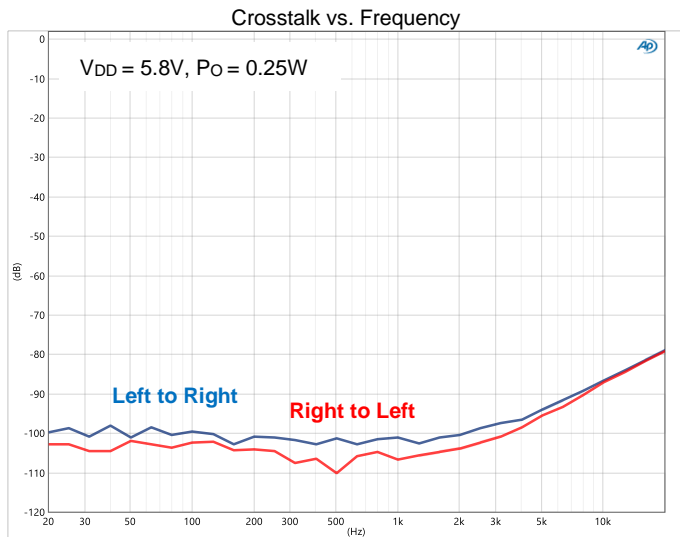
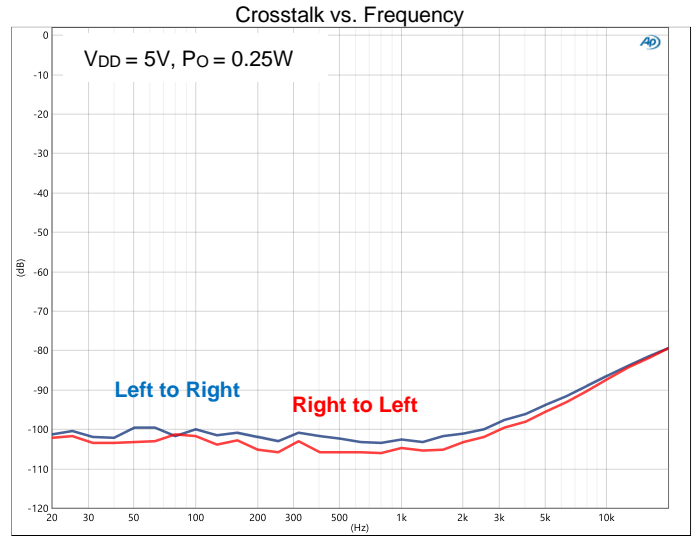
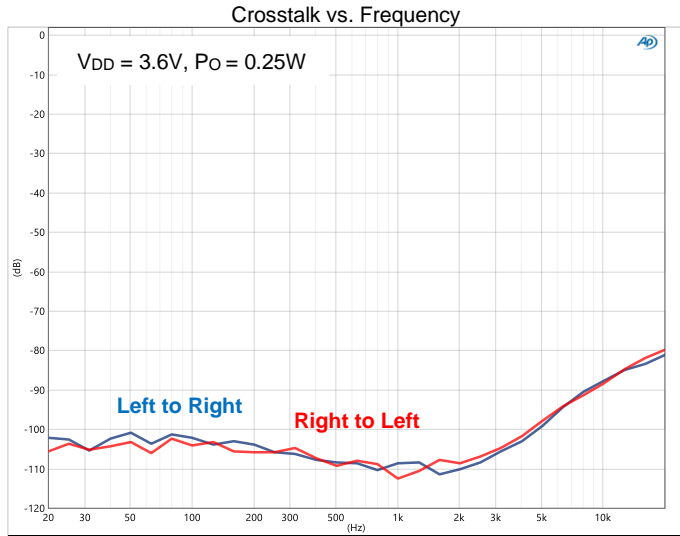
Typical Performance Characteristics

Speaker Mode, Max Gain = 20dB, $R_L = 4\Omega$, with AUX-0025 + AES-17 (20kHz) Filter



Typical Performance Characteristics (continued)

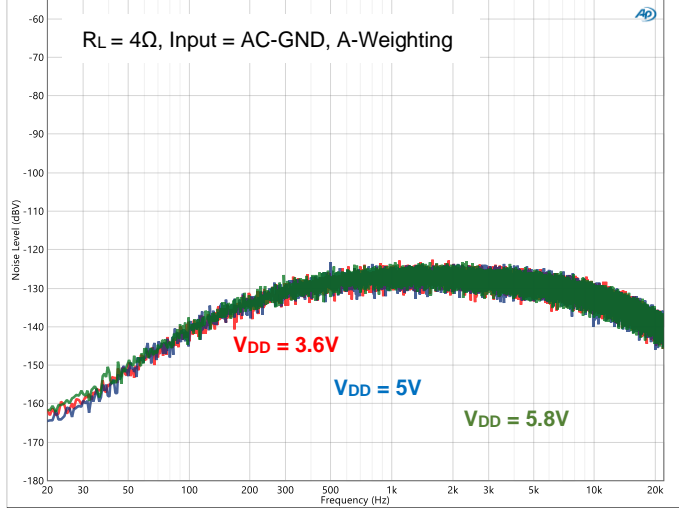
Speaker Mode, Max Gain = 20dB, $R_L = 4\Omega$, with AUX-0025 + AES-17 (20kHz) Filter



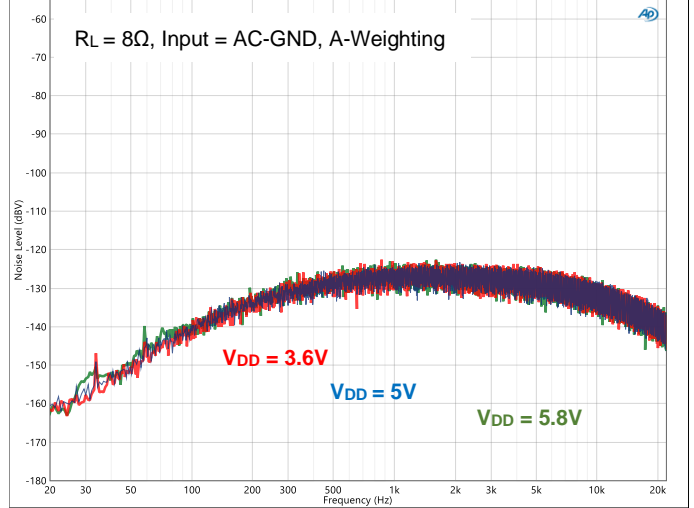
Typical Performance Characteristics (continued)

Speaker Mode, Max Gain = 20dB, $R_L = 4\Omega$, SSM = OFF, with AUX-0025 + AES-17 (20kHz) Filter

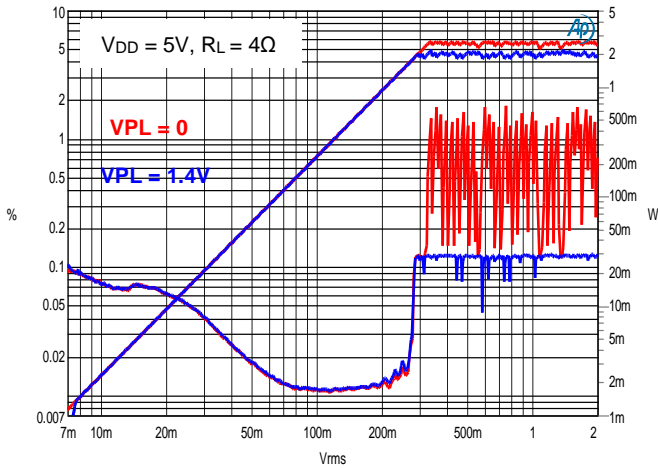
Output Noise vs. Frequency



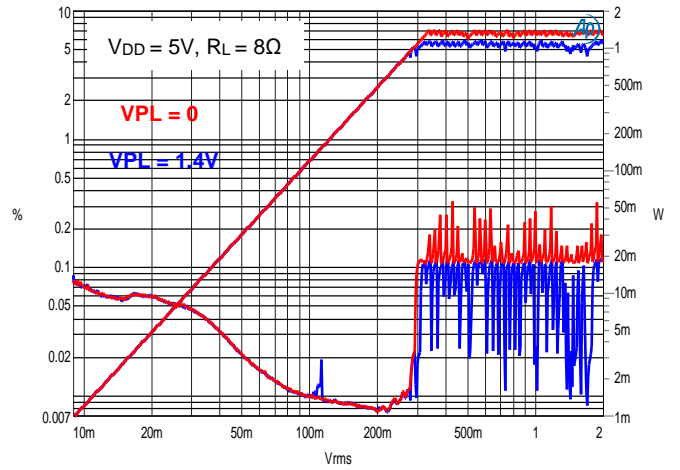
Output Noise vs. Frequency



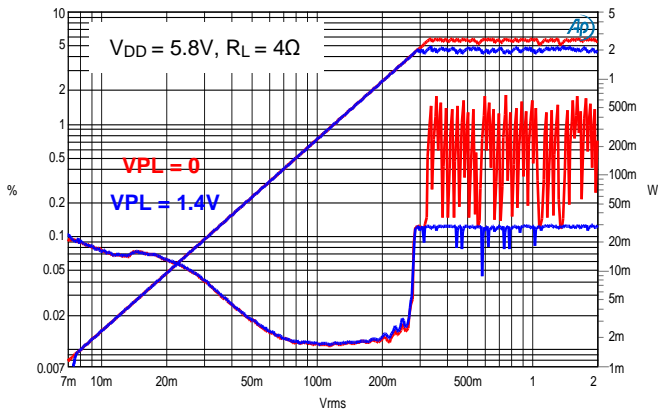
Power Limit



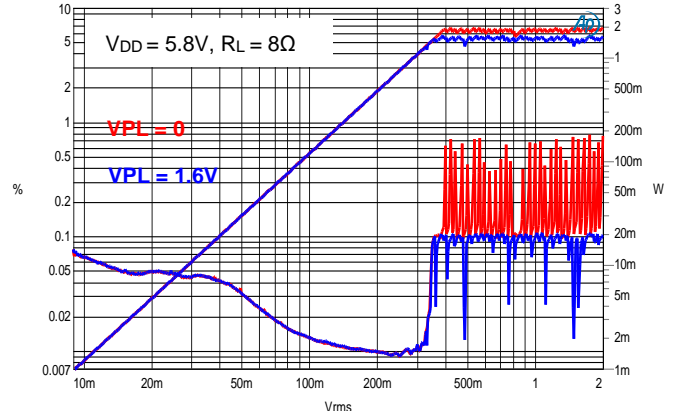
Power Limit



Power Limit



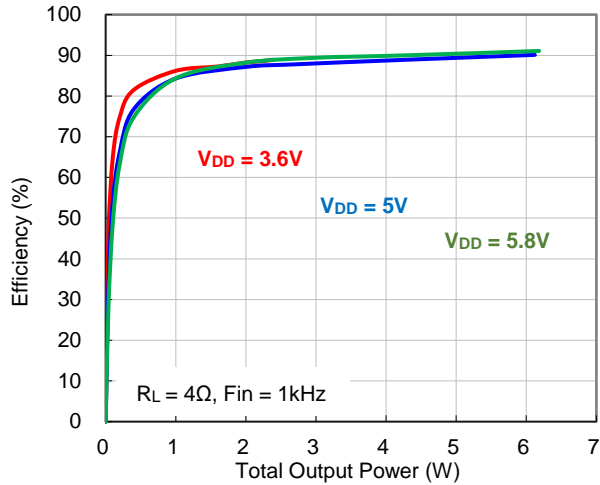
Power Limit



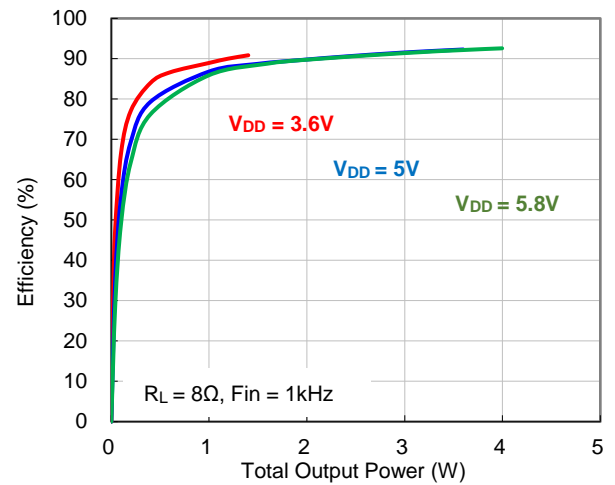
Typical Performance Characteristics (continued)

Speaker Mode, Max Gain = 20dB, $R_L = 4\Omega$, with AUX-0025 + AES-17 (20kHz) Filter

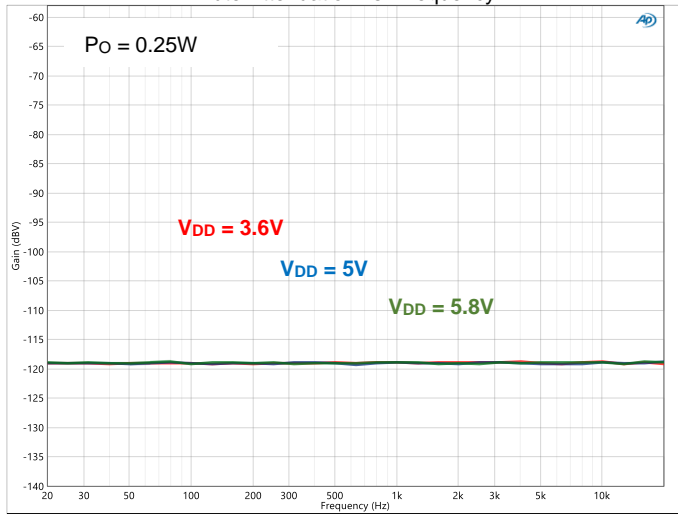
Efficiency vs. Output Power



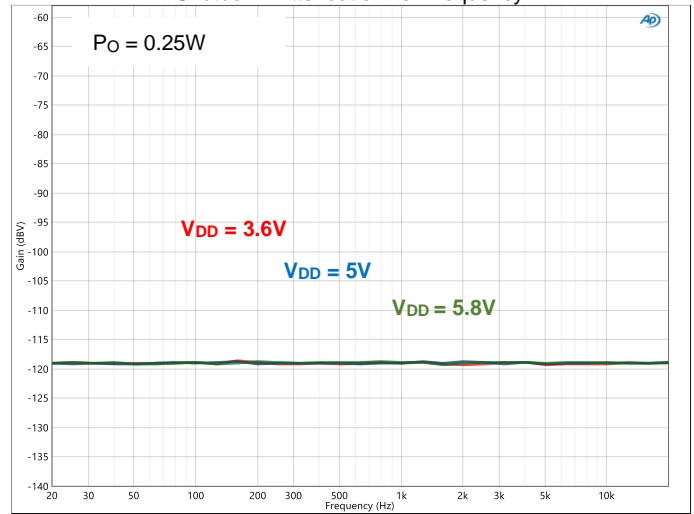
Efficiency vs. Output Power



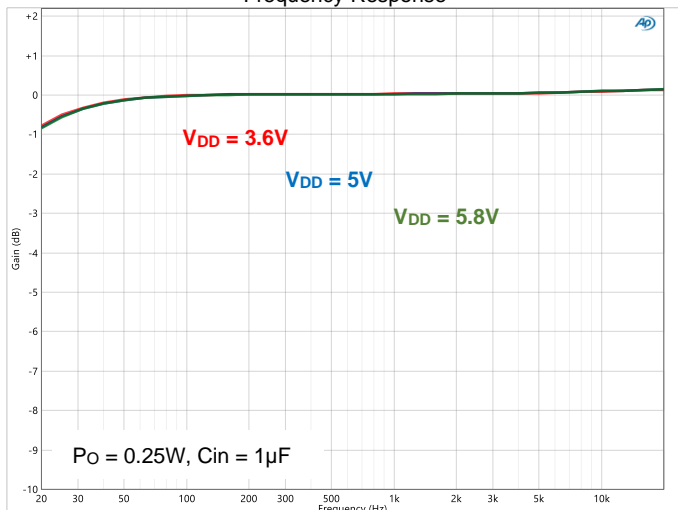
Mute Attenuation vs. Frequency



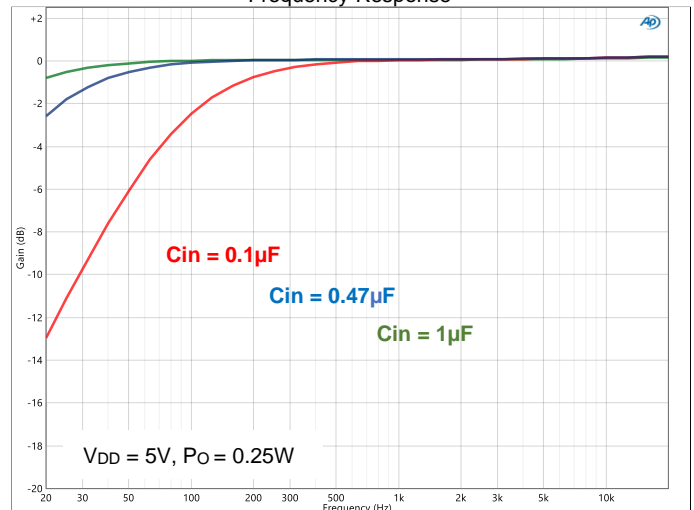
Shutdown Attenuation vs. Frequency



Frequency Response



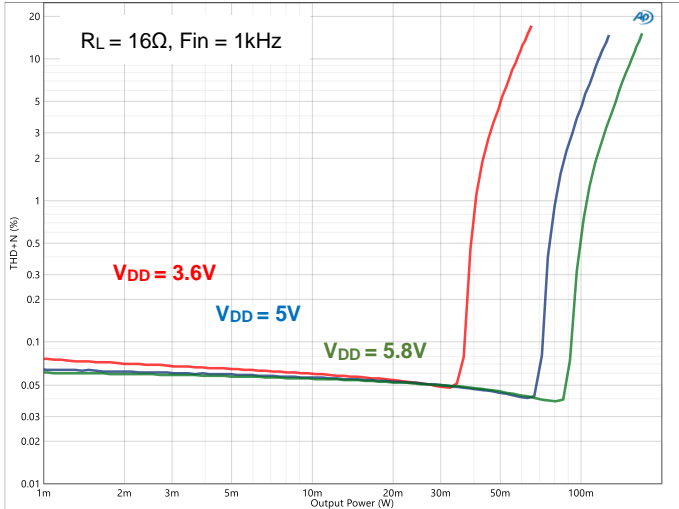
Frequency Response



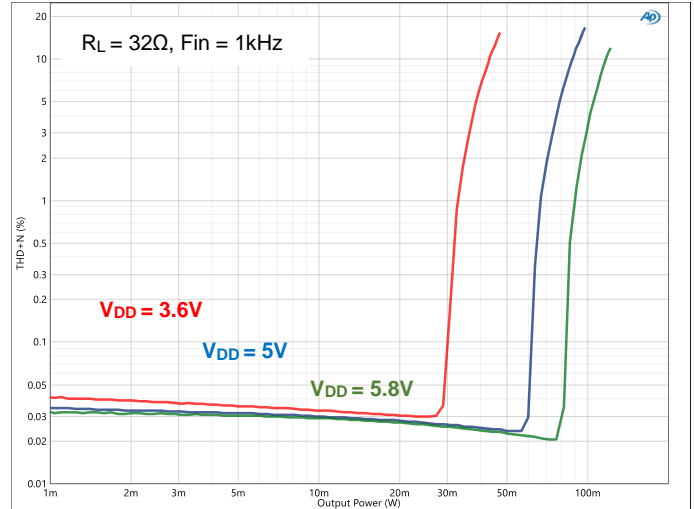
Typical Performance Characteristics (continued)

Headphone Mode, Max Gain = 3.5dB, $R_L = 32\Omega$, with AES-17 (20kHz) Filter

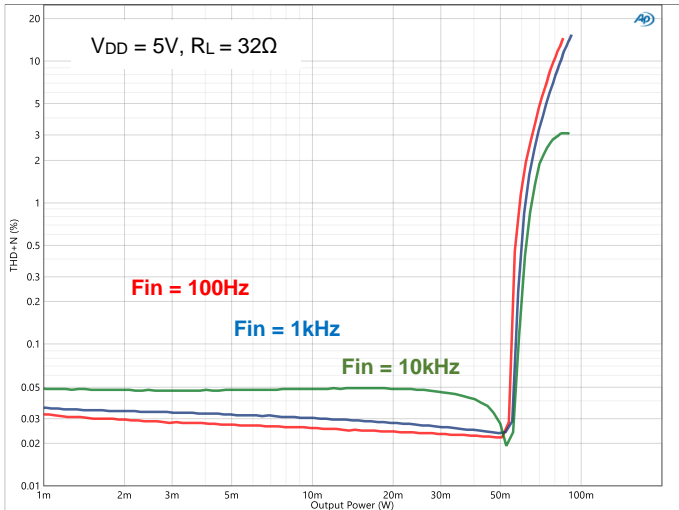
THD+N vs. Output Power



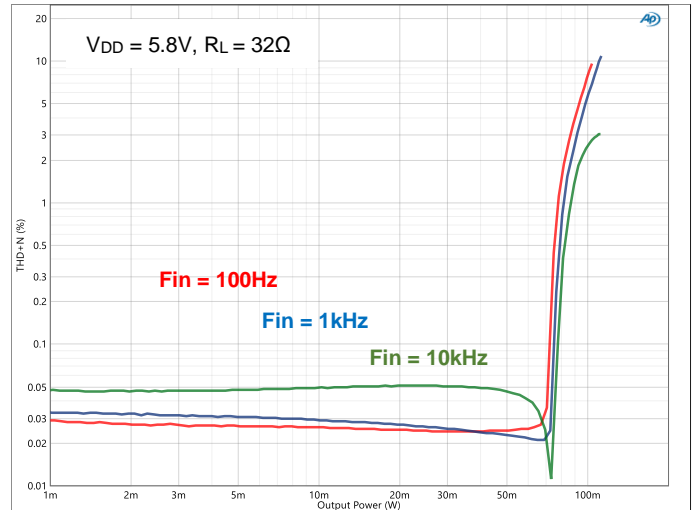
THD+N vs. Output Power



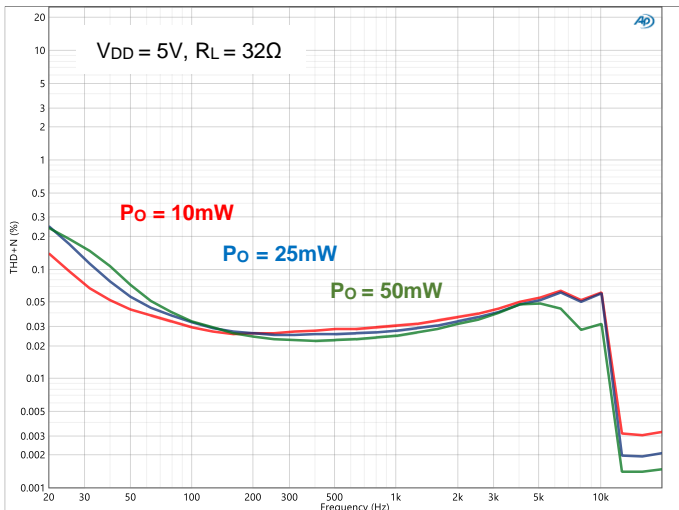
THD+N vs. Output Power



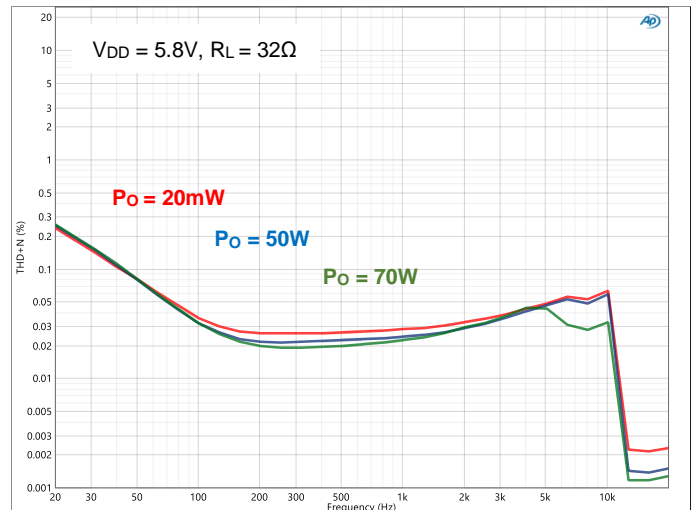
THD+N vs. Output Power



THD+N vs. Frequency

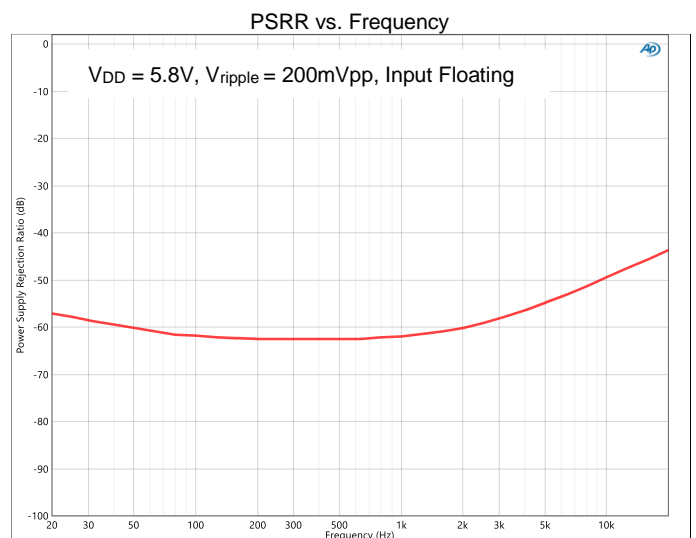
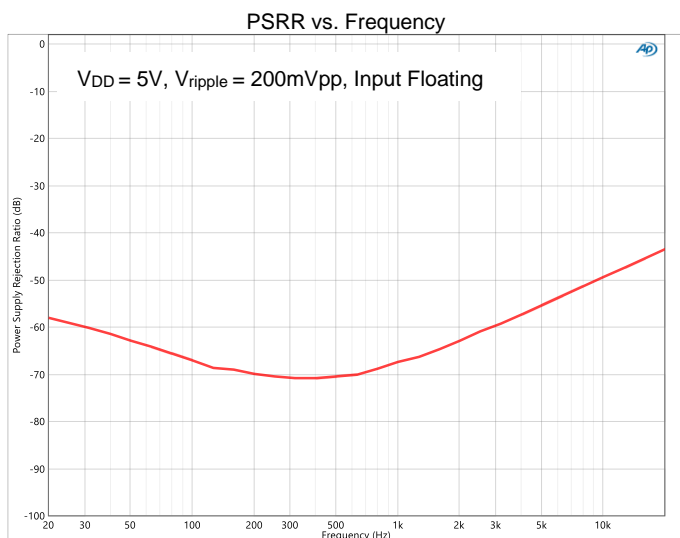
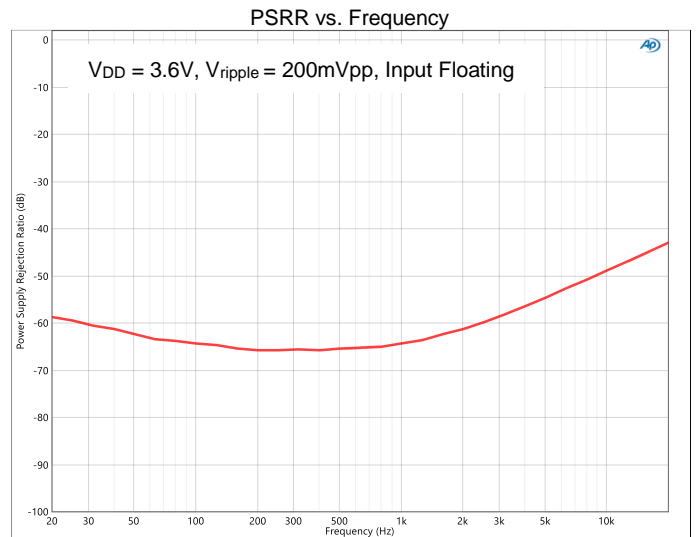
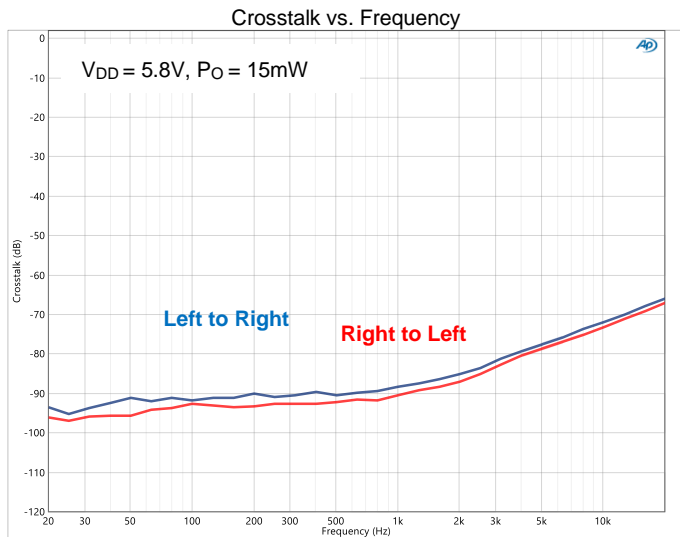
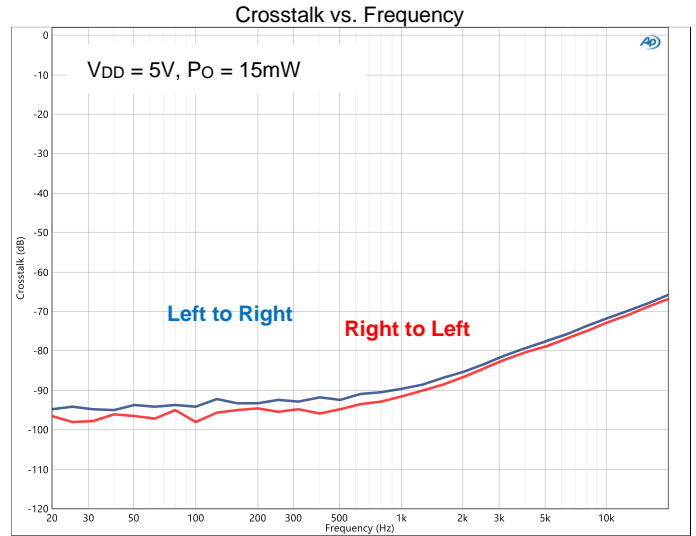
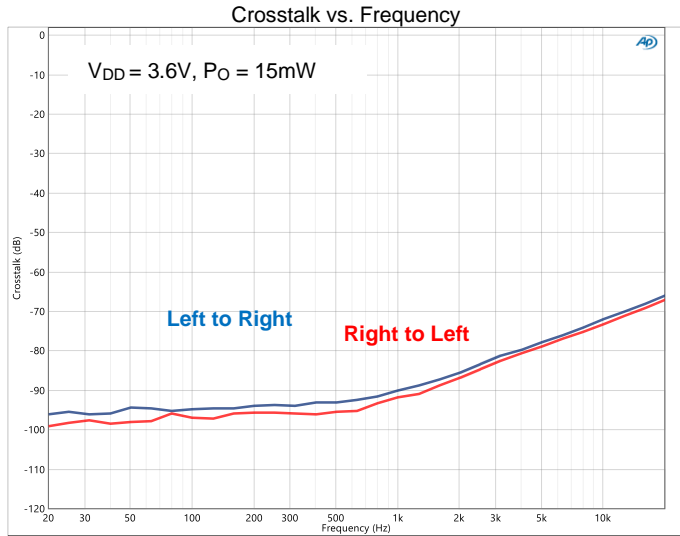


THD+N vs. Frequency



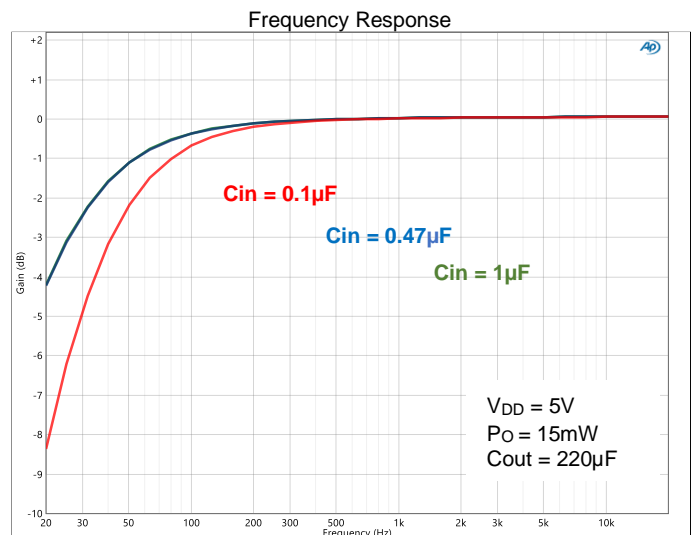
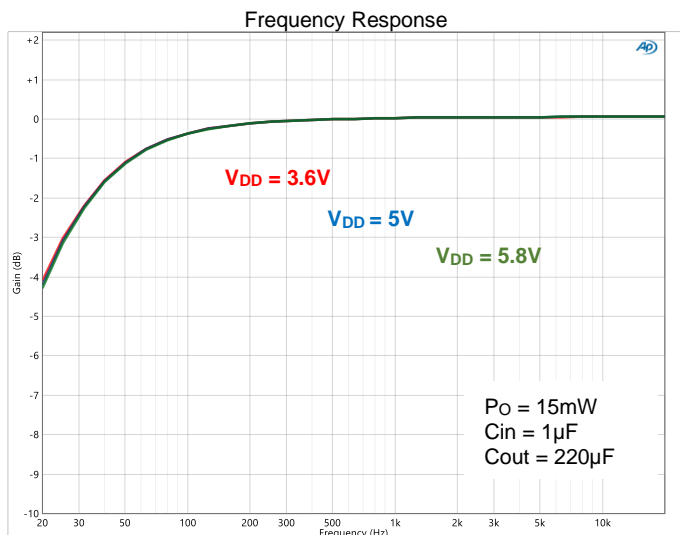
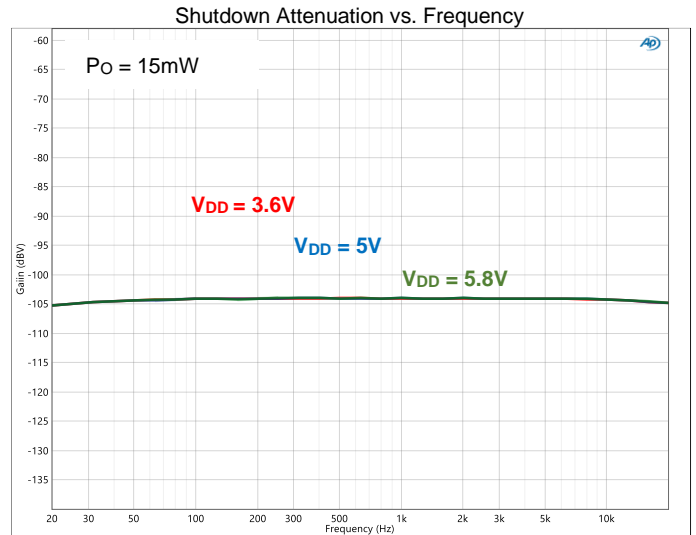
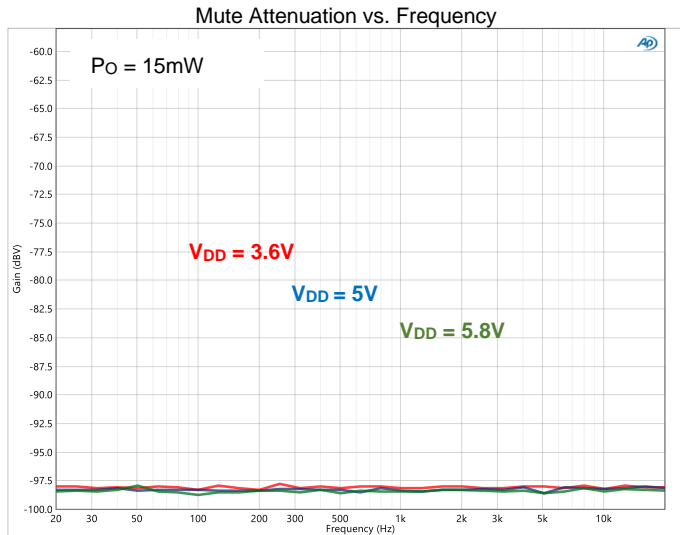
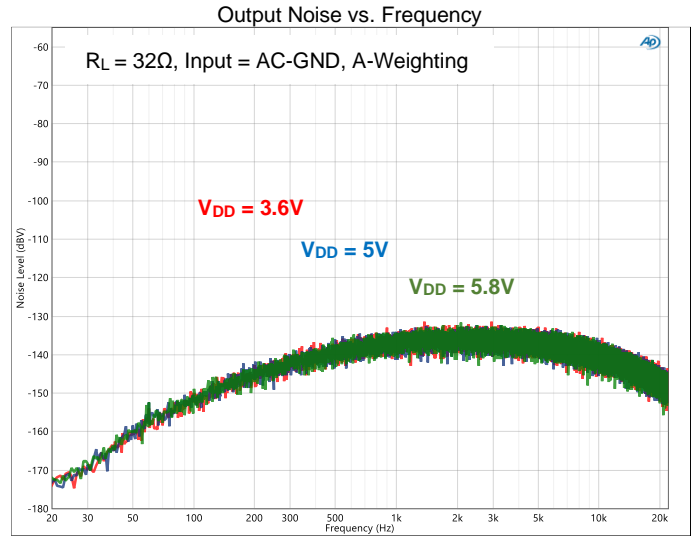
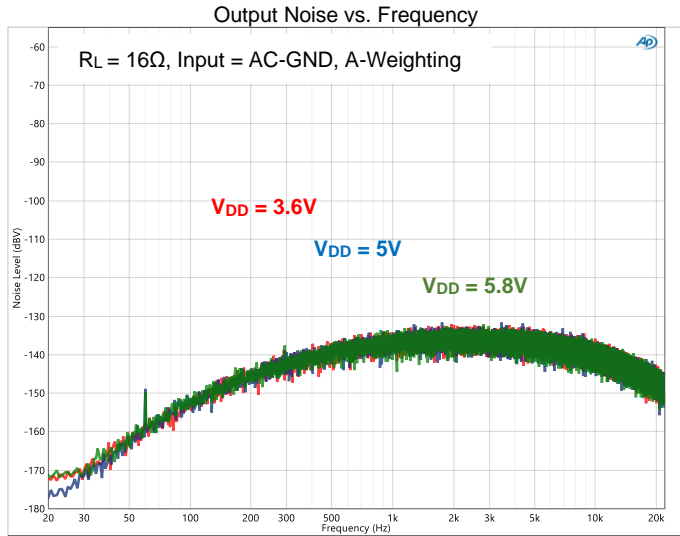
Typical Performance Characteristics (continued)

Headphone Mode, Max Gain = 3.5dB, $R_L = 32\Omega$, with AES-17 (20kHz) Filter



Typical Performance Characteristics (continued)

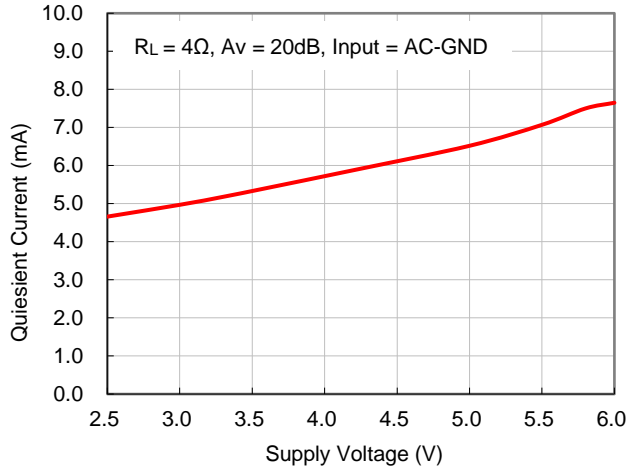
Headphone Mode, Max Gain = 3.5dB, $R_L = 32\Omega$, with AES-17 (20kHz) Filter



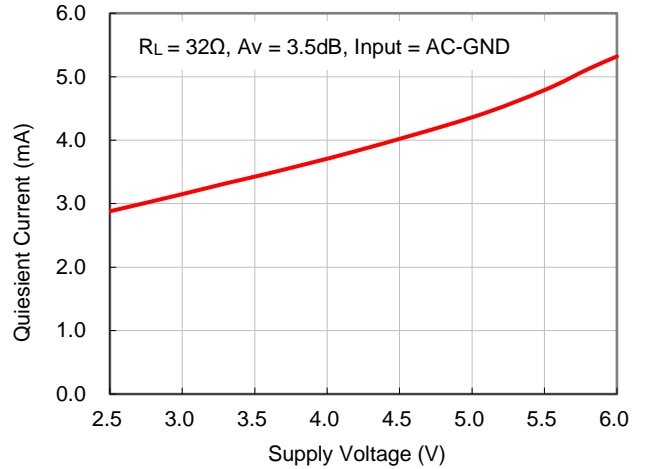
Typical Performance Characteristics (continued)

Others, Max Gain, $R_L = 4\Omega$

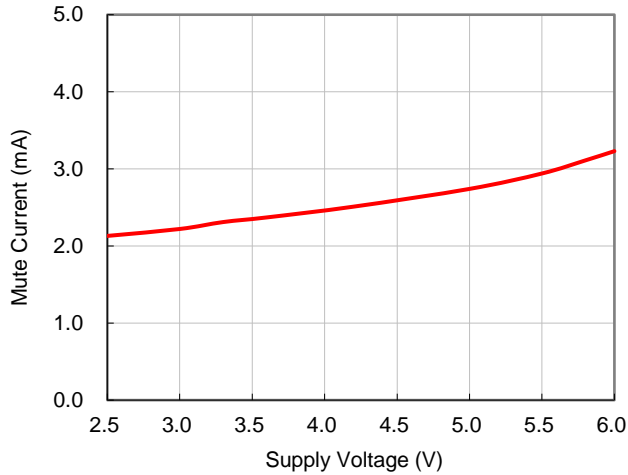
Quiescent Current vs. Supply Voltage



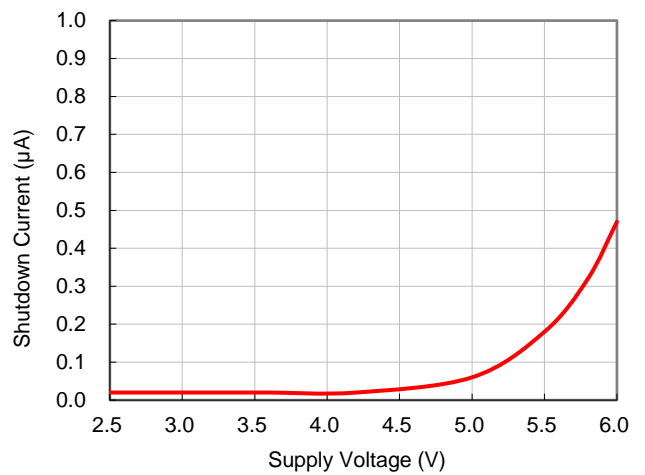
Quiescent Current vs. Supply Voltage



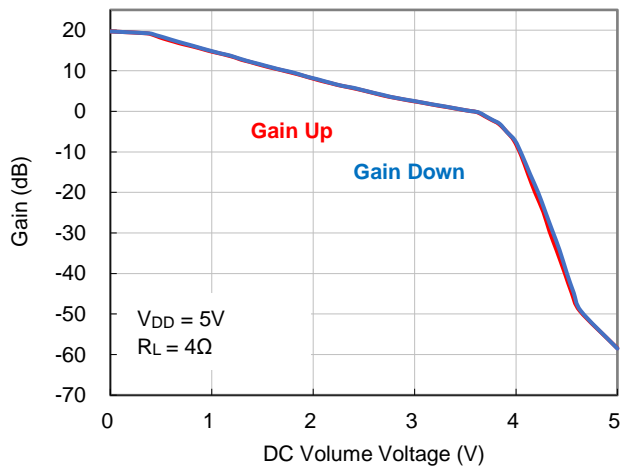
Mute Current vs. Supply Voltage



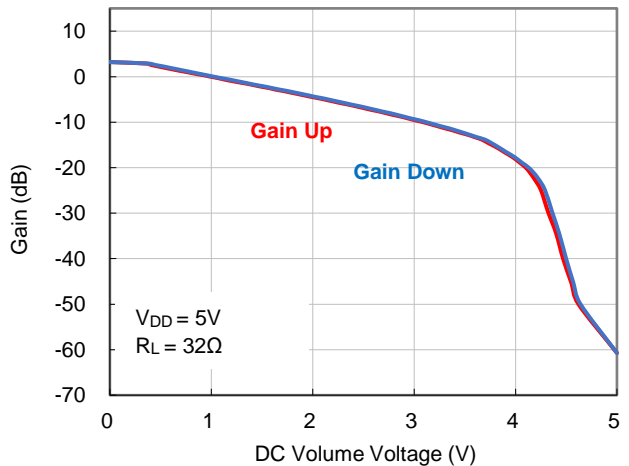
Shutdown Current vs. Supply Voltage



Speaker Gain vs. Volume Voltage



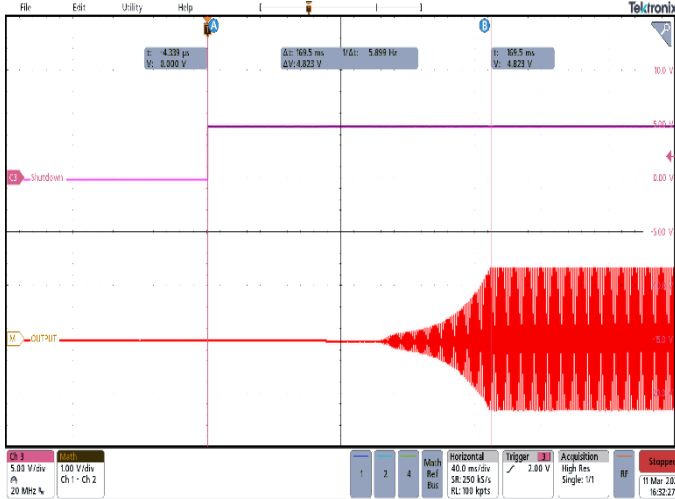
Headphone Gain vs. Volume Voltage



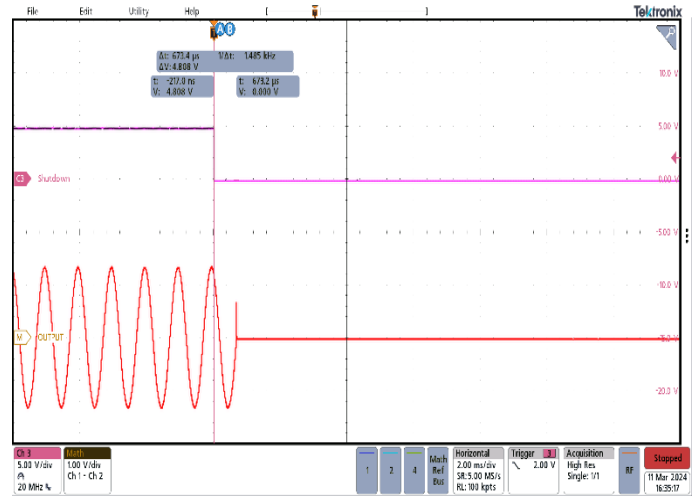
Typical Performance Characteristics (continued)

Others, Max Gain, $R_L = 4\Omega$

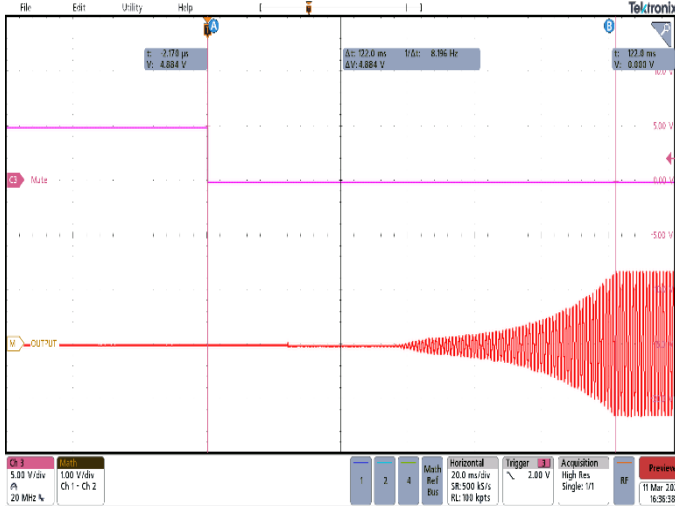
Startup from Shutdown



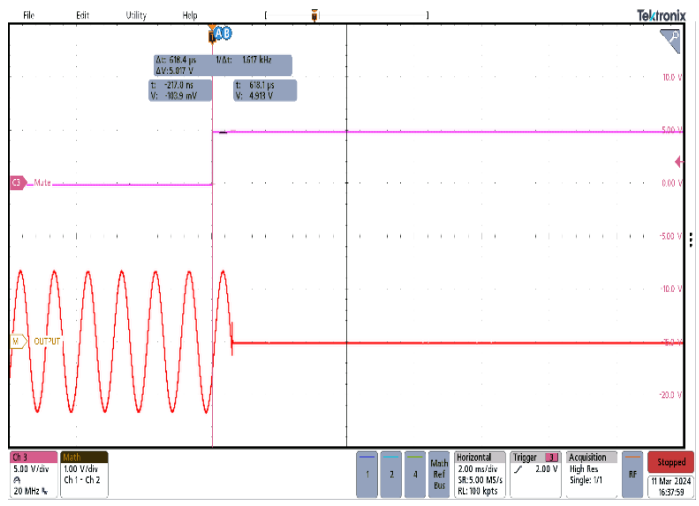
Shutdown



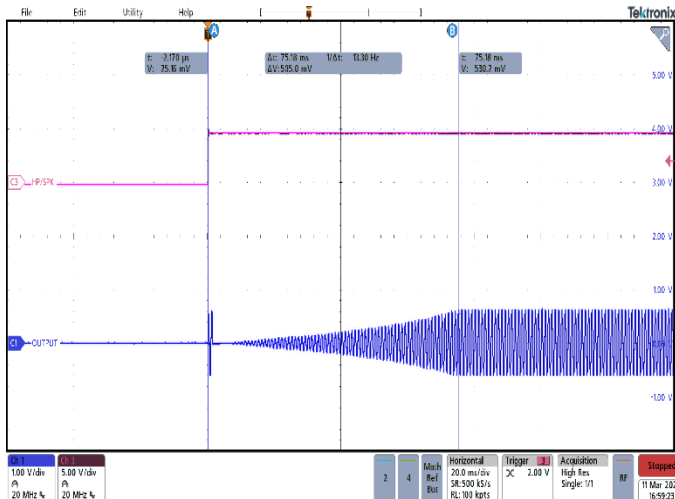
Startup from Mute



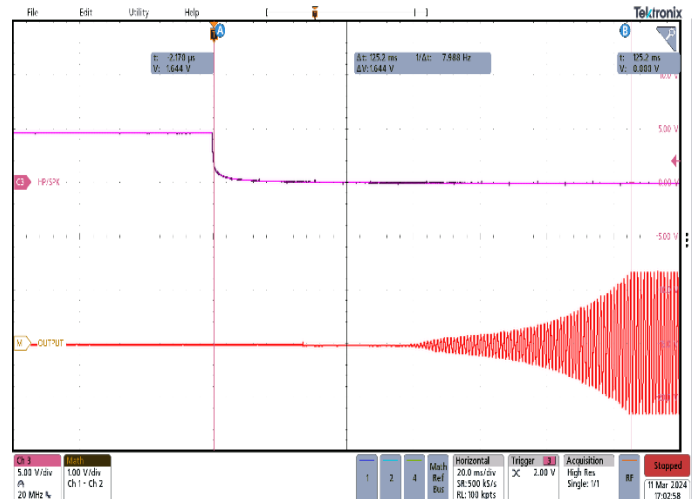
Mute



Speaker Switch to HP

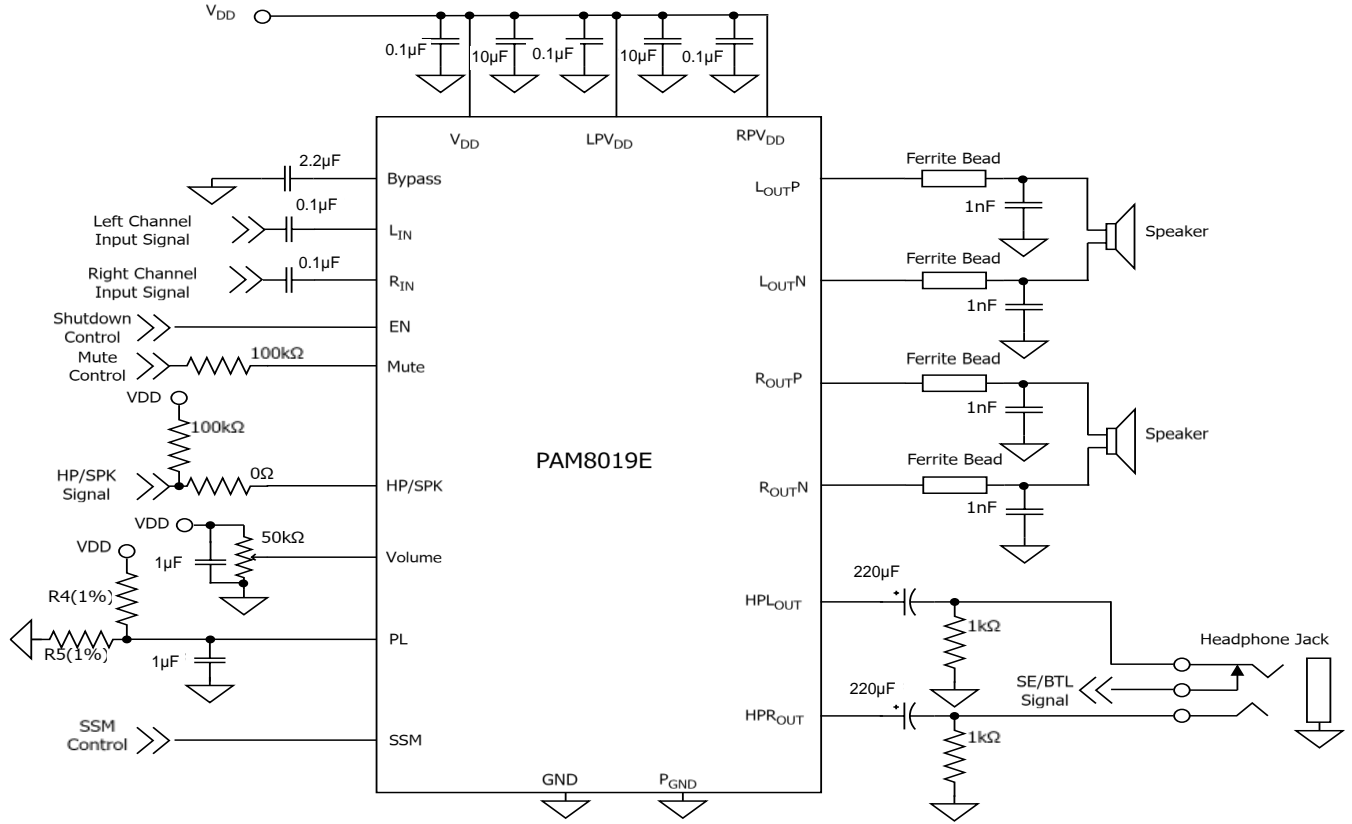


HP Switch to Speaker



Application Information

Typical Application Circuit of PAM8019E



DC Volume Control Table (DC Volume Voltage is Set as a Percentage of the V_{DD} Voltage)

Step	SPK Gain (dB)	HP Gain (dB)	Volume L-->H %V _{DD}	Volume H-->L % V _{DD}	Recommend (%V _{DD})	Recommend at V _{DD} = 5V (V)	Recommend at V _{DD} = 5.8V (V)
1	19.69	3.21	0.0%	6.2%	0.0%	0.000	0.000
2	19.22	2.88	7.2%	7.6%	7.4%	0.370	0.429
3	18.77	2.56	8.6%	9.0%	8.8%	0.440	0.510
4	18.20	2.23	9.8%	10.6%	10.2%	0.510	0.592
5	17.66	1.91	11.2%	12.0%	11.6%	0.580	0.673
6	17.15	1.59	12.6%	13.4%	13.0%	0.650	0.754
7	16.65	1.28	14.0%	14.8%	14.4%	0.720	0.835
8	16.18	0.96	15.6%	16.2%	15.9%	0.795	0.922
9	15.67	0.64	17.2%	17.6%	17.4%	0.870	1.009
10	15.18	0.33	18.6%	19.0%	18.8%	0.940	1.090
11	14.71	0.01	20.0%	20.4%	20.2%	1.010	1.172
12	14.26	-0.29	21.6%	21.8%	21.7%	1.085	1.259
13	13.82	-0.64	23.0%	23.4%	23.2%	1.160	1.346
14	13.26	-0.95	24.6%	24.8%	24.7%	1.235	1.433
15	12.72	-1.24	25.8%	26.2%	26.0%	1.300	1.508
16	12.21	-1.55	27.4%	27.6%	27.5%	1.375	1.595

DC Volume Control Table (DC Volume Voltage is Set as a Percentage of the V_{DD} Voltage) (continued)

17	11.71	-1.87	28.8%	29.0%	28.9%	1.445	1.676
18	11.23	-2.19	30.2%	30.6%	30.4%	1.520	1.763
19	10.77	-2.51	31.6%	32.0%	31.8%	1.590	1.844
20	10.31	-2.83	33.2%	33.4%	33.3%	1.665	1.931
21	9.87	-3.15	34.6%	35.0%	34.8%	1.740	2.018
22	9.44	-3.48	36.0%	36.4%	36.2%	1.810	2.100
23	8.91	-3.80	37.6%	37.8%	37.7%	1.885	2.187
24	8.40	-4.13	39.0%	39.2%	39.1%	1.955	2.268
25	7.91	-4.46	40.4%	40.6%	40.5%	2.025	2.349
26	7.43	-4.80	41.8%	42.2%	42.0%	2.100	2.436
27	6.95	-5.14	43.4%	43.6%	43.5%	2.175	2.523
28	6.49	-5.49	44.8%	45.0%	44.9%	2.245	2.604
29	6.13	-5.83	46.2%	46.4%	46.3%	2.315	2.685
30	5.77	-6.18	47.6%	47.8%	47.7%	2.385	2.767
31	5.33	-6.53	49.2%	49.4%	49.3%	2.465	2.859
32	4.90	-6.89	50.6%	50.8%	50.7%	2.535	2.941
33	4.47	-7.26	52.0%	52.2%	52.1%	2.605	3.022
34	4.02	-7.63	53.4%	53.6%	53.5%	2.675	3.103
35	3.58	-8.01	55.0%	55.2%	55.1%	2.755	3.196
36	3.25	-8.39	56.4%	56.6%	56.5%	2.825	3.277
37	2.92	-8.78	57.8%	58.0%	57.9%	2.895	3.358
38	2.60	-9.18	59.2%	59.4%	59.3%	2.965	3.439
39	2.28	-9.59	60.8%	61.0%	60.9%	3.045	3.532
40	1.96	-10.01	62.2%	62.4%	62.3%	3.115	3.613
41	1.64	-10.44	63.6%	63.8%	63.7%	3.185	3.695
42	1.32	-10.88	65.0%	65.2%	65.1%	3.255	3.776
43	1.01	-11.33	66.6%	66.8%	66.7%	3.335	3.869
44	0.69	-11.80	68.0%	68.2%	68.1%	3.405	3.950
45	0.38	-12.29	69.4%	69.6%	69.5%	3.475	4.031
46	0.06	-12.78	71.0%	71.0%	71.0%	3.550	4.118
47	-0.25	-13.31	72.4%	72.4%	72.4%	3.620	4.199
48	-1.19	-13.85	73.8%	74.0%	73.9%	3.695	4.286
49	-2.14	-14.70	75.2%	75.4%	75.3%	3.765	4.367
50	-3.10	-15.62	76.6%	76.8%	76.7%	3.835	4.449
51	-5.09	-16.60	78.2%	78.2%	78.2%	3.910	4.536
52	-7.21	-17.67	79.6%	79.8%	79.7%	3.985	4.623
53	-10.82	-18.86	81.0%	81.2%	81.1%	4.055	4.704
54	-15.55	-20.20	82.4%	82.8%	82.6%	4.130	4.791
55	-20.12	-22.28	83.8%	84.4%	84.1%	4.205	4.878
56	-24.83	-24.92	85.4%	85.8%	85.6%	4.280	4.965
57	-29.55	-29.67	86.6%	87.2%	86.9%	4.345	5.040
58	-34.24	-34.42	88.0%	88.6%	88.3%	4.415	5.121
59	-39.80	-40.08	89.6%	90.0%	89.8%	4.490	5.208
60	-44.81	-45.28	91.0%	91.4%	91.2%	4.560	5.290
61	-49.23	-49.98	92.6%	92.8%	92.7%	4.635	5.377
62	-58.45	-60.72	94.0%	100.0%	100.0%	5.000	5.800

Application Information (continued)

Non-Clip Power Limit (NCPL) Function

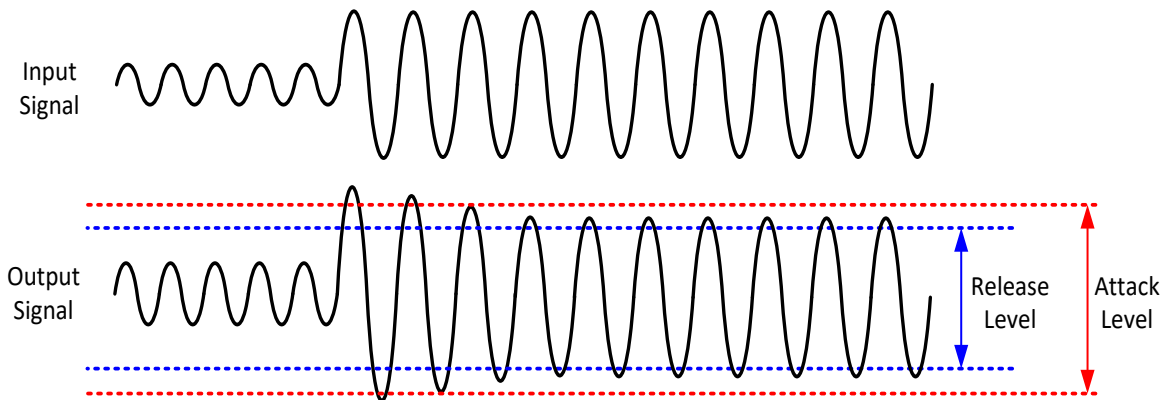
When the output reaches the maximum power setting value, the PAM8019E NCPL circuits will regulate the gain to prevent the output waveform from clipping and help to preventing speaker damaged, while maintaining maxmized audio performance. The PL pin is used to set up the NCPL function.

NCPL Setting Threshold vs. Output Power Rating

NCPL Function	Output Power
V_{DD} to $V_{DD} \times 0.45$ or PL pin floating	NCPL function disabled
$V_{DD} \times 0.45$ to $V_{DD} \times 0.27$	$P_O = [[8(1/2V_{DD}-V_{PL})^2]/R_L] \times 0.95$
$V_{DD} \times 0.27$ to GND	$P_O = 2.5W$ ($V_{DD} = 5V, R_L = 4\Omega$) $P_O = 3.5W$ ($V_{DD} = 5.8V, R_L = 4\Omega$) $P_O = 1.3W$ ($V_{DD} = 5V, R_L = 8\Omega$) $P_O = 1.8W$ ($V_{DD} = 5.8V, R_L = 8\Omega$)

If instantaneous output power exceeds the defined PL value, the PAM8019E will trigger an attack cycle. Eventually, this begins the process for the PAM8019E’s internal amplifier gain stepping down at 0.5dB steps for every attack cycle. The gain is regulated with successive attack cycles until the output power drops to the value defined by the PL pin setting

Adjusting the amplifier’s closed-loop gain to control the output power can result in an extremely smooth control; it could prevent harsh sounds due to potential saturation condition. This type of control also avoids the output signal from being clipped, thus providing a much pleasant listening experience. The figure bellow illustrates PAM8019E operation under the non-clip power limit attack cycle. The attack time for power limit is set to 50µs, while release time set to 340ms.



The Attack and Release illustration for Non-Clip Power Limit Operation

Mute Operation

The Mute pin is an input to control the Class-D/HP output state of the PAM8019E. A logic low on this pin enables the outputs and logic high on this pin disables the outputs. This pin can be used to quickly disable or enable the outputs without a volume fade. The quiescent current is listed in the electrical characteristic table.

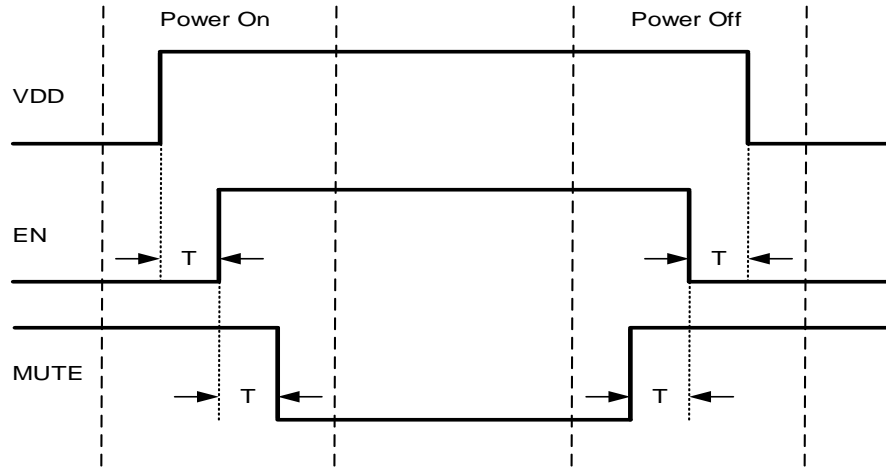
Shutdown Operation

In order to reduce power consumption while not in use, the PAM8019E is designed shutdown circuit to turn off the amplifier’s bias circuit. The amplifier can be turned off when logic low is placed on the EN pin. When switching the EN pin to low level, the amplifier enters a low-consumption current status.

Application Information (continued)

Power On and Power Off Sequence

This sequence is used to provide pop-noise-minimized operation during PAM8019E's power on/off POP cycle. After V_{DD} is ready, the EN pin can be pulled high with VOLUME set to desired level. Then Un-Mute it for pop free start up. To shut down PAM8019E, the recommended operation is to tune down VOLUME to V_{DD} and then mute the channel. After a period of time ($t = 0.1\text{sec}$ for example), the PAM8019E can be shut down with V_{DD} ramp down. The figure below illustrates the power on/off sequences described.



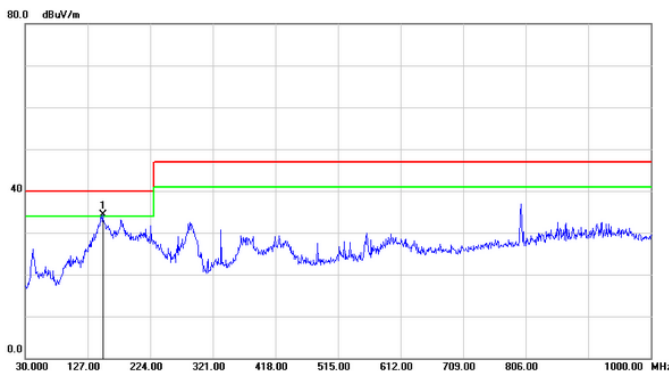
Suggested Sequences for Power On and Power Off Operation

Before the power on, make sure the speakers are good connect, if the speaker not good connects like open or short, the chip will detect and enter a protection mode, the MUTE pin will be set as a high-level signal which can report to MCU. After the speakers good connect, restart the EN single and the chip will normally working.

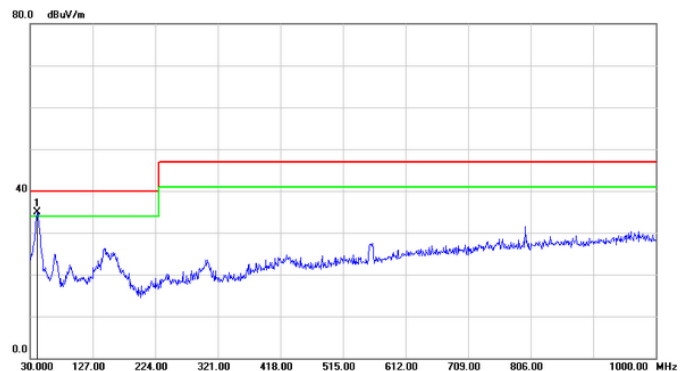
Spread Spectrum Modulation (SSM)

The PAM8019E features spread spectrum modulation, which randomizes the oscillator frequency to improve EMI performance. PAM8019E SSM design is center-spread with $\pm 11\%$ modulation. With SSM enabled, the EMI specification can be achieved with inexpensive ferrite bead filters rather than bulky low-pass LC filters at the audio output. Connect SSM pin to a voltage above V_{IH} (1.4V) to disable SSM, or below V_{IL} (0.5V) to enable it. This pin is compliant to V_{DD} .

The PAM8019E EVM passes FCC Class B standard with a ferrite bead filter using 30cm long twisted-pair wires for 4Ω speakers and operating at $V_{DD} = 5V$, $P_O = 2x2W$. Only a low-cost ferrite bead filter is required for most applications. Select the ferrite bead type and size based on the application. A 600Ω@100MHz ferrite bead with a 1nF bypass capacitor is recommended. Put the filter close to the output pins. The figure below illustrates the radiated emissions results by PAM8019E EVB.



Radiated Emission - Horizontal



Radiated Emission - Vertical

Application Information (continued)

Power Supply Decoupling

The PAM8019E is a high-performance CMOS audio-amplifier design that requires adequate power supply decoupling to ensure the optimized THD and PSRR performance. The Power supply decoupling also prevents oscillation as caused by long leads between the amplifier and the speaker. The optimum decoupling is achieved by using two capacitors of different types that target different types of noise on the power supply leads. A good low-equivalent-series-resistance (ESR) ceramic-capacitor (typically 0.1μF) is recommended to be placed as close as possible to the V_{DD} pin. It could assist to filter out the higher frequency transients, spikes or digital hash on the line. To filter out lower-frequency noise signals, a large capacitor (typical 10μF or greater) should be placed near the audio amplifier. When design PAM8019E system board, adding an electrolytic-capacitor (such as 220μF) can help maintaining a stable power supply voltage.

Make sure the power supply capacitor be placed after the via which should be close to the pin terminal and the same layer with PAM8019E.

Input Capacitor (C_i)

It is desirable to use a large input capacitor but in applications where the speaker lacks the ability to reproduce signals below 100Hz to 150Hz, it is feasible to minimize C_i without affecting overall system performance. The input capacitor (C_i) and input resistance (R_i) of the amplifier could form a high-pass filter with the corner frequency as determined by equation below:

$$F_c = 1/2\pi R_i \times C_i$$

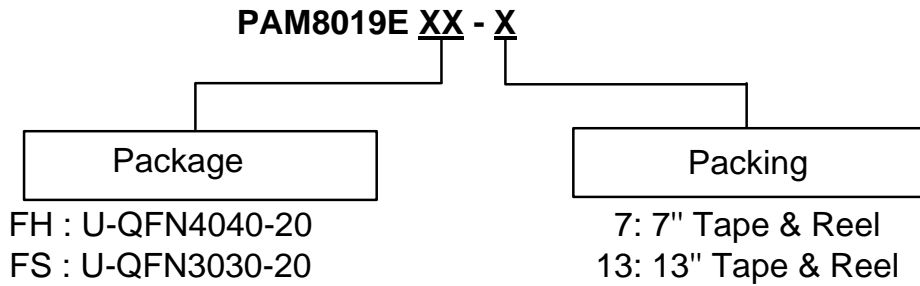
Considering the system cost and board/component size, the click and pop performance is usually affected by the size of the input coupling capacitor C_i. A larger in/out coupling capacitor requires more charge to reach its quiescent DC voltage (Normally 1/2 V_{DD}). This charge comes from the internal circuit via the feedback and is apt to create pops upon device enabling. Minimizing the capacitor size based on necessary low frequency response, turn on pop can be minimized. A ceramic Input capacitor (C_i) of 0.1μF is recommended for the best click and pop performance.

Bypass Capacitor (C_{BYP})

Bypass Capacitor (C_{BYP}) is the most critical capacitor and serves several important functions for any sound quality critical design. During startup or recovery stage from shutdown mode, the C_{BYP} determines the rate at which the amplifier starts up. The second function is to reduce noise as produced by the power supply by output signal coupling. Such noise will potentially impact the internal analog reference to the amplifier and appears with degraded PSRR and THD+N.

A ceramic bypass capacitor (C_{BYP}) of 2.2μF is recommended for the best THD and noise performance. Increasing the bypass capacitor reduces clicking and popping noise from power on/off and when entering and exiting the shutdown mode.

Ordering Information

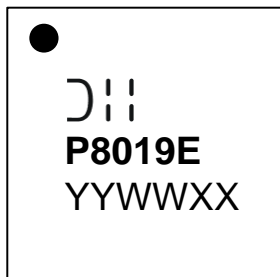


Part Number	Package Code	Package	Packing	
			Qty.	Carrier
PAM8019EFS-7	FS	U-QFN3030-20	1500	7" Tape & Reel
PAM8019EFH-13	FH	U-QFN4040-20	3000	13" Tape & Reel

Marking Information

U-QFN4040-20/U-QFN3030-20

(Top View)



Logo :

Marking : P8019E

YY : Year : 24, 25, 26~

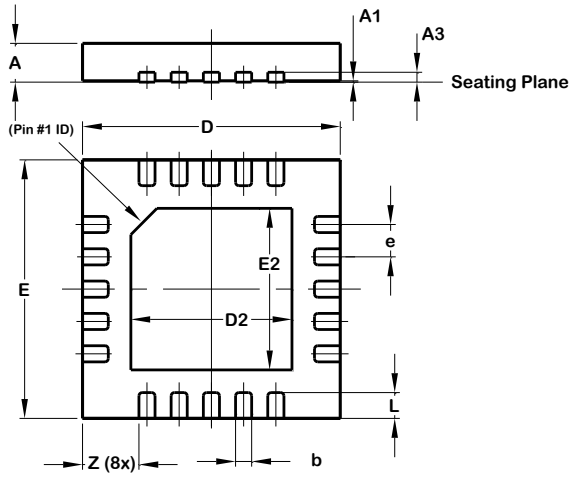
WW : Week : 01~52; 52
 represents 52 and 53 week

XX : Internal Code

Package Outline Dimensions

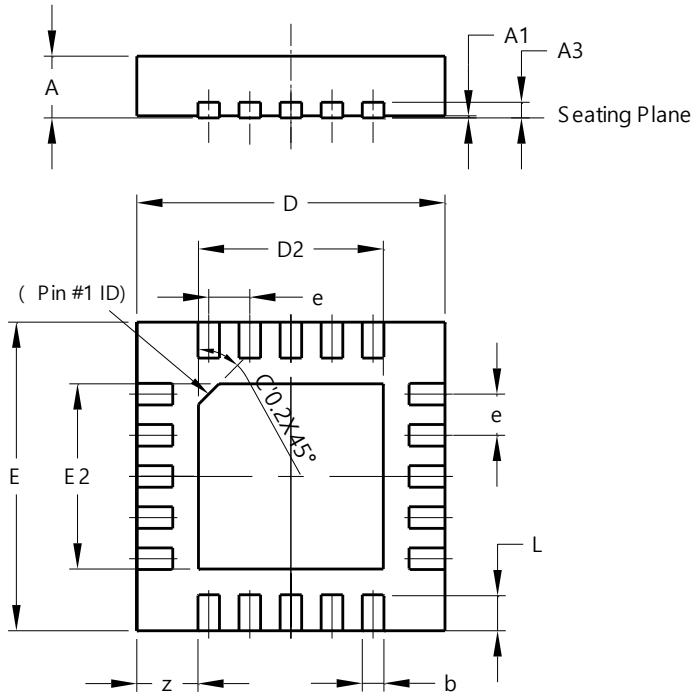
Please see <http://www.diodes.com/package-outlines.html> for the latest version.

U-QFN4040-20



U-QFN4040-20			
Dim	Min	Max	Typ
A	0.55	0.65	0.60
A1	0	0.05	0.02
A3	-	-	0.15
b	0.20	0.30	0.25
D	3.95	4.05	4.00
D2	2.40	2.60	2.50
E	3.95	4.05	4.00
E2	2.40	2.60	2.50
e	0.50 BSC		
L	0.35	0.45	0.40
Z	-	-	0.875
All Dimensions in mm			

U-QFN3030-20

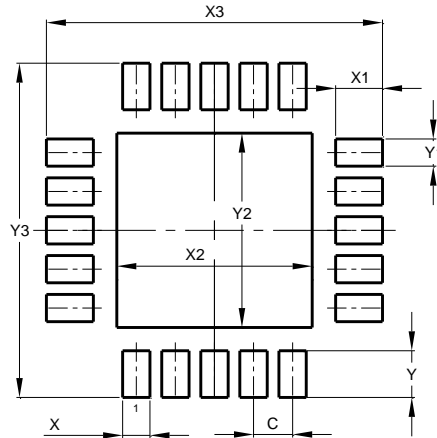


U-QFN3030-20			
Dim	Min	Max	Typ
A	0.57	0.63	0.60
A1	0.00	0.05	0.02
A3	-	-	0.15
b	0.16	0.26	0.21
D	2.95	3.05	3.00
D2	1.70	1.90	1.80
E	2.95	3.05	3.00
E2	1.70	1.90	1.80
e	-	-	0.40
L	0.30	0.40	0.35
z	-	-	0.595
All Dimensions in mm			

Suggested Pad Layout

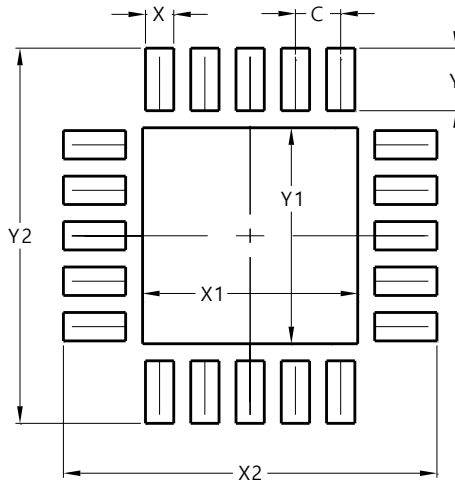
Please see <http://www.diodes.com/package-outlines.html> for the latest version.

U-QFN4040-20



Dimensions	Value (in mm)
C	0.500
X	0.350
X1	0.600
X2	2.500
X3	4.300
Y	0.600
Y1	0.350
Y2	2.500
Y3	4.300

U-QFN3030-20



Dimensions	Value (in mm)
C	0.400
X	0.250
X1	1.900
X2	3.300
Y	0.550
Y1	1.900
Y2	3.300

Mechanical Data

U-QFN4040-20

- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals: Finish – NiPdAu, Solderable per J-STD-002, Test B1 (e4)
- Weight: 0.029 grams (Approximate)

U-QFN3030-20

- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals: Finish – NiPdAu, Solderable per J-STD-002, Test B1 (e4)
- Weight: 0.016 grams (Approximate)

IMPORTANT NOTICE

1. DIODES INCORPORATED (Diodes) AND ITS SUBSIDIARIES MAKE NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARDS TO ANY INFORMATION CONTAINED IN THIS DOCUMENT, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS (AND THEIR EQUIVALENTS UNDER THE LAWS OF ANY JURISDICTION).
2. The Information contained herein is for informational purpose only and is provided only to illustrate the operation of Diodes' products described herein and application examples. Diodes does not assume any liability arising out of the application or use of this document or any product described herein. This document is intended for skilled and technically trained engineering customers and users who design with Diodes' products. Diodes' products may be used to facilitate safety-related applications; however, in all instances customers and users are responsible for (a) selecting the appropriate Diodes products for their applications, (b) evaluating the suitability of Diodes' products for their intended applications, (c) ensuring their applications, which incorporate Diodes' products, comply the applicable legal and regulatory requirements as well as safety and functional-safety related standards, and (d) ensuring they design with appropriate safeguards (including testing, validation, quality control techniques, redundancy, malfunction prevention, and appropriate treatment for aging degradation) to minimize the risks associated with their applications.
3. Diodes assumes no liability for any application-related information, support, assistance or feedback that may be provided by Diodes from time to time. Any customer or user of this document or products described herein will assume all risks and liabilities associated with such use, and will hold Diodes and all companies whose products are represented herein or on Diodes' websites, harmless against all damages and liabilities.
4. Products described herein may be covered by one or more United States, international or foreign patents and pending patent applications. Product names and markings noted herein may also be covered by one or more United States, international or foreign trademarks and trademark applications. Diodes does not convey any license under any of its intellectual property rights or the rights of any third parties (including third parties whose products and services may be described in this document or on Diodes' website) under this document.
5. Diodes' products are provided subject to Diodes' Standard Terms and Conditions of Sale (<https://www.diodes.com/about/company/terms-and-conditions/terms-and-conditions-of-sales/>) or other applicable terms. This document does not alter or expand the applicable warranties provided by Diodes. Diodes does not warrant or accept any liability whatsoever in respect of any products purchased through unauthorized sales channel.
6. Diodes' products and technology may not be used for or incorporated into any products or systems whose manufacture, use or sale is prohibited under any applicable laws and regulations. Should customers or users use Diodes' products in contravention of any applicable laws or regulations, or for any unintended or unauthorized application, customers and users will (a) be solely responsible for any damages, losses or penalties arising in connection therewith or as a result thereof, and (b) indemnify and hold Diodes and its representatives and agents harmless against any and all claims, damages, expenses, and attorney fees arising out of, directly or indirectly, any claim relating to any noncompliance with the applicable laws and regulations, as well as any unintended or unauthorized application.
7. While efforts have been made to ensure the information contained in this document is accurate, complete and current, it may contain technical inaccuracies, omissions and typographical errors. Diodes does not warrant that information contained in this document is error-free and Diodes is under no obligation to update or otherwise correct this information. Notwithstanding the foregoing, Diodes reserves the right to make modifications, enhancements, improvements, corrections or other changes without further notice to this document and any product described herein. This document is written in English but may be translated into multiple languages for reference. Only the English version of this document is the final and determinative format released by Diodes.
8. Any unauthorized copying, modification, distribution, transmission, display or other use of this document (or any portion hereof) is prohibited. Diodes assumes no responsibility for any losses incurred by the customers or users or any third parties arising from any such unauthorized use.
9. This Notice may be periodically updated with the most recent version available at <https://www.diodes.com/about/company/terms-and-conditions/important-notice>

The Diodes logo is a registered trademark of Diodes Incorporated in the United States and other countries.
All other trademarks are the property of their respective owners.
© 2024 Diodes Incorporated. All Rights Reserved.

www.diodes.com