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Chapter 1. Introduction

Growing popularity of standard USB PD3.1 chargers for mobile phone and notebook PC spurs the demand for leveraging standard PD3.1 chargers to replace purposely and individually built chargers for any battery power electronic devices to reduce E-Waste.

AP33772S Evaluation Board (EVB) is intended to be used as an evaluation vehicle for charging applications between a Type C Connector-equipped Device (**TCD**, Energy Sink) and a Type C Connector-equipped PD3.1 compliance Charger or Adaptor (**PDC**, Energy Source).

Figure 1 illustrates a TCD, embedded with PD3.1 Sink controller IC (AP33772S), is physically connected to PDC, embedded with USB PD3.1 decoder (AP43771), through a Type C-to-Type C cable. Based on built-in USB PD3.1 compliant firmware, The AP33772S and AP43771 pair would go through the USB PD3.1 standard attachment procedure to establish suitable PD3.1 charging state.

The AP33772S User's Guide of the Evaluation Board (EVB) explains a flexible I2C setting arrangement (I2C Interface Pin, I2C register Map and Operations) to request desired input voltage and input power for a typical TCD. Various system protection functions and system status checks could be also performance by accessing relevant I2C register contents by the host MCU device of the TCD so as to take proper system actions.

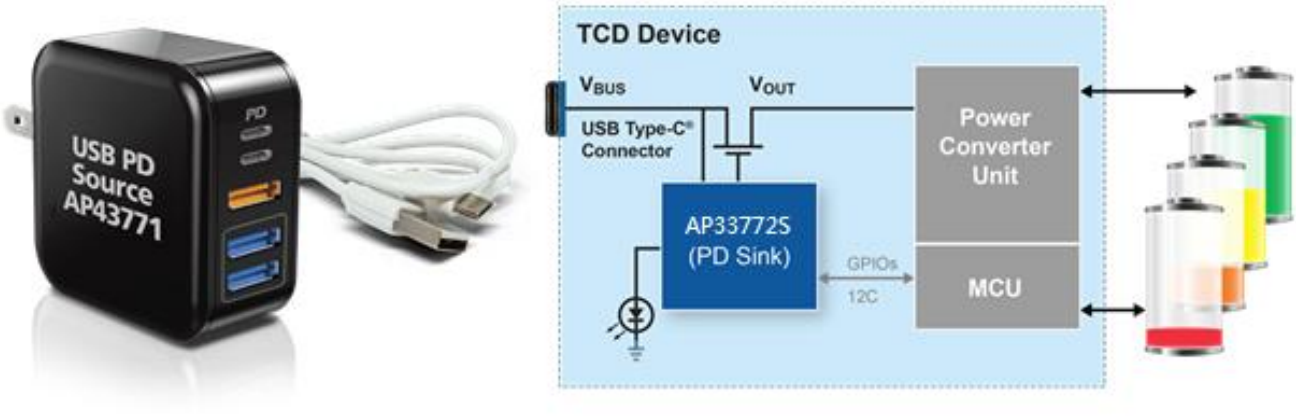


Figure 1 – A typical TCD uses AP33772S PD Sink Controller with I2C Interface to request power from an USB Type-C PD3.1/PPS Compliance Source Adapter

Chapter 2. AP33772S Sink Controller

2.1 Package Outline

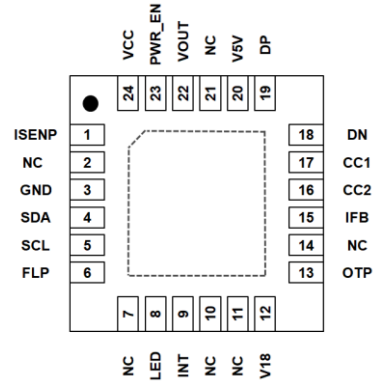


Figure 2 – AP33772S Package Outline

2.2 Pin Descriptions

Pin No	Pin Name	Type (Note)	Pin Function
1	ISENP	AHV	Current Sense Positive Node.
2	NC	-	No Connection
3	GND	GND	Ground
4	SDA	DIO	I2C Data
5	SCL	DI	I2C Clock
6	FLP	DO	Flip indicator of Type-C plug CC1 or CC2
7	NC	-	No Connection
8	LED	DO	LED indication
9	INT	DO	Interrupt pin
10	NC	-	No Connection
11	NC	-	No Connection
12	V18	DP	1.8V LDO output for internal use, need to connect a 100nF cap to GND. This pin cannot drive external load.
13	OTP	AIO	100uA current source output. Can be connected to external NTC sensor for Over Temperature Protection
14	NC	-	No connection.
15	IFB	AI	For current measurement, a 100nF cap to Ground is suggested
16	CC2	AIO	Type-C configuration channel 2
17	CC1	AIO	Type-C configuration channel 1
18	DN	AIO	DN for USB 2.0
19	DP	AIO	DP for USB 2.0
20	V5V	AP	5V LDO output if VCC is on. A 1uF cap is required to connect this pin to GND. Alternative 5V power input for internal 5V core circuit if VCC is off.
21	NC	-	No Connection
22	VOUT	AHV	Terminal for VOUT monitoring and discharge path.
23	PWR_EN	AHV	To control external NMOS switch ON (High) or OFF (Low).
24	VCC	AHV	The power supply of the IC. A 1uF cap is required to connect this pin to GND pin.
-	EPAD	GND	Exposed pad is suggested to connect to Ground

Note:
AHV– Analog High Voltage pin
AP – Power for Analog Circuit and Analog I/O pins, 5.0V operation
AI – Analog Input pin
DP – Power for Digital Circuit operation
AIO – Analog I/O pin with 5.0V operation. CC1/CC2 pins are 3.3V operation
DIO – Digital I/O pin. All are 5.0V operation
DI – Digital input pin. All are 5.0V operation
DO – Digital output pin. All are 5.0V operation

Table 1 – AP33772S Pin Number, Name, Type, and Pin Function

Chapter 3. EVB Hardware Details

3.1 EVB TOP View

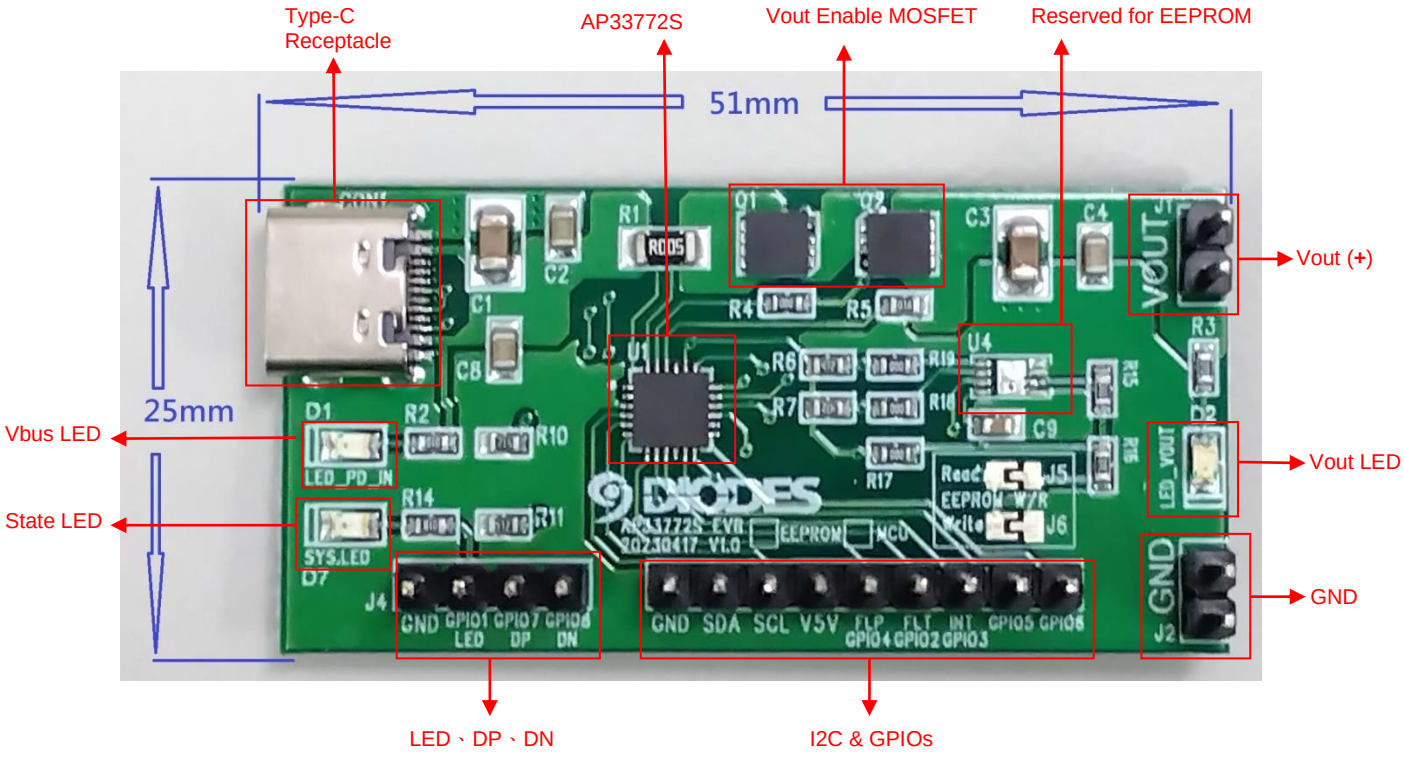


Figure 3 – AP33772S Evaluation board top view and its key portions

3.2 EVB Block Diagram

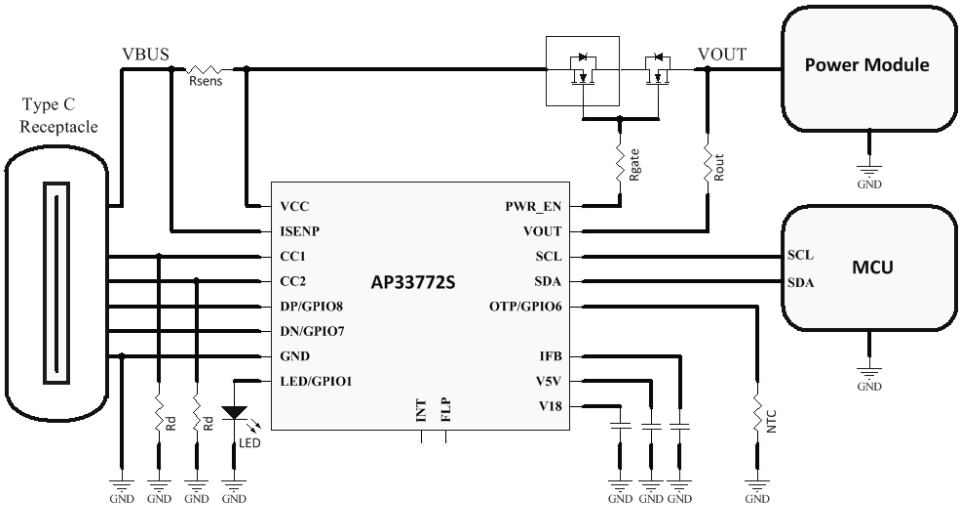


Figure 4 – AP33772S Evaluation Board Block Diagram

3.3 EVB Schematics

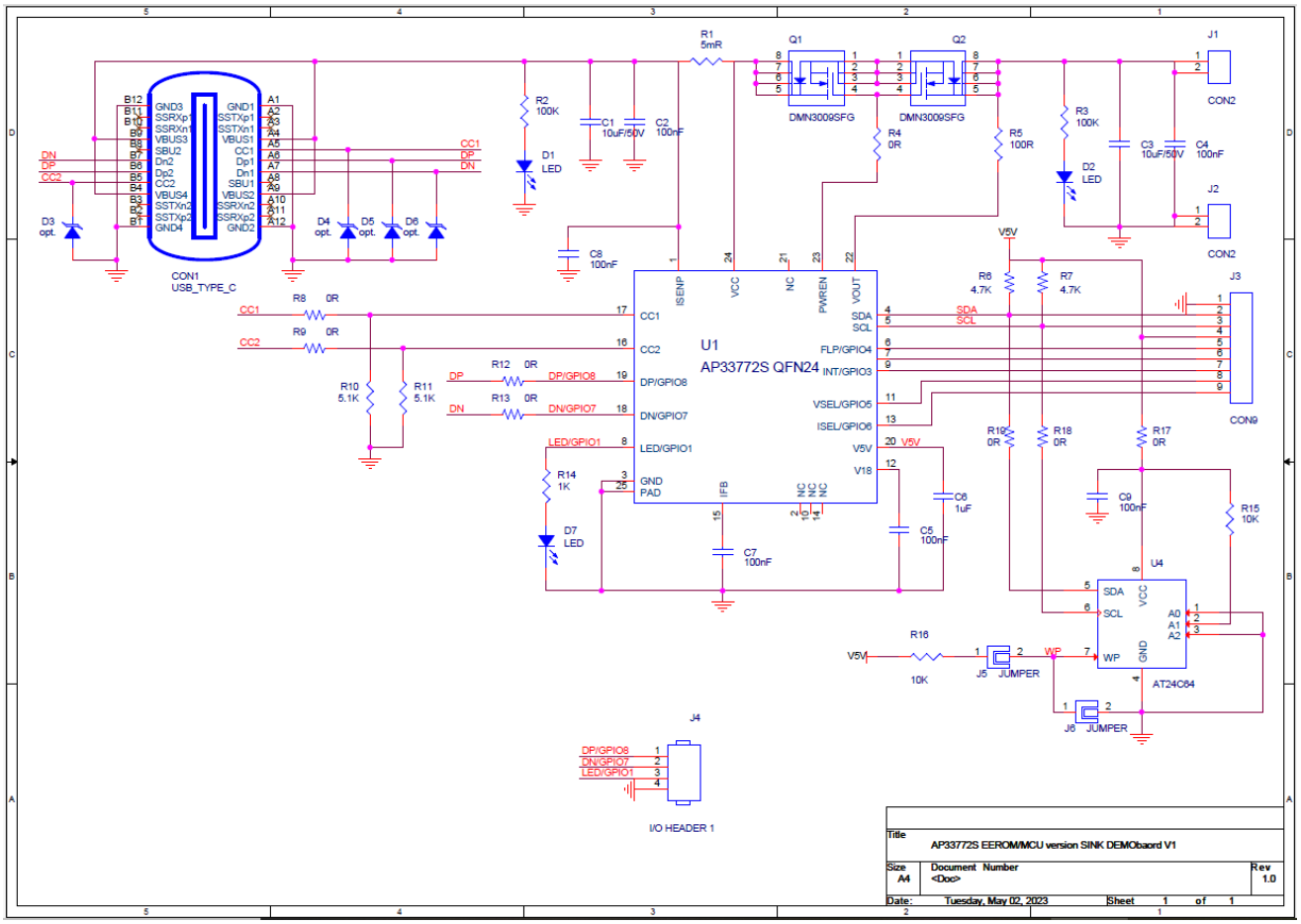


Figure 5 – Detailed schematics of the AP33772S evaluation board

3.4 EVB System BOM

Item	Quantity	Reference	Description	Manufacturer Part Number	Manufacturer
1	2	C1, C3	10u/50V		
2	6	C2, C4, C5, C7, C8, C9	0.1u/50V		
3	1	C6	1u/50V		
4	8	R4, R8. R9, R12, R13, R17, R18,R19	0R		
5	1	R5	100R		
6	1	R14	1K		
7	2	R6, R7	4.7K		
8	2	R10, R11	5.1K		
9	2	R15, R16	10K		
10	2	R2, R3	100K		
11	1	R1	5mR/1W 1206	SMD12A1FR005T	SART Inc.

12	3	D1, D2, D7	LED		
13	2	Q1, Q2	30V/45A/4.4mΩ N-CH PowerDI3333-8	DMN3009SFG	Diodes Inc.
14	1	U1	USB PD3.1 Sink Controller With I²C	AP33772S QFN-24	Diodes Inc.
15	1	U4	Reserved EEPROM solder location	N/A	N/A
16	1	CON1	USB Type-C Receptacle		
17	2	J1, J2	Vout & GND		
18	2	J3, J4	DP, DN, I²C, & other test Pins		
19	4	D3~D6	Zener Diode(option)	N/A	N/A

Table 2 – BOM List of the AP33772S EVB Schematics

Chapter 4. EVB Function Description

AP33772S EVB provides users a convenient but flexible way of power profile setting as well as various status monitoring for proper actions by the host MCU in TCD through simple I2C interface pins (SCL and SDA).

4.1 Board Outline

The AP33772S EVB outline and floor plan is shown as Figure 6, where its connector and jumper location are listed in Table 3.

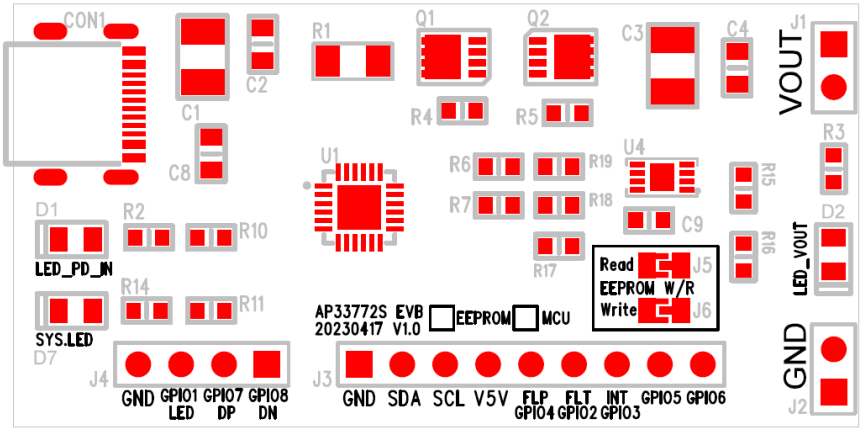


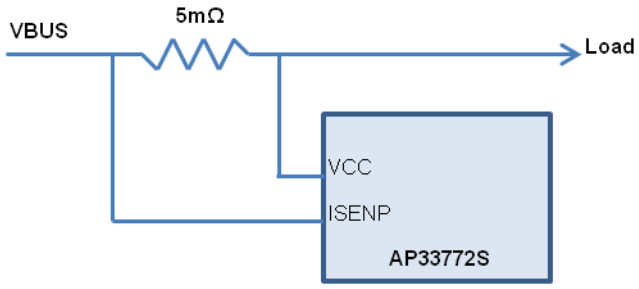
Figure 6 – Connector and jumper locations

Location	Function
J1, J2	VOUT and Load Connector
J3	I2C Bus & other test pins
J4	DP, DN & other test pins

Table 3 – Connectors and jumper names of the evaluation board

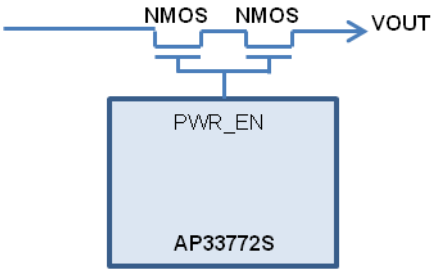
4.2 Application Circuit Description

Sensing of Input Current



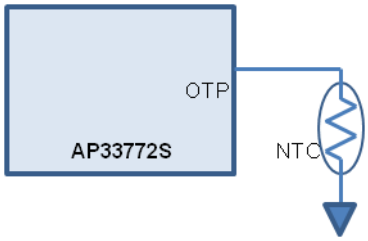
As shown in the figure above, the sense resistor is connected in series to detect the charging current. The ISENP pin is connected to the input side of the sense resistor, and the VCC pin is connected to the other side, AP33772S detects the current by measuring the voltage drop across the current sense resistor.

Use of Back-to-back N-MOS chips



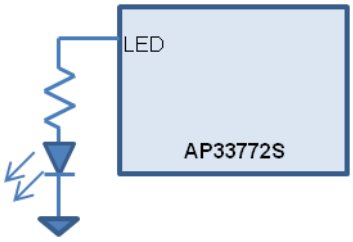
The Common-Source Back-to-back N-MOSFET in the battery pack protection circuit module control charging and play a protective role in the occurrence of failures such as over-voltage, over-current and over-temperature that may damage the electrical appliances. The Back-to-back N-MOSFET control is also used to prevent current flows backward through the system when unplug the cable from PD Charger.

Temperature Sensing Circuitry



A 10kΩ NTC (Negative Temperature Coefficient) thermistor is connected to OTP pin and grounded nearby the potential hot spot. The characteristic data of temperature and resistance value of the NTC thermistor needs to set by the user through I2C. Then host MCU could read and calculate the temperature and enable OTP (Over Temperature Protection), De-rating function through I2C interface.

LED Light Indication Circuitry



The LED light and resistor is used to connect to LED pin and ground. The LED charging indication light starts to breathe at a speed to match quick charging pace for the battery.

I2C Support

The I2C Interface is supported in the AP33772S, and used to communicate with the host MCU of TCD. I2C pins are listed as below Table 4. They are used to set the AP33772S register data like Initialization, PDO, APDO, OCP, OTP, temperature, de-rating, interrupt, and so on, Also, the AP33772S operating status can be monitored at the same time.

Meanwhile, INT is used as a fault report channel to the Interrupt input pin of the host MCU in case of any fault occur which deserves immediate action from the host MCU.

For the I2C commands and registers, please refer to Chapter 5.

Pin No	Pin Name	Pin Function
4	SDA	I2C Data
5	SCL	I2C Clock
9	INT	Issue an interrupt to the host MCU

Table 4 – I2C interface pin list

4.3 Application Alert for Power Sequencing Requirement

When using a Host System (Single Board Computer, or MCU-based System) with I2C interface pins (SDA, SCL) to connect to AP33772S EVB, please make sure to power the AP33772S EVB board first before apply power to the Host System. The power-sequencing requirement for AP33772S EVB being powered up first is a MUST due to the I2C design for SDA and SCL pins.

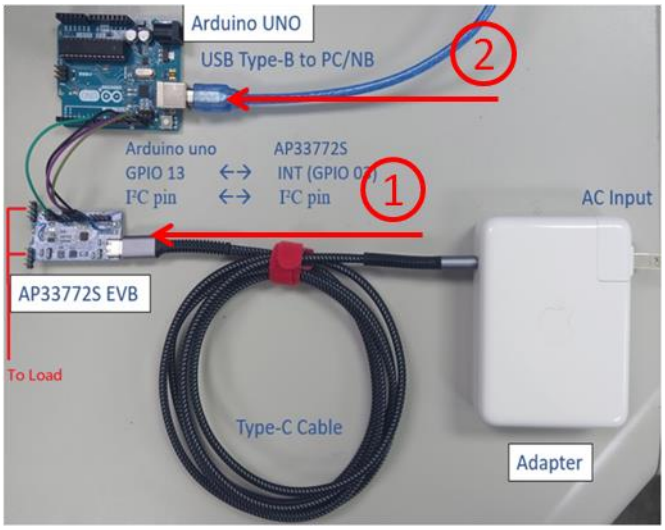


Figure 7 – AP33772S EVB power up sequence

If AP33772S EVB has been connect to the other I2C-based Host System already. The power up sequence MUST be followed:

1. AP33772S EVB should be “Powered Up” first.
2. Then apply power to the Host System Board.

Chapter 5. I2C Command/Register Summary

As an I2C slave device, the physical address of the AP33772S is 0x52. All AP33772S I2C related control operations and commands are summarized in this chapter.

5.1 I2C Command Format

Device Address Format

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
DevAddr6	DevAddr5	DevAddr4	DevAddr3	DevAddr2	DevAddr1	DevAddr0	R/W
1	0	1	0	0	1	0	1/0

Command Format

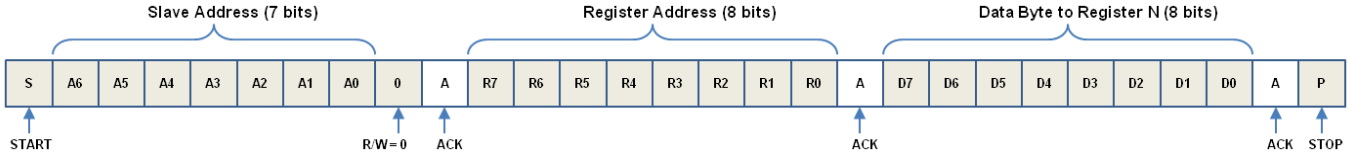
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
CmdBit7	CmdBit6	CmdBit5	CmdBit4	CmdBit3	CmdBit2	CmdBit1	CmdBit0

Data Format

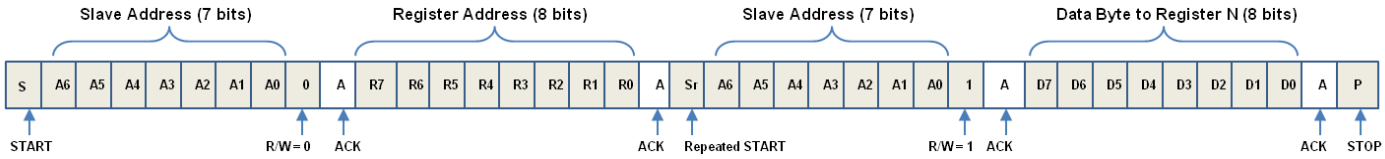
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
DataBit7	DataBit6	DataBit5	DataBit4	DataBit3	DataBit2	DataBit1	DataBit0

5.2 I2C Operation

I2C Write Operation



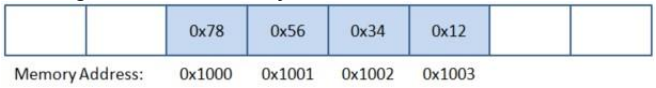
I2C Read Operation



5.3 Register Summary

The memory representation of multibyte data types on AP33772S is Little Endian Byte Order. The least significant byte (the "little end") of the data is placed at the byte with the lowest address.

Suppose integer is stored as 4 bytes then a variable X with value 0x12345678 will be stored as following.



Register	Command	Length	Attribute	Pwr-on	Description
STATUS	0x01	1	RC	00h	Status
MASK	0x02	1	RW	03h	Interrupt enable mask
OPMODE	0x03	1	RO	00h	Operation mode
CONFIG	0x04	1	RW	F8h	System configuration options
PDCONFIG	0x05	1	RW	03h	PD mode configuration options
SYSTEM	0x06	1	RO/RW	10h	System control and information
TR25	0x0C	2	RW	2710h	Thermal Resistance @25°C, Unit: Ω
TR50	0x0D	2	RW	1041h	Thermal Resistance @50°C, Unit: Ω
TR75	0x0E	2	RW	0788h	Thermal Resistance @75°C, Unit: Ω
TR100	0x0F	2	RW	03CEh	Thermal Resistance @100°C, Unit: Ω
VOLTAGE	0x11	2	RO	0000h	The VOUT Voltage, LSB 80mV
CURRENT	0x12	1	RO	00h	The VOUT Current, LSB 24mA
TEMP	0x13	1	RO	19h	Temperature, Unit: °C The default value is 19h (25°C).
VREQ	0x14	2	RO	0000h	The latest requested voltage negotiated with the source, LSB 50mV
IREQ	0x15	2	RO	0000h	The latest requested current negotiated with the source, LSB 10mA
VSELMIN	0x16	1	RW	19h	The Minimum Selection Voltage, LSB 200mV The default value is 19h (5000mV).
UVPTHR	0x17	1	RW	01h	UVP Threshold, percentage(%) of VREQ The default value is 01h (80%).
OVPTHR	0x18	1	RW	19h	OVP Threshold, offset from VREQ. LSB 80mV The default value is 19h (2000mV).
OCPTHR	0x19	1	RW	00h	OCP Threshold, LSB 50mA
OTPTHR	0x1A	1	RW	78h	OTP Threshold, Unit: °C The default value is 78h (120°C).
DRTHR	0x1B	1	RW	78h	De-Rating Threshold, Unit: °C The default value is 78h (120°C).
SRCPDO	0x20	26	RO	All 00h	Get all PD Source Power Capabilities (SRC_SPR_PDO1 ~ SRC_EPR_PDO13)
SRC_SPR_PDO1	0x21	2	RO	0000h	Source SPR PDO1
SRC_SPR_PDO2	0x22	2	RO	0000h	Source SPR PDO2
SRC_SPR_PDO3	0x23	2	RO	0000h	Source SPR PDO3
SRC_SPR_PDO4	0x24	2	RO	0000h	Source SPR PDO4
SRC_SPR_PDO5	0x25	2	RO	0000h	Source SPR PDO5
SRC_SPR_PDO6	0x26	2	RO	0000h	Source SPR PDO6
SRC_SPR_PDO7	0x27	2	RO	0000h	Source SPR PDO7
SRC_EPR_PDO8	0x28	2	RO	0000h	Source EPR PDO8
SRC_EPR_PDO9	0x29	2	RO	0000h	Source EPR PDO9
SRC_EPR_PDO10	0x2A	2	RO	0000h	Source EPR PDO10
SRC_EPR_PDO11	0x2B	2	RO	0000h	Source EPR PDO11
SRC_EPR_PDO12	0x2C	2	RO	0000h	Source EPR PDO12
SRC_EPR_PDO13	0x2D	2	RO	0000h	Source EPR PDO13
PD_REQMSG	0x31	2	WO	0000h	Send request message with selected voltage, current and PDO index
PD_CMDMSG	0x32	1	WO	00h	Send specific PD command message
PD_MSGRLT	0x33	1	RO	00h	Result and status of PD request or command message

Attribute Convention
RW: Readable / Writable
RO: Read-Only
RC: Read-Clear
WO: Write-Only

Table 5 – AP33772S Register Summary

5.4 Register Description

STATUS

The host MCU, working as I2C master, can access status of the AP33772S through the STATUS register. The STATUS register will be reset to 0 after a read operation.

STATUS	Bit	Attribute	Pwr-on	Description
	7	RC	0h	Reserved
OTP	6	RC	0h	1:OTP status
OCP	5	RC	0h	1: OCP status
OVP	4	RC	0h	1: OVP status
UVP	3	RC	0h	1:UVP status
NEWPDO	2	RC	0h	1: New source PDOs received (Valid when PDMOD = 1)
READY	1	RC	0h	1: Ready to receive I2C request/command
STARTED	0	RC	0h	1: System started. Allow system configuration (register) to be updated within 100ms

MASK

The AP33772S supports a level-triggered interrupt signal through INT pin to the host MCU. The MASK register defines enable and disable of ON and OFF for various STATUS defined events.

MASK	Bit	Attribute	Pwr-on	Description
	7	RW	0h	Reserved
OTP_MSK	6	RW	0h	1: OTP status mask
OCP_MSK	5	RW	0h	1: OCP status mask
OVP_MSK	4	RW	0h	1: OVP status mask
UVP_MSK	3	RW	0h	1: UVP status mask
NEWPDO_MSK	2	RW	0h	1: NEWPDO status mask
READY_MSK	1	RW	1h	1: READY status mask
STARTED_MSK	0	RW	1h	1: STARTED status mask

OPMODE

The OPMODE register defines the operation mode of AP33772S.
When CCFLP = 1, CC2 is connected to CC line.
When DR = 1, AP33772S works in De-rating (DR) mode.
When PDMOD = 1, AP33772S works in PD mode.
When LGCYMOD = 1, AP33772S works in Legacy mode (non-PD).

OPMODE	Bit	Attribute	Pwr-on	Description
CCFLP	7	RO	0h	0 : CC1 is connected to CC line or unattached mode 1 : CC2 is connected to CC line
DR	6	RO	0h	0 : Normal mode 1 : DR (De-Rating) mode
	5	RO	0h	Reserved
	4	RO	0h	Reserved
	3	RO	0h	Reserved
	2	RO	0h	Reserved
PDMOD	1	RO	0h	1: PD source connected
LGCYMOD	0	RO	0h	1: Legacy source connected (non-PD)

CONFIG

The CONFIG register defines the system configuration options that enable specific modules.

CONFIG	Bit	Attribute	Pwr-on	Description
DR_EN	7	RW	1h	0/1: Disable/enable DR function
OTP_EN	6	RW	1h	0/1: Disable/enable OTP function
OCP_EN	5	RW	1h	0/1: Disable/enable OCP function
OVP_EN	4	RW	1h	0/1: Disable/enable OVP function
UVP_EN	3	RW	1h	0/1: Disable/enable UVP function
	2	RW	0h	Reserved
	1	RW	0h	Reserved
	0	RW	0h	Reserved

PDCONFIG

The PDCONFIG register defines the PD mode configuration options that enable specific modules.

PDCONFIG	Bit	Attribute	Pwr-on	Description
	7:4	RW	0h	Reserved
	3	RW	0h	Reserved
	2	RW	0h	Reserved
PPS_AVS_EN	1	RW	1h	0/1 : Disable/Enable sink PPS and AVS capability
EPR_MODE_EN	0	RW	1h	0/1 : Disable/Enable EPR mode

SYSTEM

The SYSTEM register defines the system information and control options that request specific functions.

By default, the VOUT MOS Switches are controlled by AP33772S. Writing the VOUTCTL parameter can force the VOUT MOS Switches to turn OFF/ON.

SYSTEM	Bit	Attribute	Pwr-on	Description
	7	RO	0h	Reserved
	6	RO	0h	Reserved
CMDVER	5:4	RO	1h	I2C Command Version 1: Version 1.0 others: Reserved, Shall Not be used
	3	RW	0h	Reserved
	2	RW	0h	Reserved
VOUTCTL	1:0	RW	0h	VOUT control option switch 0: Auto VOUT Control (controlled by AP33772S) 1: VOUT force OFF 2: VOUT force ON 3: Reserved, Shall Not be used

TR25

The TR25 register defines the resistance value of NTC thermistor at 25°C (Unit: Ω).

TR25	Bit	Attribute	Pwr-on	Description
TR25	15:0	RW	2710h	The resistance value of NTC thermistor at 25°C (Unit: Ω) The default value is 2710h (10000Ω)

TR50

The TR50 register defines the resistance value of NTC thermistor at 50°C (Unit: Ω).

TR50	Bit	Attribute	Pwr-on	Description
TR50	15:0	RW	1041h	The resistance value of NTC thermistor at 50°C (Unit: Ω) The default value is 1041h (4161Ω)

TR75

The TR75 register defines the resistance value of NTC thermistor at 75°C (Unit: Ω).

TR75	Bit	Attribute	Pwr-on	Description
TR75	15:0	RW	0788h	The resistance value of NTC thermistor at 75°C (Unit: Ω) The default value is 0788h (1928Ω)

TR100

The TR100 register defines the resistance value of NTC thermistor at 100°C (Unit: Ω).

TR100	Bit	Attribute	Pwr-on	Description
TR100	15:0	RW	03CEh	The resistance value of NTC thermistor at 100°C (Unit: Ω) The default value is 03CEh (974Ω)

VOLTAGE

The VOLTAGE register contains the voltage of VOUT. The LSB (Least Significant Bit) is 80mV.

VOLTAGE	Bit	Attribute	Pwr-on	Description
VOLTAGE	15:0	RO	0000h	The VOUT Voltage, LSB 80mV

CURRENT

The CURRENT register contains the current of VOUT. The LSB is 24mA.

CURRENT	Bit	Attribute	Pwr-on	Description
CURRENT	7:0	RO	00h	The VOUT Current, LSB 24mA

TEMP

The TEMP register contains the temperature near the NTC thermistor. The unit is °C. The default value is 19h (25°C).

TEMP	Bit	Attribute	Pwr-on	Description
TEMP	7:0	RO	19h	Temperature near the NTC thermistor, Unit: °C The default value is 19h (25°C).

VREQ

The VREQ register contains the latest request voltage, which depends on the PD negotiation result after setting request message (PD_REQMSG). The LSB is 50mV.

Host MCU write PD_REQMSG will initiate a PD negotiation process. If negotiation is successful (PD_MSGRLT.RESPONSE = 1), VREQ will be updated to the requested voltage (PD_REQMSG.VOLTAGE_SEL). If negotiation is unsuccessful, VREQ will not be updated.

VREQ	Bit	Attribute	Pwr-on	Description
VREQ	15:0	RO	0000h	The latest requested voltage, LSB 50mV The value depends on the PD negotiation result after setting PD_REQMSG (VOLTAGE_SEL).

IREQ

The IREQ register contains the latest request current, which depends on the PD negotiation result after setting request message (PD_REQMSG). The LSB is 10mA.

If negotiation is successful (PD_MSGRLT.RESPONSE=1), IREQ will be updated to the requested current (PD_REQMSG.CURRENT_SEL). If negotiation is unsuccessful, IREQ will not be updated.

IREQ	Bit	Attribute	Pwr-on	Description
IREQ	15:0	RO	0000h	The latest requested current, LSB 10mA The value depends on the PD negotiation result after setting PD_REQMSG (CURRENT_SEL).

VSELMIN

The VSELMIN register defines the Minimum Selection Voltage. If the VREQ voltage is more than or equal to the VSELMIN voltage, the VOUT MOS Switches turn ON after the system is ready (STATUS.READY = 1). The default value for VSELMIN is 19h (5000mV) and the LSB is 200mV.

VSELMIN	Bit	Attribute	Pwr-on	Description
VSELMIN	7:0	RW	19h	The Minimum Selection Voltage, the LSB is 200mV. If $V_{VREQ} \geq V_{VSELMIN}$, VOUT MOS Switches turn on after system ready (READY=1). The default value is 19h (5000mV).

UVPTHR

The UVPTHR register defines the UVP Threshold Voltage that triggers UVP protection function. The UVP Threshold Voltage is UVPTHR percentage (%) of the VREQ voltage. The default value for UVPTHR is 01h (80%). Refer to Under Voltage Protection section for more details.

UVPTHR	Bit	Attribute	Pwr-on	Description
	7:4	RW	0h	Reserved
UVPTHR	3:0	RW	1h	The UVP Threshold Voltage is UVPTHR percentage (%) of VREQ voltage. Unit: % 1: 80% 2: 75% 3: 70% others: Reserved, Shall Not be used The default value is 01h (80%).

OVPTHR

The OVPTHR register defines the OVP Threshold Voltage that triggers OVP protection function. The OVP Threshold Voltage is the VREQ voltage plus OVPTHR offset voltage (mV). The default value for OVPTHR is 19h (2000mV) and the LSB is 80mV. Refer to Over Voltage Protection section for more details.

OVPTHR	Bit	Attribute	Pwr-on	Description
OVPTHR	7:0	RW	19h	The OVP Threshold Voltage is the VREQ voltage plus OVPTHR offset voltage (mV), the LSB is 80mV. The default value is 19h (2000mV). That means the OVP Threshold Voltage is V_{VREQ} +2000mV by default.

OCPTHR

The OCPTHR register defines the OCP Threshold Current that triggers OCP protection function. The OCP Threshold Current is 110% of the OCPTHR current value. The default value for OCPTHR is 00h and the LSB is 50mA.

If OCPTHR is set to 0, the OCP Threshold Current will be updated to 110% of the selected PDO maximum current after successful negotiation with PD source. Refer to Over Current Protection section for more details.

OCPTHR	Bit	Attribute	Pwr-on	Description
OCPTHR	7:0	RW	00h	The OCP Threshold Current is 110% of the OCPTHR current value, the LSB is 50mA. The default value is 00h. That means the OCP Threshold Current will be updated to 110% of the selected PDO maximum current after successful negotiation.

OTPTHR

The OTPTHR register defines the OTP Threshold Temperature (°C) that triggers OTP protection function. The default value for OTPTHR is 78h (120°C). Refer to Over Temperature Protection and De-rating section for more details.

OTPTHR	Bit	Attribute	Pwr-on	Description
OTPTHR	7:0	RW	78h	OTP Threshold Temperature, Unit: °C The temperature threshold triggers OTP function, the default value for OTPTHR is 78h (120°C).

DRTHR

The DRTHR register defines the De-Rating Threshold Temperature (°C) that triggers the De-Rating function. The default value for DRTHR is 78h (120°C). Refer to Over Temperature Protection and De-rating section for more details.

DRTHR	Bit	Attribute	Pwr-on	Description
DRTHR	7:0	RW	78h	De-Rating Threshold Temperature, Unit: °C The temperature threshold triggers De-Rating function, the default value for DRTHR is 78h (120°C).

SRCPDO

The SRCPDO register can obtain all the PD Source Power Capabilities and has a total length of 28 bytes.

SRCPDO	Byte	Attribute	Pwr-on	Description
SRC_EPR_PDO13	25:24	RO	0000h	Data format refer to **SRC_EPR_PDO**
SRC_EPR_PDO12	23:22	RO	0000h	
SRC_EPR_PDO11	21:20	RO	0000h	
SRC_EPR_PDO10	19:18	RO	0000h	
SRC_EPR_PDO9	17:16	RO	0000h	
SRC_EPR_PDO8	15:14	RO	0000h	
SRC_SPR_PDO7	13:12	RO	0000h	Data format refer to **SRC_SPR_PDO**
SRC_SPR_PDO6	11:10	RO	0000h	
SRC_SPR_PDO5	9:8	RO	0000h	
SRC_SPR_PDO4	7:6	RO	0000h	
SRC_SPR_PDO3	5:4	RO	0000h	
SRC_SPR_PDO2	3:2	RO	0000h	
SRC_SPR_PDO1	1:0	RO	0000h	

SRC_SPR_PDO1 ~ SRC_SPR_PDO7

The SRC_SPR_PDO register can obtain the PD Source SPR PDO of a specific index, each length is 2 bytes. The structure of the SRC_SPR_PDO register is as follows.

<table>
<tr><th>SRC_SPR_PDO</th><th>Bit</th><th>Attribute</th><th>Pwr-on</th><th colspan="2">Description</th></tr>
<tr><td>DETECT</td><td>15</td><td>RO</td><td>0h</td><td colspan="2">0: Not detected
1: Detected</td></tr>
<tr><td>TYPE</td><td>14</td><td>RO</td><td>0h</td><td colspan="2">0: Fixed PDO
1: PPS APDO</td></tr>
<tr><td>CURRENT_MAX</td><td>13:10</td><td>RO</td><td>0h</td><td colspan="2">0: 0.00A ~ 1.24A (Less than 1.24A)
1: 1.25A ~ 1.49A
2: 1.50A ~ 1.74A
3: 1.75A ~ 1.99A
4: 2.00A ~ 2.24A
5: 2.25A ~ 2.49A
6: 2.50A ~ 2.74A
7: 2.75A ~ 2.99A
8: 3.00A ~ 3.24A
9: 3.25A ~ 3.49A
10: 3.50A ~ 3.74A
11: 3.75A ~ 3.99A
12: 4.00A ~ 4.24A
13: 4.25A ~ 4.49A
14: 4.50A ~ 4.99A
15: 5.00A ~ (More than 5.00A)</td></tr>
<tr><td rowspan="2">PEAK_CURRENT
or
VOLTAGE_MIN</td><td rowspan="2">9:8</td><td rowspan="2">RO</td><td rowspan="2">0h</td><td>PEAK_CURRENT</td><td>VOLTAGE_MIN</td></tr>
<tr><td>For Fixed PDO (bit[14]=0)
Peak Current</td><td>For PPS APDO (bit[14]=1)
0 : Reserved
1 : 3.3V
2 : 3.3V < VOLTAGE_MIN ≤ 5V
3 : others</td></tr>
<tr><td>VOLTAGE_MAX</td><td>7:0</td><td>RO</td><td>0h</td><td colspan="2">If bit[14]=0 (Fixed PDO) :
Voltage in 100mV units
If bit[14]=1 (PPS APDO) :
Maximum Voltage in 100mV units</td></tr>
</table>

SRC_EPR_PDO8 ~ SRC_EPR_PDO13

The SRC_EPR_PDO register can obtain the PD Source EPR PDO of a specific index, each length is 2 bytes. The structure of the SRC_EPR_PDO register is as follows.

SRC_EPR_PDO	Bit	Attribute	Pwr-on	Description
DETECT	15	RO	0h	0: Not detected 1: Detected
TYPE	14	RO	0h	0: Fixed PDO 1: AVS APDO
CURRENT_MAX	13:10	RO	0h	0: 0.00A ~ 1.24A (Less than 1.24A) 1: 1.25A ~ 1.49A 2: 1.50A ~ 1.74A 3: 1.75A ~ 1.99A 4: 2.00A ~ 2.24A 5: 2.25A ~ 2.49A 6: 2.50A ~ 2.74A 7: 2.75A ~ 2.99A 8: 3.00A ~ 3.24A 9: 3.25A ~ 3.49A 10: 3.50A ~ 3.74A 11: 3.75A ~ 3.99A 12: 4.00A ~ 4.24A 13: 4.25A ~ 4.49A 14: 4.50A ~ 4.99A 15: 5.00A ~ (More than 5.00A)
PEAK_CURRENT or VOLTAGE_MIN	9:8	RO	0h	PEAK_CURRENT: For Fixed PDO (bit[14]=0) Peak Current VOLTAGE_MIN: For AVS APDO (bit[14]=1) 0 : Reserved 1 : 15V 2 : 15V < VOLTAGE_MIN ≤ 20V 3 : others
VOLTAGE_MAX	7:0	RO	0h	If bit[14]=0 (Fixed PDO) : Voltage in 200mV units If bit[14]=1 (AVS APDO) : Maximum Voltage in 200mV units

Bits 9…8	Description for **PEAK_CURRENT**
00	Peak current equals I_{OC} (default) or look at extended Source capabilities
01	Overload Capabilities: 1. Peak current equals 150% I_{OC} for 1ms @ 5% duty cycle (low current equals 97% I_{OC} for 19ms) 2. Peak current equals 125% I_{OC} for 2ms @ 10% duty cycle (low current equals 97% I_{OC} for 18ms) 3. Peak current equals 110% I_{OC} for 10ms @ 50% duty cycle (low current equals 90% I_{OC} for 10ms)
10	Overload Capabilities: 1. Peak current equals 200% I_{OC} for 1ms @ 5% duty cycle (low current equals 95% I_{OC} for 19ms) 2. Peak current equals 150% I_{OC} for 2ms @ 10% duty cycle (low current equals 94% I_{OC} for 18ms) 3. Peak current equals 125% I_{OC} for 10ms @ 50% duty cycle (low current equals 75% I_{OC} for 10ms)
11	Overload Capabilities: 1. Peak current equals 200% I_{OC} for 1ms @ 5% duty cycle (low current equals 95% I_{OC} for 19ms) 2. Peak current equals 175% I_{OC} for 2ms @ 10% duty cycle (low current equals 92% I_{OC} for 18ms) 3. Peak current equals 150% I_{OC} for 10ms @ 50% duty cycle (low current equals 50% I_{OC} for 10ms)
I_{OC} : The Operating Current of an RDO (The Operating Current Select parameter of PD_REQMSG) For more information, refer to the “Peak Current” section of the USB PD Specification.	

PD_REQMSG

The PD_REQMSG register defines the request message format to initiate negotiation with the PD source. The request message can select the source PDO index and request the desired voltage and current output. If the selected PDO is a Fixed PDO (TYPE=0), setting VOLTAGE_SEL has no meaning (except VOLTAGE_SEL=FFh).

PD_REQMSG	Bit	Attribute	Pwr-on	Description
PDO_INDEX	15:12	WO	0h	Source PDO index select [1] ~ [7]: For SRC_SPR_PDO1 ~ SRC_SPR_PDO7 selection, if its corresponding PDO is detected [8] ~ [13]: For SRC_EPR_PDO8 ~ SRC_EPR_PDO13 selection, if its corresponding PDO is detected Others: Reserved, Shall Not be used
CURRENT_SEL	8:11	WO	0h	Operating Current Select 0: 1.00A 1: 1.25A 2: 1.50A 3: 1.75A 4: 2.00A 5: 2.25A 6: 2.50A 7: 2.75A 8: 3.00A 9: 3.25A 10: 3.50A 11: 3.75A 12: 4.00A 13: 4.25A 14: 4.50A 15: 5.00A or Maximum Current (Note1)
VOLTAGE_SEL	7:0	WO	0h	Output Voltage Select If select SRC_SPR_PDO (PDO1 ~ PDO7): (Note2) Output Voltage in 100mV units for SPR PPS APDO selected If select SRC_EPR_PDO (PDO8 ~ PDO13): Output Voltage in 200mV units for EPR AVS APDO selected FFh: Maximum Voltage (Note1)
Note1: If set CURRENT_SEL=Fh and VOLTAGE_SEL=FFh, AP33772S will request the Maximum Current and Maximum Voltage of the selected Source PDO Note2: Setting VOLTAGE_SEL has no meaning when a Fixed PDO is selected				

AP33772S provides special request message to request the maximum current and maximum voltage of the selected source PDO by setting only PDO_INDEX and keeping CURRENT_SEL = Fh and VOLTAGE_SEL = FFh.

For example, if source PDO3 is detected, writing PD_REQMSG=3FFFh to request the maximum current and maximum voltage of source PDO3.

PD_REQMSG	Bit	Attribute	Pwr-on	Value
PDO_INDEX	15:12	WO	0h	1 to 13
CURRENT_SEL	8:11	WO	0h	Fh
VOLTAGE_SEL	7:0	WO	0h	FFh

PD_CMDMSG

The PD_CMDMSG register defines the command message that issues the specific USB PD command.

PD_CMDMSG	Bit	Attribute	Pwr-on	Description
	7:4	WO	0h	Reserved
	3	WO	0h	Reserved
	2	WO	0h	Reserved
	1	WO	0h	Reserved
HRST	0	WO	0h	1: Issue Hard Reset command

PD_MSGRLT

The PD_MSGRLT register defines the message processing results of PD_REQMSG and PD_CMDMSG.

The RESPONSE parameter displays the message response made by AP33772S base on the result of interaction with the PD source. The response values and meanings are as follows.

PD_MSGRLT	Bit	Attribute	Pwr-on	Description
	7:4	RO	0h	Reserved
	3	RO	0h	Reserved
RESPONSE	2:0	RO	0h	The message response 0: System busy or no response 1: Success 2: Invalid command or argument 3: Command not supported or rejected 4: Transaction failed. No GoodCRC is received after sending Others: Reserved

Chapter 6. Function Description

6.1 I2C Request Message

I2C request message (PD_REQMSG) can update the PDO index, Operating Current and Output Voltage settings at runtime.

- PDO_INDEX can assign the source PDO index.
- CURRENT_SEL can set the Operating Current value of RDO.
- VOLTAGE_SEL can set the Output Voltage value of PPS/AVS RDO, but it has no meaning for selecting Fixed PDO.

AP33772S starts to negotiate with PD source after receiving the PD_REQMSG. When the PD negotiation is completed AP33772S sets the STATUS.READY bit and update the negotiation result in PD_MSGRLT.RESPONSE.

6.2 Support EPR / AVS

After the first negotiation with PD source which supports EPR Mode, AP33772S will try to enter EPR Mode when PDCONFIG.EPR_MODE is set to 1. If successfully enter EPR Mode, AP33772S stores the EPR Source Capability in SRC_EPR_PDOx registers and enables EPR request.

6.3 VOUT MOS Switch

When VREQ voltage is more than or equal to VSELMIN voltage, AP33772S enables the associated MOS Switches and then VBUS is connected to VOUT.

When over-voltage, under-voltage, over-current or over-temperature protection occurs, the associated VOUT MOS Switches are turned off to protect the electrical appliances from possible damage. The host MCU will need to load a new PD_REQMSG to start the PD negotiation process to resume quick charging operation.

By default, the VOUT MOS Switches are controlled by AP33772S. Writing the VOUTCTL parameter of SYSTEM register can force the VOUT MOS Switches to turn OFF/ON.

6.4 LED Indication

The AP33772S controls LED lighting through LED pin. Table bellow summarizes the LED indication and VOUT in each State.

State	LED Indication	VOUT	Comments
INIT	NA	OFF	VBUS/Rp attached and AP33772S initialization
CHARGING	4-sec Breathing	ON	Successful negotiation or enter Non-PD Mode and start charging
MISMATCH	Full Light	OFF	VSELMIN mismatch ($V_{VREQ} < V_{VSELMIN}$)
MOISTURE	2-sec Flicker	OFF	DN abnormal impedance detected
FAULT	0.6-sec Flicker	OFF	OVP, OCP, UVP or OTP occurs

6.5 Interrupt

The AP33772S supports a level-triggered interrupt signal through INT pin to the host MCU. The MASK register defines enable and disable of options of ON and OFF for each interrupt-able event.

Interrupt initialization is required before use. When defined interrupt-able event happens, the AP33772S will set the INT level high (1) if the relevant event of the MASK register is enabled. Then the host MCU should read STATUS to obtain the status of AP33772S in real time.

For example, if the OVP_MSK is set to be 1 (MASK = 0x13), INT is to be set at high when OVP event occurs.

6.6 CC Flip Indication

AP33772S uses FLP Pin for CC Flip Indication. If CC is non-flipped (CC1 attached), the FLP output low. If CC is flipped (CC2 attached), the FLP output high.

CC Flip Indication		
CC Detection	**CC1** Attached	**CC2** Attached
FLP Output	**Low** (0)	**High** (1)

6.7 Legacy Type A Charger with Type A-to-C Cable

When the energy source is from a legacy Type A charger with Type A-to-C cable connection to the Type-C Connector-equipped Devices (TCD), the AP33772S enters the Non-PD Mode after PD negotiation fails. When VREQ voltage is less than VSELMIN voltage, the associated VOUT MOS Switches are turned off. Table bellow shows the Non-PD Mode state of AP33772S.

Non-PD Mode State		
V_{VREQ}	$V_{VSELMIN}$	V_{VOUT}
V_{VREQ} = 5V	$V_{VSELMIN}$ = 5V	ON
V_{VREQ} = 5V	$V_{VSELMIN}$ > 5V	OFF

6.8 Temperate Estimate

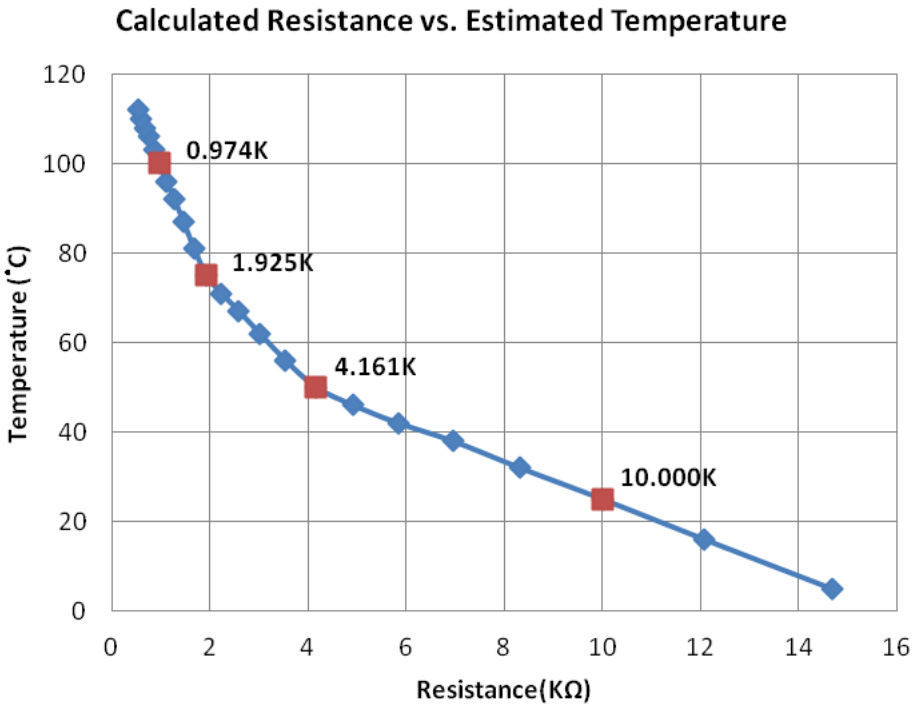
The AP33772S measures and estimates the temperature value based on 4 User-Entered NTC resistance value vs. temperature (TR25, TR50, TR75 and TR100) in the practical usage temperature range of the TCD.

AP33772S use Murata NTC NCP03XH103 as default. Table bellow shows the NTC resistance value vs. temperature.

Register	Default Value	NTC Resistance (KΩ)	Temperature (°C)
TR25	2710h	10	25
TR50	1041h	4.161	50
TR75	0788h	1.928	75
TR100	03CEh	0.974	100

If the calculated NTC resistance value is bounded by TR25 and TR100, the AP33772S uses the “LINEAR INTERPOLATION” of the two bounding TR values to estimate the temperature value and deposits this estimated temperature value in the I2C register TEMP.

If the calculated NTC resistance value is higher than TR25 value, the AP33772S uses the “LINEAR EXTRAPOLATION” of TR50 and TR25 to estimate the temperature below 25°C. Similarly, if the calculated resistance value is lower than TR100 value, the AP33772S uses the “LINEAR EXTRAPOLATION” of TR75 and TR100 to estimate the temperature above 100°C.



Ex. AP33772S calculates the resistance value of NTC is 2.250kΩ. The near boundary 50°C is 4.161kΩ, 75°C is 1.925kΩ. Therefore, 2.250kΩ corresponds to:

SLOPE = (1.925kΩ – 4.161kΩ) / (75°C – 50°C) = - 0.08944 kΩ/°C
Temperature = 50°C + (2.250kΩ - 4.161kΩ) / (- 0.08944 kΩ/°C) = 71.4°C

So, the TEMP register value is to be set at 47h (71°C).

Chapter 7. Protection

7.1 Over Voltage Protection (OVP)

The AP33772S triggers the OVP protection when VBUS voltage is higher than OVP Threshold Voltage. Table bellow summarizes correspondence between VREQ, OVPTHR and OVP Threshold Voltage.

Mode	Criteria	OVP Threshold Voltage
SPR Mode	(V_{VREQ} + V_{OVPTHR}) ≤ 20V	**V_{VREQ} + V_{OVPTHR}**
	(V_{VREQ} + V_{OVPTHR}) > 20V	**V_{VREQ} * 110%**
EPR Mode	(V_{VREQ} + V_{OVPTHR}) ≤ 40V	**V_{VREQ} + V_{OVPTHR}**
	(V_{VREQ} + V_{OVPTHR}) > 40V	**V_{VREQ} * 110%**

The OVP debounce time mechanism is to prevent false triggering caused by various spurious noises. The OVP debounce time is preset to 30ms. If the VBUS voltage is greater than the OVP threshold voltage after the debounce time (30ms), the STATUS.OVP will be set to 1 and the associated VOUT MOS Switches are turned off. The host MCU will need to load new PD_CMDMSG to start a PD negotiation process to resume quick charging operation.

7.2 Over Current Protection (OCP)

The AP33772S triggers the OCP protection when the charging current is larger than OCP Threshold Current. Table bellow shows the correspondence between OCPTHR and OCP Threshold Current. The default value of the OCPTHR register is 00h.

After successful negotiation with the PD source, if the OCPTHR value is still 00h, the OCP Threshold Current should be updated to 110% of the maximum current (I_{MAX}) of the selected PDO/APDO.

If the OCPTHR value has been updated through I2C interface, the OCP Threshold Current should be updated to 110% of OCPTHR value.

OCPTHR	OCP Threshold Current
OCPTHR = 0	**I_{MAX} * 110%** (Note)
OCPTHR != 0	**I_{OCPTHR} * 110%**

Note:

I_{MAX}: The Maximum Current of PDO/APDO

The default OCP debounce time is 30ms. If the charging current is larger than OCP Threshold Current after debounce time (30ms), the STATUS.OCP will be set to 1 and the associated VOUT MOS Switches are turned off. The host MCU will need to load new PD_CMDMSG to start a PD negotiation process to resume quick charging operation.

7.3 Under Voltage Protection (UVP)

The AP33772S triggers the UVP protection when VBUS voltage is lower than UVP Threshold Voltage. Table bellow shows the correspondence between UVPTHR and UVP Threshold Voltage.

The default value of Under Voltage Protection Threshold (UVPTHR) is 80%, which can be modified by writing the UVPTHR command.

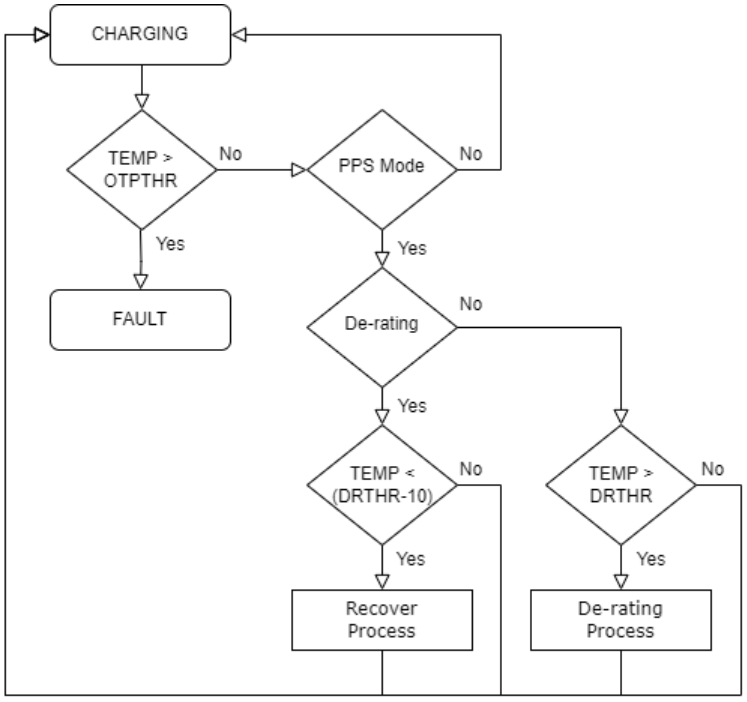
UVPTHR	UVP Threshold Voltage
1	V_{VREQ} * 80%
2	V_{VREQ} * 75%
3	V_{VREQ} * 70%

The default UVP debounce time is 30ms. If VBUS voltage is lower than UVP Threshold Voltage after debounce time (30ms), the STATUS.UVP will be set to 1 and the associated VOUT MOS Switches are turned off. The host MCU will need to load new PD_CMDMSG to start a PD negotiation process to resume quick charging operation.

7.4 Over Temperature Protection (OTP) and De-Rating

The host MCU could access the estimated temperature of a potential hot spot by accessing the TEMP register. A NTC thermistor is used to connect to OTP pin and ground nearby the potential hot spot. The host MCU must initialize the TR25, TR50, TR75 and TR100 registers before reading TEMP register or enabling OTP and power de-rating functions.

The default value of the OTPTHR register is 78h (120°C), which can be updated through I2C interface. If the TEMP value rises over the OTPTHR value after the de-bouncing time (30ms), the STATUS.OTP will be set to 1 and the associated VOUT MOS Switches are turned off. The host MCU will need to load new PD_CMDMSG to start a PD negotiation process to resume quick charging operation.



Furthermore, the AP33772S defines DRTHR register as threshold temperature value to trigger the power de-rating functions. If requested source PDO is PPS APDO, when TEMP value rises over DRTHR value after the de-bouncing time (30ms) the input current will be reduced by 50% through sending out a new RDO to negotiate with the PD source device.

AP33772S monitors the temperate at the potential hot spot continuously. After some time duration, if TEMP value under DRTHR value more than 10°C will recovers the charging power.

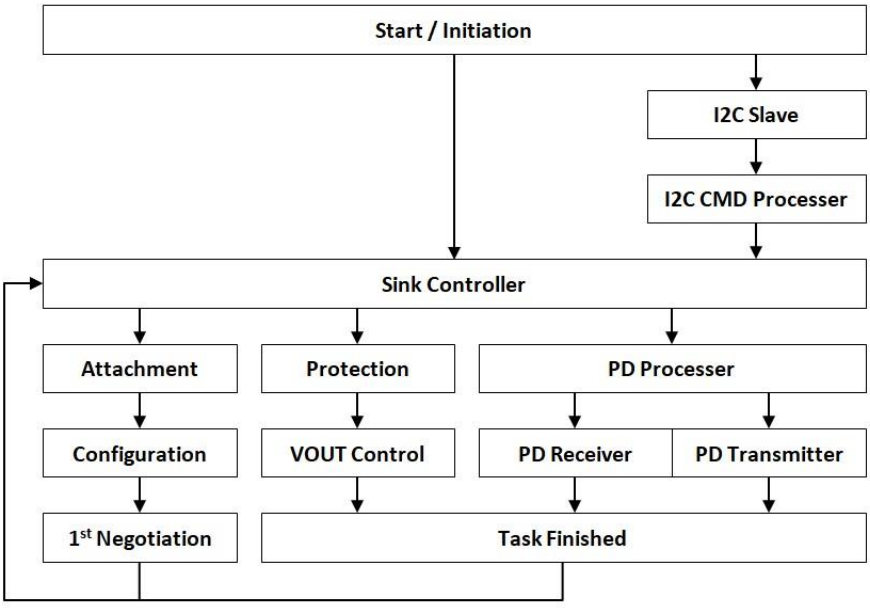
7.5 Moisture Detection

After connecting to the Power Source, AP33772S will first check whether the impedance of DN pin is abnormal. If the DN impedance check fails, the AP33772S goes into the MOISTURE state and does not acknowledge the Source Capability Messages.

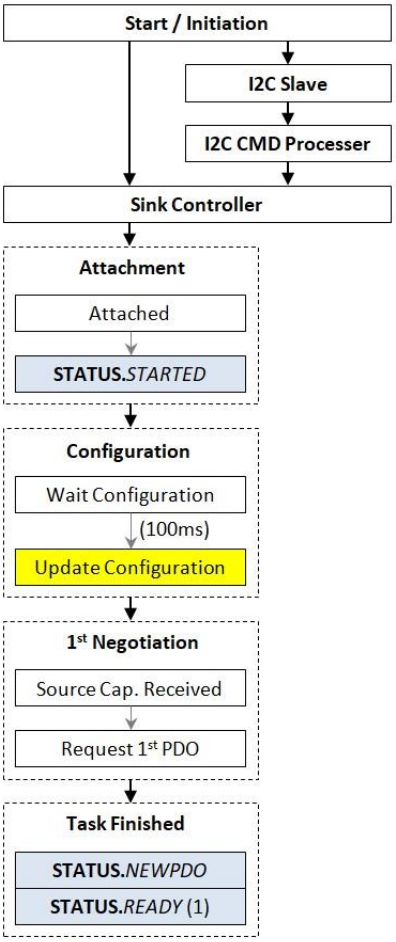
In MOISTURE state, the associated VOUT MOS Switches are turned off with LED flickering with the “MOISTURE” pattern and AP33772S will check the DN impedance ever 2200ms. If the impedance check of DN pin is normal, AP33772S start to negotiate with the source.

Chapter 8. Quick Start

8.1 Firmware Block Diagram



8.2 Firmware Startup Process



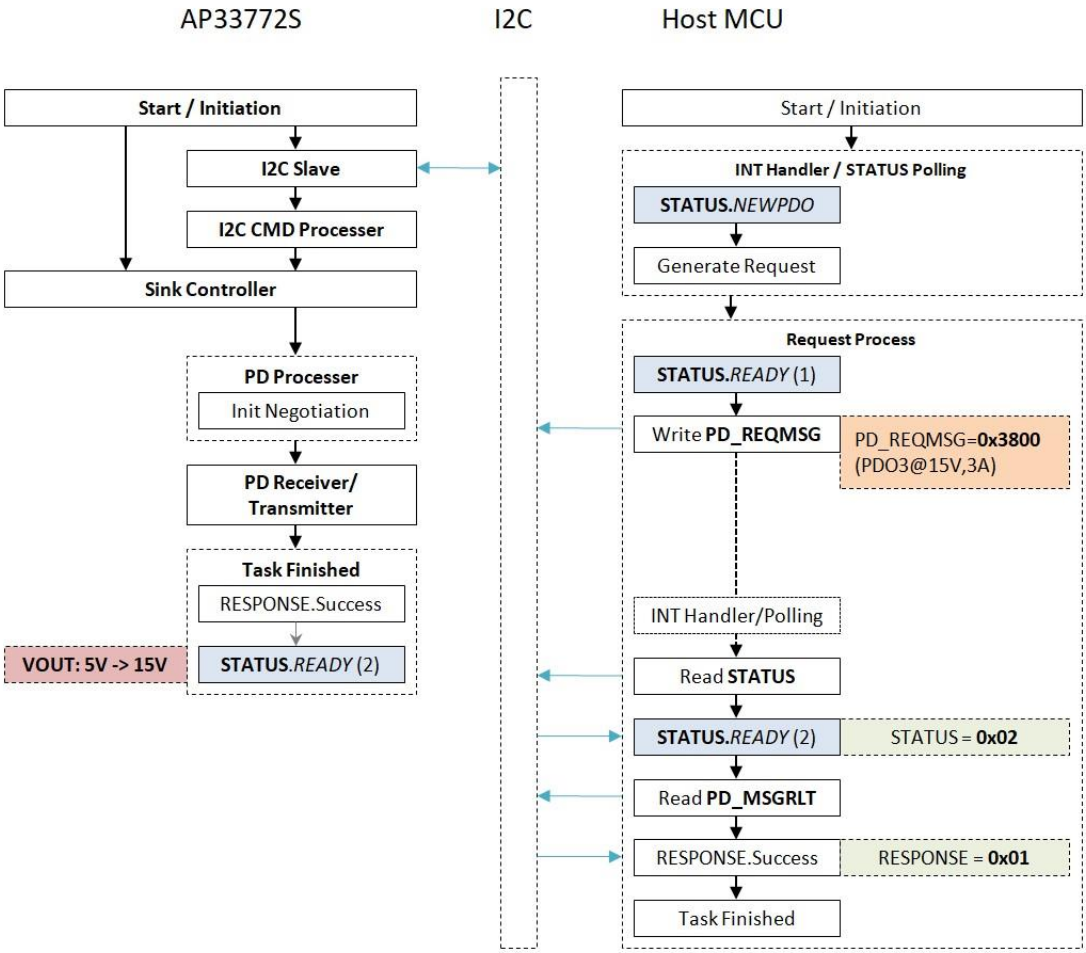
After AP33772S is powered on, the firmware begins to initialize the sink controller and I2C slave state machine. When the sink controller detects the VBUS and Rp is attached, the STATUS.STARTED flag is set to 1 and the interrupt signal is triggered through INT pin to the host MCU.

Once AP33772S is started (STATUS.STARTED = 1), the host MCU can disable/enable specific modules based on TCD requirements by writing the configurable registers. Then 100ms after AP33772S is started, the initial configuration is updated accordingly and the 1st negotiation with the PD source will begin.

After the 1st negotiation is completed, the source capabilities are stored in the SRC_SPR_PDO registers. If the PD source supports EPR mode, the EPR source capabilities are stored in the SRC_EPR_PDO registers. Then the STATUS.NEWPDO flag set to 1, indicating that the new source capabilities have been received. The host MCU should read the SRCPDO register and generate a request message (PD_REQMSG) based on the TCD requirements.

Finally, the STATUS.READY flag set to 1, indicating that the startup process is completed and the host MCU can send requests thereafter.

8.3 Request Process



For example, the energy sourcing side, the system uses a USB PD3.1 compliance charger (PDC), rated at 60W output power (5V/9V/15V/20V@3A). For the energy sinking side, a battery-powered Type-C mobile device adopts the AP33772S as the USB PD3.1 Sink compliance controller. The host appliance requests 45W power at 15V@3A input and starts charging after successful negotiation.

Based on the TCD requirements and the source capabilities obtained by reading the SRCPDO register and, the host MCU selects the required PDO_INDEX, CURRENT_SEL and VOLTAGE_SEL to generate the request message (PD_REQMSG).

After the AP33772S startup process is completed (STATUS.READY=1), the host MCU can initiate the request process through the I2C interface. Here PD_REQMSG is written to 3800h to request 45W power at 15V@3A. The request parameters are described in the following table.

PD_REQMSG	Bit	Attribute	Value	Description
PDO_INDEX	15:12	WO	3h	Select source PDO index “3”
CURRENT_SEL	8:11	WO	8h	Select Operating Current @3.00A
VOLTAGE_SEL	7:0	WO	0h	For fixed PDO selection, this parameter remains at 0

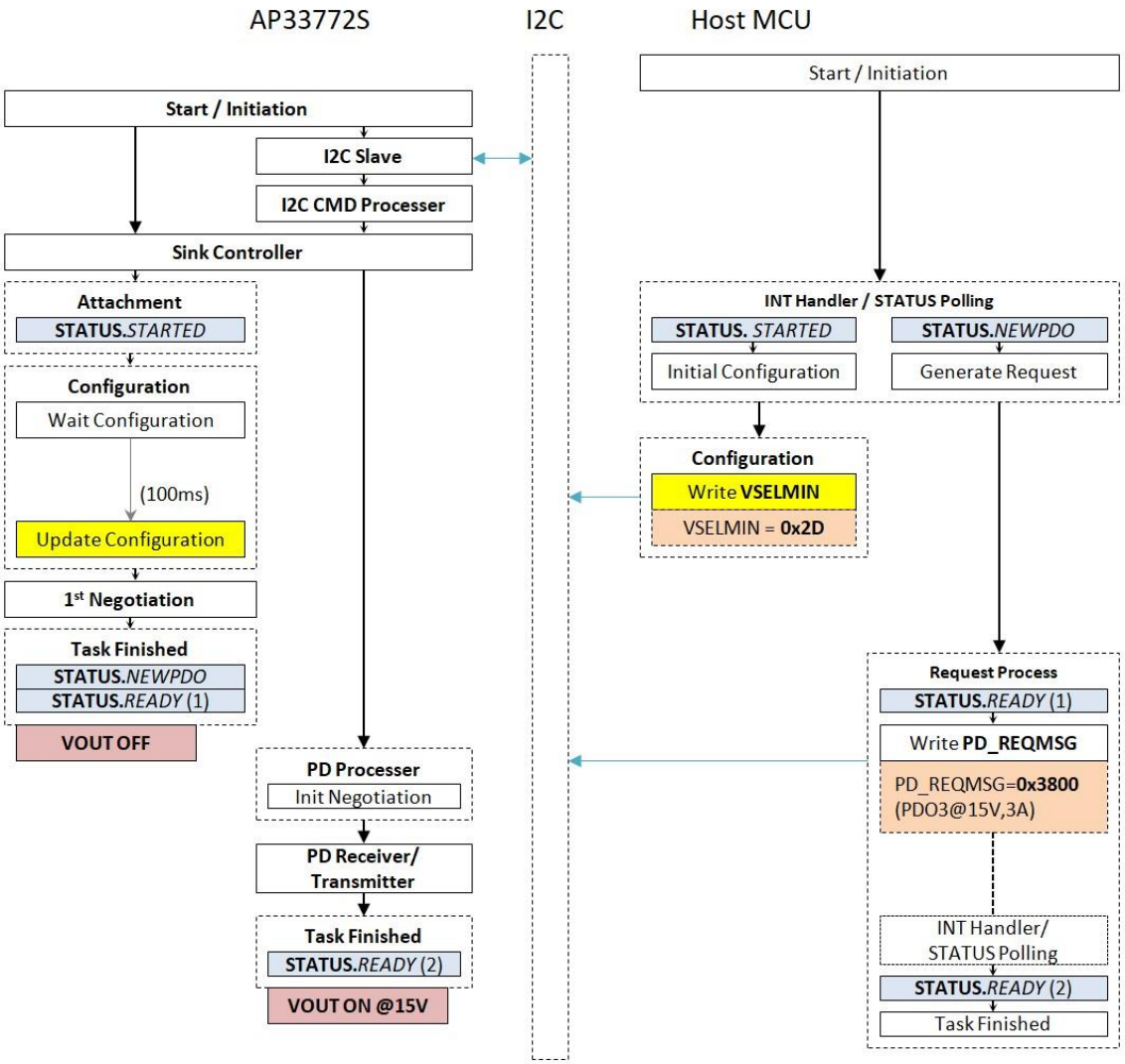
When receiving the PD_REQMSG command, AP33772S will initiate negotiation with the PD source according to the requirements of the host MCU. After the PD negotiation is completed, if AP33772S receives a PS_RDY message from the PD source, it sets the PD_MSGRLT.RESPONSE parameter to 1 (Success). Then the VOUT voltage transitions from 5V to 15V.

Finally, the STATUS.READY flag is set to 1, indicating that the request process is completed and the host MCU can send other requests/commands thereafter.

Therefore, the host MCU should handle the INT signal or poll STATUS to obtain the status of AP33772S in real time.

1. STARTED = 1, the host MCU can disable/enable specific modules by writing MASK, CONFIG, PDCONFIG and VSELMIN register at startup.
2. NEWPDO = 1, the host MCU should read the SRCPDO register to obtain the latest PD source capabilities, and then search for the appropriate PDO again.
3. READY = 1, the host MCU can send requests/commands or read/write any register through the I2C interface.
4. After writing to PD_REQMSG register, the host MCU should wait for STATUS.READY flag to be set high and then read PD_MSGRLT register to obtain the negotiation result.

8.4 Initial Configuration



Continuing the example from the previous section, the battery-powered host appliance requires the VOUT voltage higher than 9V to protect the circuit and requests 45W power at 15V@3A for charging.

The power-on value of VSELMIN is 19h (5000mV). Under the default configuration, if the VREQ voltage is more than or equal to 5000mV, AP33772S enables the VOUT MOS Switches. During the 1st negotiation, AP33772S requests the default PDO1@5V and the VREQ voltage set to 5V. Since VREQ voltage is equal to VSELMIN voltage, the VOUT MOS Switches turn “ON” and then VBUS is connected to VOUT. Therefore, the default output of AP33772S is 5V when connected to the PD source, which may damage this host appliance.

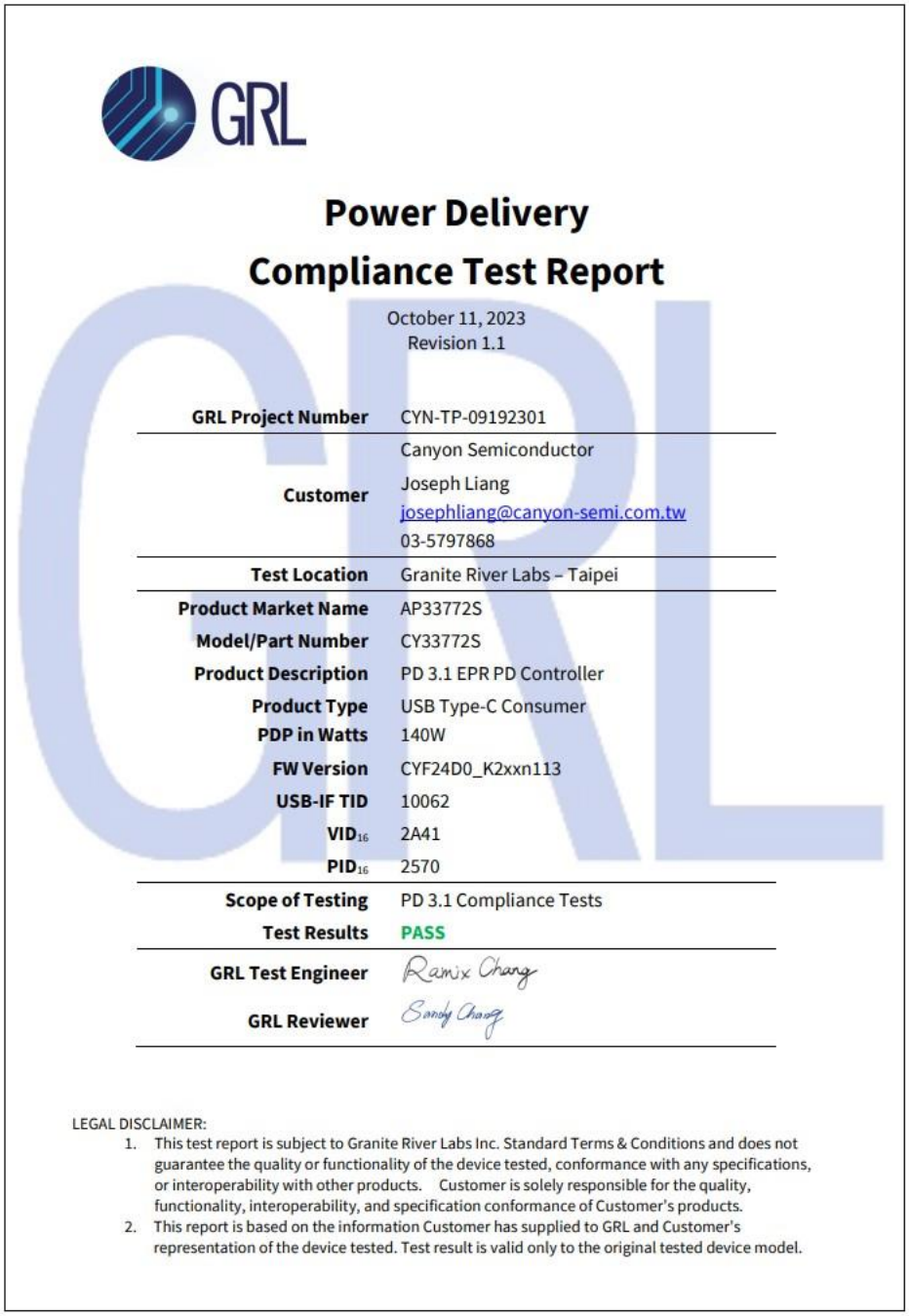
Once AP33772S is started (STARTED=1), the host MCU can change the power-on values of the configurable registers and the initial configurations will be updated accordingly after 100ms. For this custom application, the host MCU set VSELMIN to 2Dh (9000mV) during configuration. After the 1st negotiation is completed, the VOUT MOS Switches are turned “OFF” since VREQ voltage (5V) is less than VSELMIN voltage (9V).

Then the host MCU writes PD_REQMSG to 3800h to request 45W power at 15V@3A. After successful negotiation, the VOUT MOS Switches are turned “ON” since VREQ voltage (15V) is more than VSELMIN voltage (9V). By modifying the initial configuration, host appliance can ensure that VOUT voltage is always greater than 9V.

Chapter 9. Compliance test

Product Testing Information

- Product Name: AP33772S
- Model: CY33772S
- USB-IF TID: 10062



GRL

Power Delivery

Compliance Test Report

October 11, 2023
Revision 1.1

GRL Project Number	CYN-TP-09192301
Customer	Canyon Semiconductor Joseph Liang josephliang@canyon-semi.com.tw 03-5797868
Test Location	Granite River Labs – Taipei
Product Market Name	AP33772S
Model/Part Number	CY33772S
Product Description	PD 3.1 EPR PD Controller
Product Type	USB Type-C Consumer
PDP in Watts	140W
FW Version	CYF24D0_K2xxn113
USB-IF TID	10062
VID_{16}	2A41
PID_{16}	2570
Scope of Testing	PD 3.1 Compliance Tests
Test Results	PASS
GRL Test Engineer	Ramix Chang
GRL Reviewer	Sandy Chang

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2. This report is based on the information Customer has supplied to GRL and Customer's representation of the device tested. Test result is valid only to the original tested device model.

Chapter 10. Revision History

Item NO	Hardware Version	Firmware Version	Change Description	Date
1	1.0	1.0	1st Release	11/14/2023
2	1.0	1.1	Remove VDC	05/03/2024

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