Quick Start Guide:

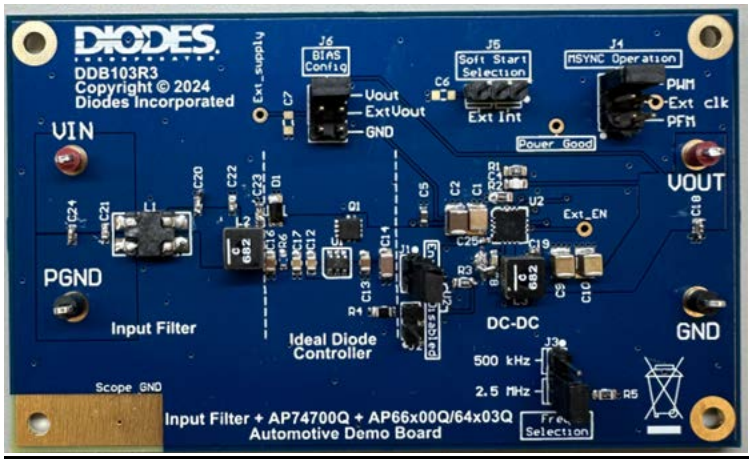


Figure 1: DDB103R3 Demo Board

Pin	Description
Vin	3.8V – 60V Supply In
GND	Common PCB ground
PGND	PCB Input GND
Vout	Output voltage (5V)
J1	Enable device using jumper
J2	Disable device using jumper
J3	Configures switching frequency to 500 kHz or 2.5 MHz using jumpers.
J4, ExtClk	Configures the MSYNC operation to PWM, PFM or External Clock operation using jumpers
J5	Configure internal or external soft start using jumpers
J6	Configures BIAS pin to Vout, PGND or external voltage source (using ExtSupply)
Ext_EN	Connect external voltage source on the enable pin

Table 1: DDB103R3 Pin Description

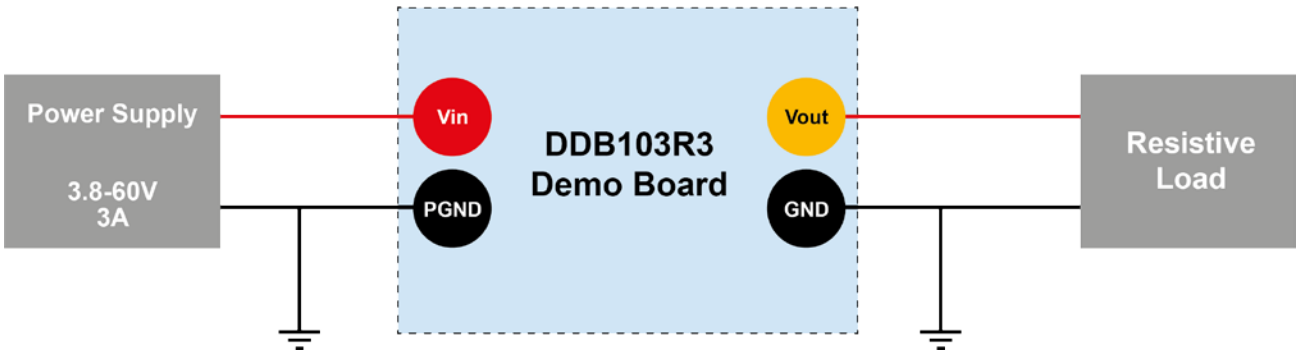


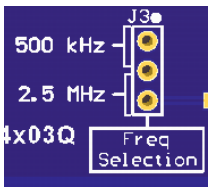
Figure 2: DDB103R3 Demo Board Test Setup

The DDB103R3 demo board has a simple layout and allows access to the appropriate signals through test points. To evaluate the performance of the DDB103R3, follow the procedure below:

1) Set jumpers to default positions. For more information about jumper configuration, please see page 2.
2) Connect a DC power supply between the VIN and GND terminals.
3) Connect the load to the VOUT and GND terminals.
4) Check all connections, then turn on the power supply.
5) The EVM board should now power up with a 5V output voltage.

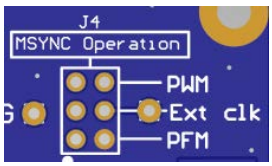
Jumper Configuration:

Note: A pale-blue row indicates the default jumper position.

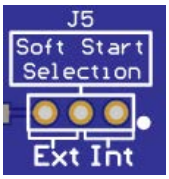


J1/J2	Effect on DDB103R3
Header on J1	Enables the AP66x00Q/AP64x03Q device
Header on J2	Disables the AP66x00Q/AP64x03Q device
Neither/Both Connected	Not recommended

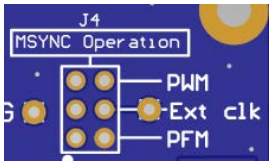
J3	Effect on DDB103R3
Header on pin 1 and 2	Switching frequency of the AP66x00Q/AP64x03Q set to 500 kHz
Header on pin 2 and 3	Switching frequency of the AP66x00Q/AP64x03Q to 2.5MHz
Neither/Both Connected	Not recommended



J4	Effect on DDB103R3
Header on top 2 (horizontal) pins	MSYNC to forced PWM (VCC) operation
Header on middle 2 (horizontal) pins	MSYNC to an external clock source on MSYNC pin for synchronization with positive edge trigger and PWM.
Header on bottom 2 (horizontal) pins	MSYNC to PFM (GND) operation
Neither/Both Connected	Not recommended



J5	Effect on DDB103R3
Header on left 2 (horizontal) pins	Connect GND through capacitor for default external soft start
Header on right 2 (horizontal) pins	Connect VCC for internal soft start of 1.7ms
Neither/Both Connected	Not recommended



J6	Effect on DDB103R3
Header on top 2 (horizontal) pins	Connect BIAS pin to VOUT
Header on middle 2 (horizontal) pins	Connect an external voltage source on BIAS pin (<15 V)
Header on bottom 2 (horizontal) pins	Connect BIAS pin to PGND
Neither/Both Connected	Not recommended

Description:

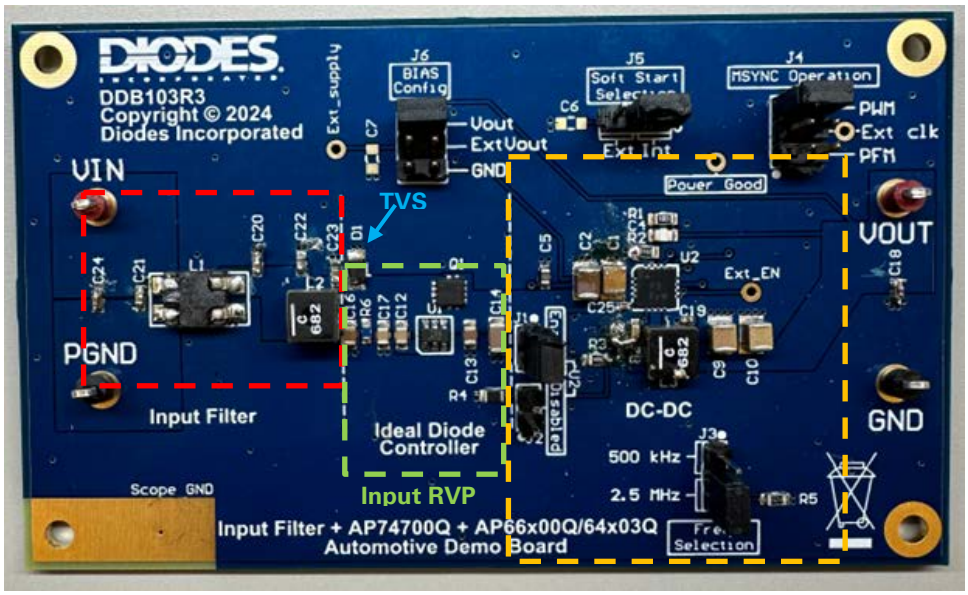


Figure 3: Picture of the DDB103R3 Demo Board

The DDB103R3 Demo Board showcases the **AP66x00Q/AP64x03Q** 3A DC-DC buck converter, the **AP74700Q** ideal diode controller, and an EMI input filter. It demonstrates a system-level solution with reverse voltage protection, **ISO 7637-2** transient pulse protection (using a suitable TVS), EMI filtering that passes **CISPR 25 Class 5**, and the DC-DC buck converter.

The input filter (as shown in figure 3 within the red square) contains a common mode choke with capacitors on either side in a Pi configuration. This is connected in series with an LC low pass filter containing an inductor and a capacitor. This combination makes the board CISPR 25 class 5 compliant.

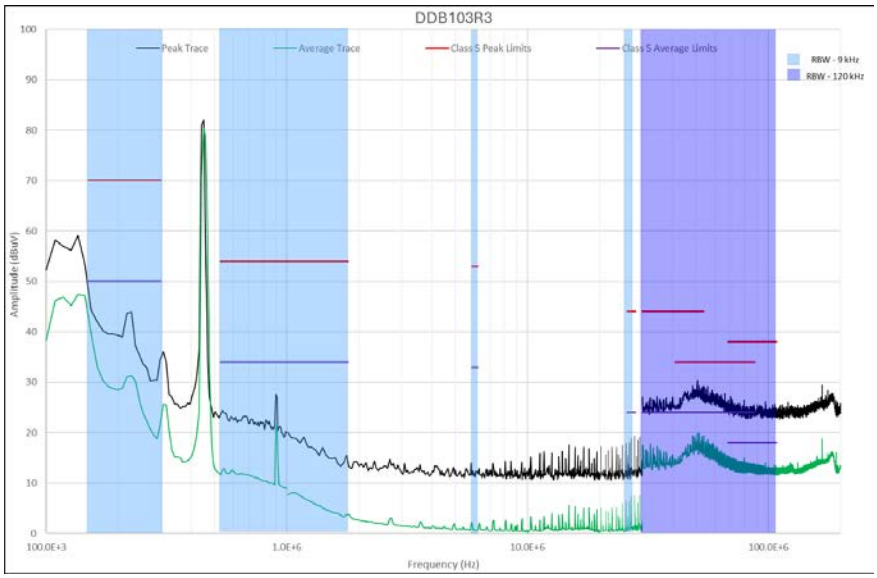


Figure 4: EMC Sweep of DDB103R3 from 100 kHz – 200 MHz, 13.5V_{in}, 3A load, against CISPR 25 Class 5 limits

The TVS is highlighted in light blue; this provides the board with ISO7367-2 pulse protection (the SMF4L30CAQ, for example, is a suitable choice).

The input RVP section of the board is highlighted in green and consist of the **AP74700Q**.

Description (continued):

The AP74700Q is a ±65V ideal diode MOSFET controller which provides a low-loss 20mV forward voltage drop rectifier in unidirectional power paths, as well as reverse voltage. The AP74700Q supports a wide input operation range from 3.2V to 65V, allowing control of many popular DC rail voltages such as 12V, 24V, or higher automotive battery systems. The 3.2V input voltage support fits for severe cold crank requirements in automotive systems. The AP74700Q can withstand and protect the loads from reverse voltages down to -65V.

The MOSFET design requirements of the AP74700Q are:

- 60V $V_{DS(MAX)}$ and ±20V $V_{GS(MAX)}$
- $R_{DS(ON)}$ @$I_{Load(Nominal):}$ (20 mV/ $I_{Load(Nominal)}$) ≤ $R_{DS(ON)}$
- MOSFET gate threshold voltage V_{TH}: 2V maximum

Due to the DDB103R3's 3x3 footprint and the AP74700Q's design requirements, the DMTH6016LFVWQ is the best choice of MOSFET (Q1).

The **AP66x00Q/AP64x03Q** (highlighted in yellow) are adjustable switching frequency, internally compensated, synchronous DC-DC buck converter families. The AP66x00Q family has a V_{IN} range of 3.8V-60V, and the AP64x03Q family has a V_{IN} of 3.8V-40V. The AP66x00Q/AP64x03Q device families fully integrate a high-side power MOSFET and low-side power MOSFET to provide high-efficiency step-down DC-DC conversion.

The AP66x00Q/AP64x03Q enables continuous load currents of up to 2A/3A, with efficiency as high as 95%. It features current mode control operation, which enables easy loop stabilization supporting a wide range of capacitive loads. The AP66x00Q/AP64x03Q simplifies board layout with its high level of integration and minimal external components.

The AP66x00Q/AP64x03Q is available in the U-QFN4040-16/SWP package.

Schematic Diagram:

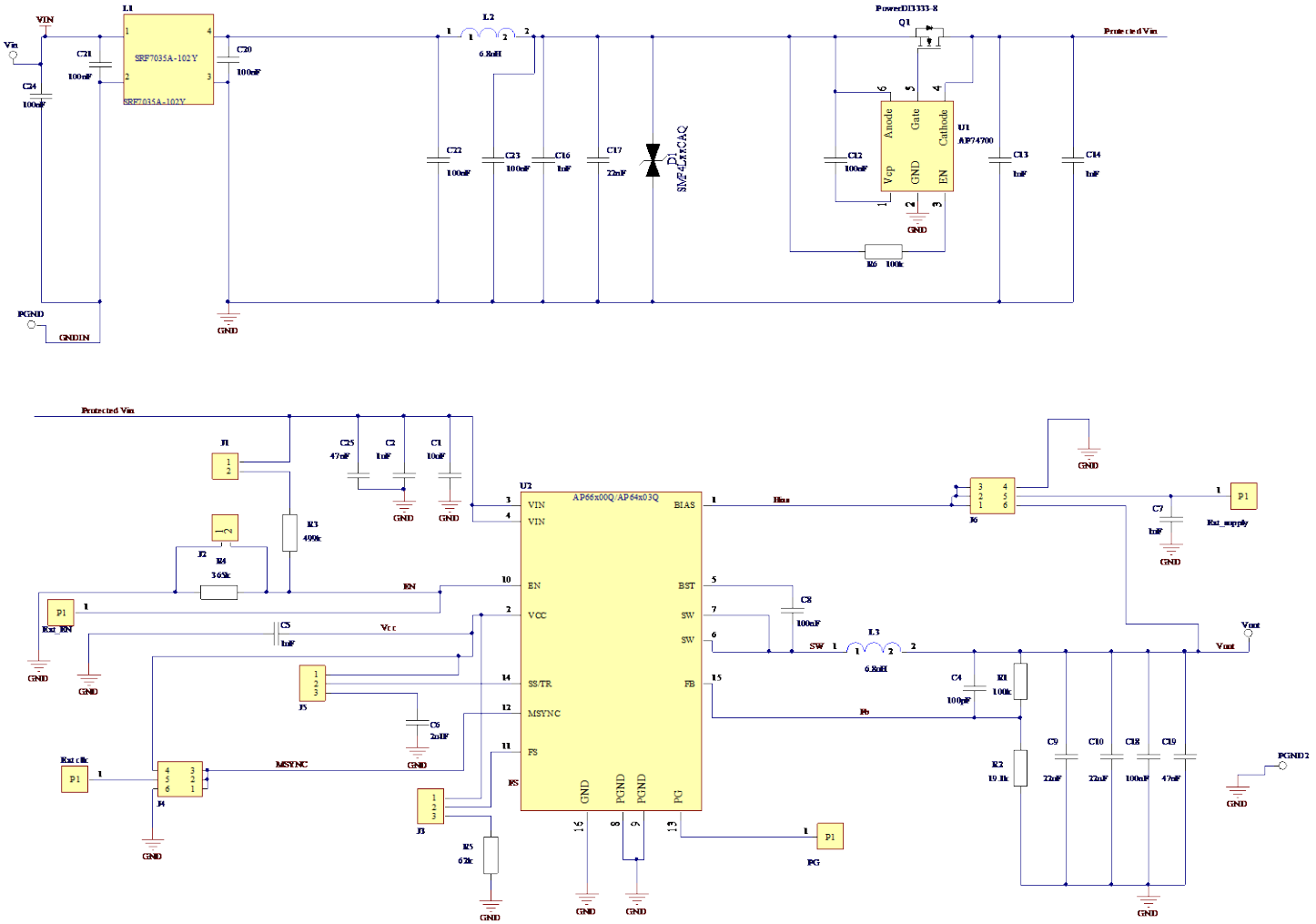
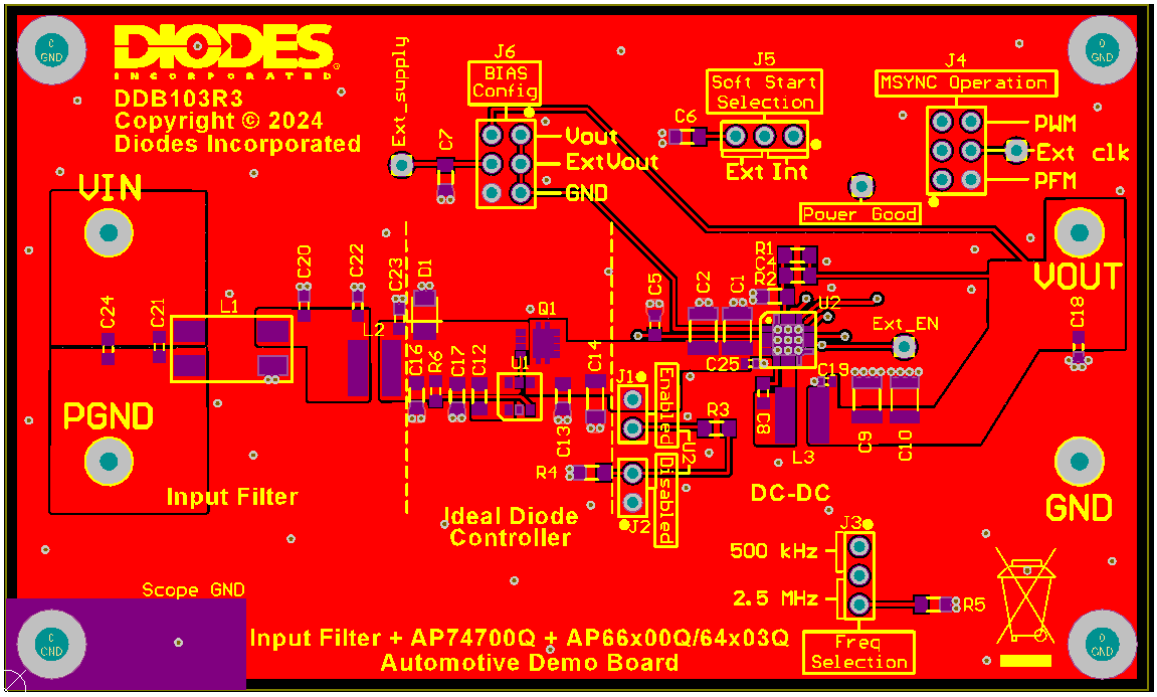


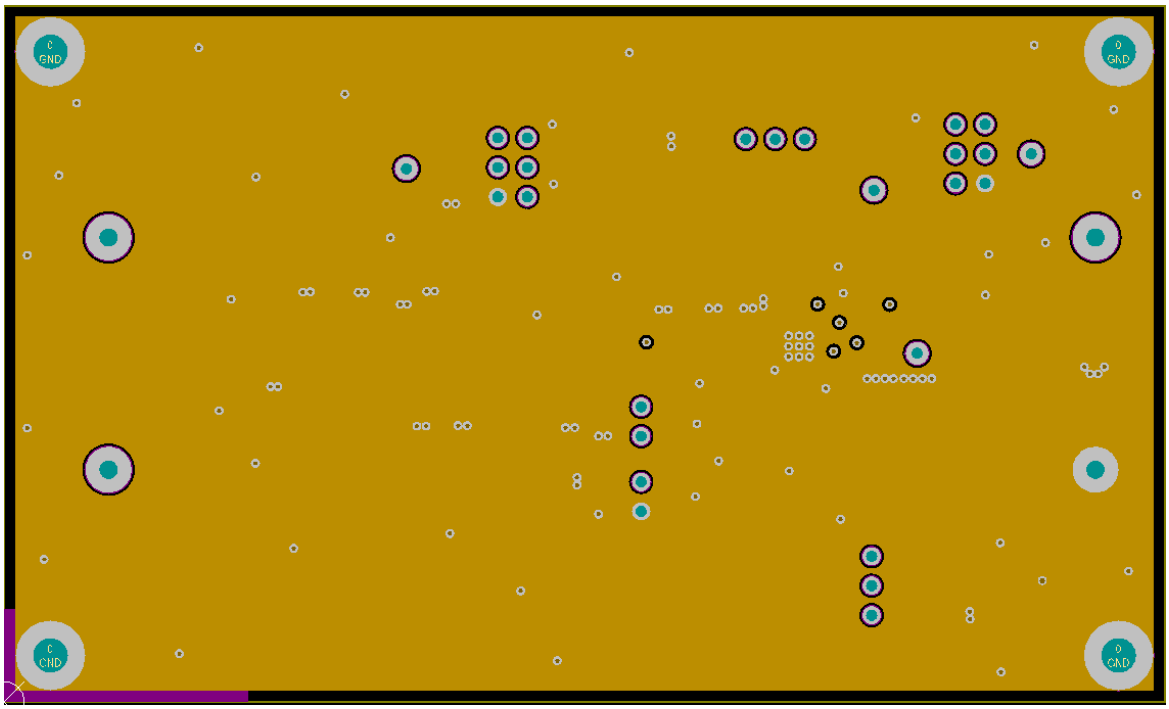
Figure 5: Schematic Diagram of the DDB103R3 Demo Board

Board Layers (top view):

Top Layer:

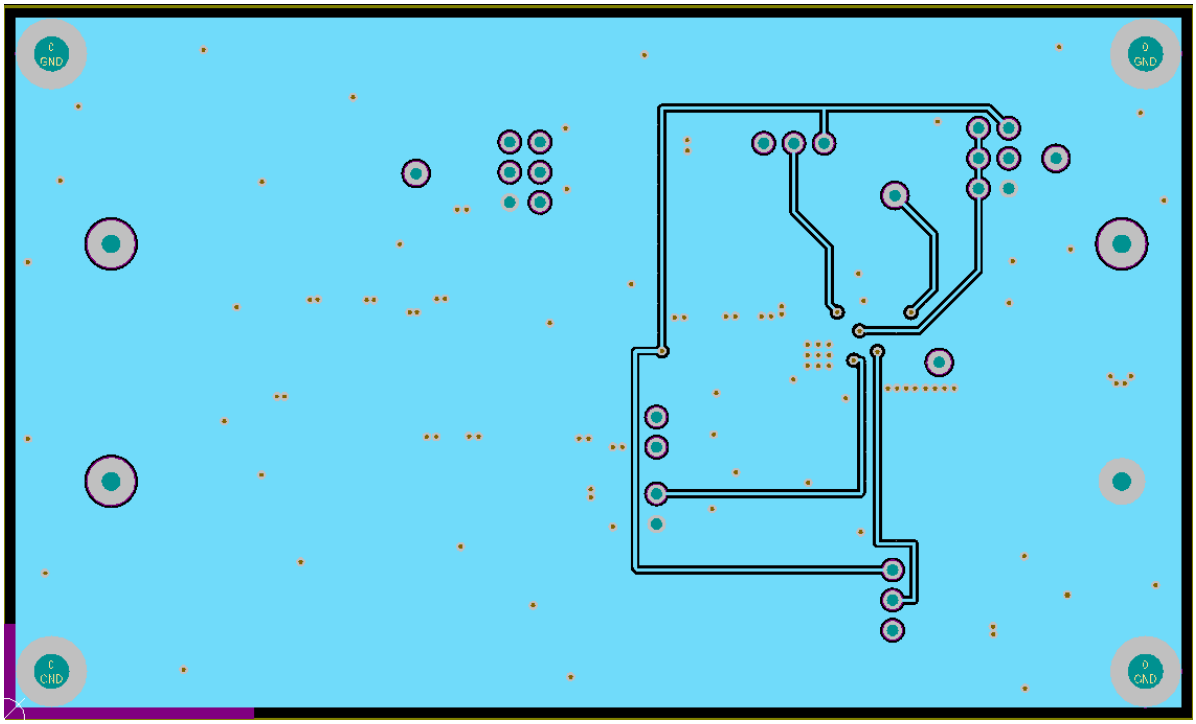


Mid Layer 1:

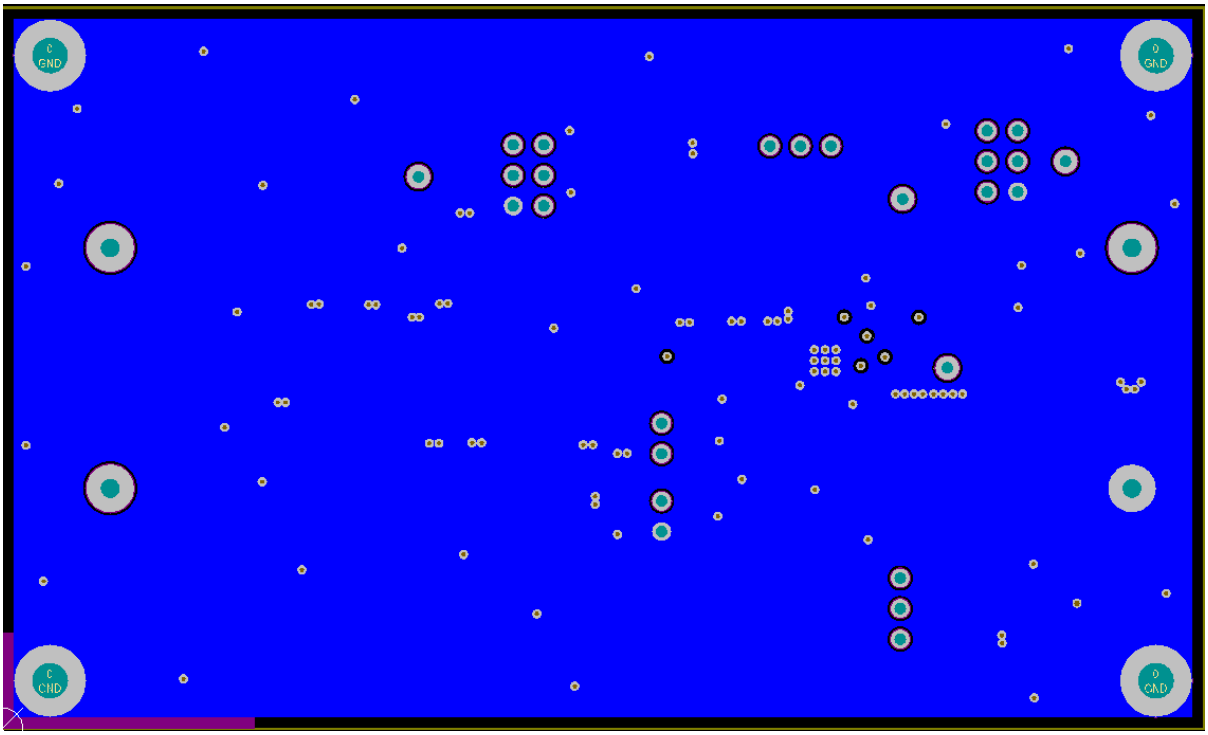


Board Layers (top view) (continued):

Mid Layer 2:



Bottom Layer:



BILL OF MATERIALS for DDB103R3 EVM:

Quantity	Idents	Description	Footprint
1	U2	AP66x00Q/AP64x03Q	U-QFN4040-16/SWP
1	U1	AP74700Q	SOT26
1	Q1	DMTH6016LFVWQ	PowerDI3333-8
1	D1	SMF4Lxx(C)AQ	DO-219AA
1	C1	10uF X7R Ceramic SMD Capacitor	1210
1	C2	1uF X7R Ceramic SMD Capacitor	1210
2	C9, C10	22uF X7R Ceramic Capacitor	1210
1	C12	100nF X7R Ceramic Capacitor	0805
1	C4	100pF X7R Ceramic Capacitor	0805
1	C17	22nF X7R Ceramic Capacitor	0805
2	C22, C23	47nF X7R Ceramic Capacitor	0603
1	C6	2.2uF X7R Ceramic SMD Capacitor	0805
3	C7, C13, C16	1uF X7R Ceramic SMD Capacitor	0805
3	C5, C21, C20	1uF X7R Ceramic SMD Capacitor	0603C
4	C8, C1, C24, C18	100nF X7R Ceramic SMD Capacitor	0603C
4	ExtClk, ExtSupply, ExtSupply1	1 pin header	0.1” 1W
2	J1, J2	2W header	0.1” 2W
2	J3, J5	2W header	0.1” 2W
2	J4.J6	6W header	0.1” 6W
1	L1	Common-mode Choke, BOURNS SRF7035A-102Y	7mm x 6mm x 3.5mm
1	L2	Coilcraft XGL5050-682MEC, 6.8uH, 6.2A	5050
1	L3	Coilcraft XGL5030-682MEC, 6.8uH, 5.5A (500 kHz) Coilcraft XGL4030-122MEC, 1.2uH, 9A (2.5 MHz)	5030/4030
5	R1, R2, R3, R4, R5	Resistor	0805
4	Vin, Vout, PGND, GND	Test eyelets	1.6mm test eyelets

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