PI3TB212
PI3TB212 Thunderbolt Application Information

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1 Introduction

PI3TB212 is a Thunderbolt® (TB) and DisplayPort Rev 1.2 mux or de-mux switch, which supports up to 10.3125Gbps data rate. PI3TB212 also implement the AUX and DDC MUX for the Dual-mode DP signaling. In this application information, the external components of the typical host application circuit and layout guideline are described.

2 External Component Requirements

2.1 AC Coupling Capacitors on high speed lanes

According to Thunderbolt™ Interconnect Specification, the high speed electrical interface must be AC-coupled. The AC-coupling capacitors on the transmit path & receive path is different.

	Min	Max
Transmit path	0.17uF	0.3uF
Receive path	0.34uF	0.6uF

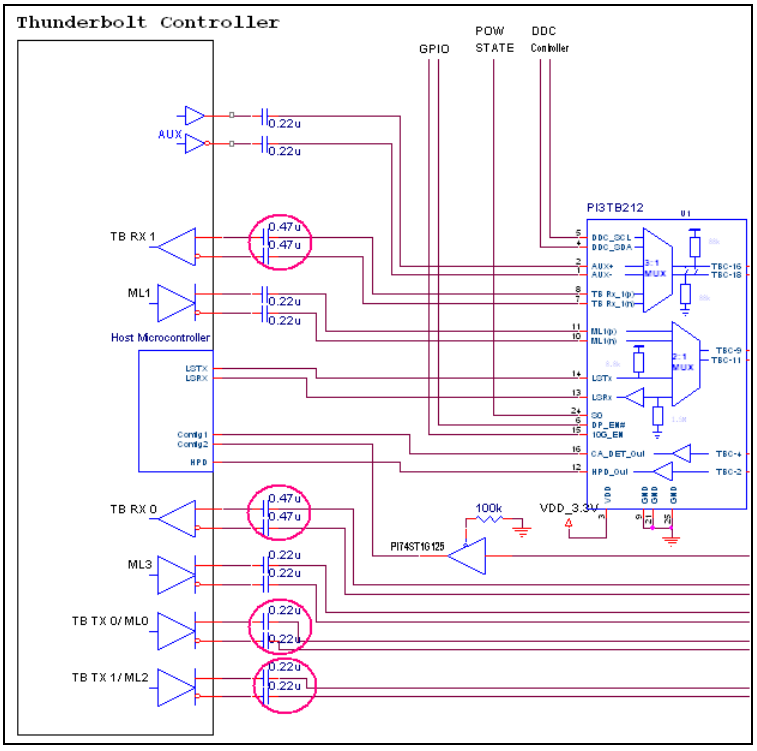


Figure 1: AC coupling capacitors at high speed lanes

2.2 Pull-down Resistor on HPD, Config1, Config2

Thunderbolt connector is designed compatible with mini DP connector (mDP). It is used to carry the Thunderbolt protocol, but also retains the capability to carry the native DisplayPort signal. To determine whether the connection should operate as a Thunderbolt Technology link or as a native DisplayPort link, the thunderbolt host will detect the HPD, Config1, Config2 and LSRX signal after the device is attached.

Mode	HPD	Config1	Config2	LSRX
Thunderbolt	LOW	LOW	HIGH	HIGH
DisplayPort	HIGH	LOW	LOW	X
HDMI	HIGH	HIGH	HIGH	X
DVI	HIGH	HIGH	X	X

According to the specification, these pins must have pull-down resistors.

	Min	Max
HPD	100kΩ	
Config1, Config2	0.95MΩ	1.05MΩ
LSRX	0.7MΩ	1.05MΩ

PI3TBT212 have the internal 1MΩ pull-down resistor on LSRX pin and no need to place the external one.

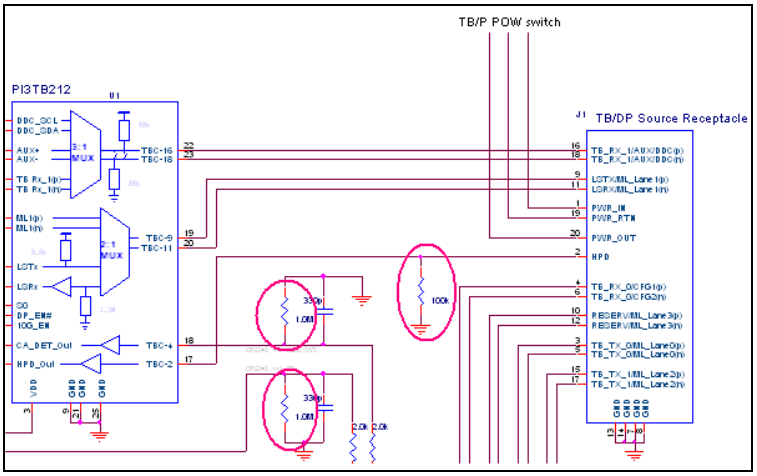


Figure 2: Pull-down resistors on the HPD, Config1 & Config2 pins

3 Layout Design Guideline

Layout guideline especially for high-speed transmission is highlighted.

3.1 Power and GROUND

To provide a clean power supply for PI3TB212, few recommendations are listed below.

- Power (VDD) and ground (GND) pins should be connected to corresponding power planes of the printed circuit board directly. The distance from each VDD or GND pin to the plane should be less than 50mil.
- The thickness of the PCB dielectric layer should be minimized such that the VDD and GND planes create low inductance paths.
- One low-ESR 0.1uF decoupling capacitor should be mounted at each VDD pin or should supply bypassing for at most two VDD pins. Smaller body size capacitors can facilitate component placement. The capacitor should be placed next to a VDD pin, i.e. within 100mil.
- One capacitor with capacitance in the range of 4.7uF to 10uF should be incorporated in the power supply decoupling design as well. It can be either tantalum or an ultra-low ESR ceramic.
- A ferrite bead for isolating the power supply for Pericom device and power supplies for other parts of the printed circuit board should also be implemented.

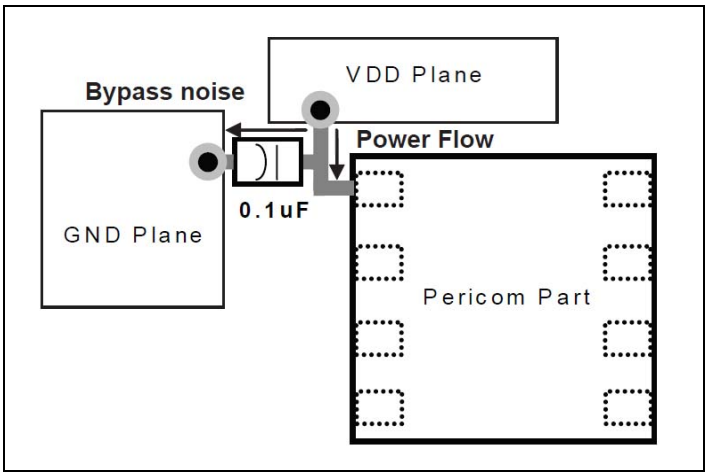
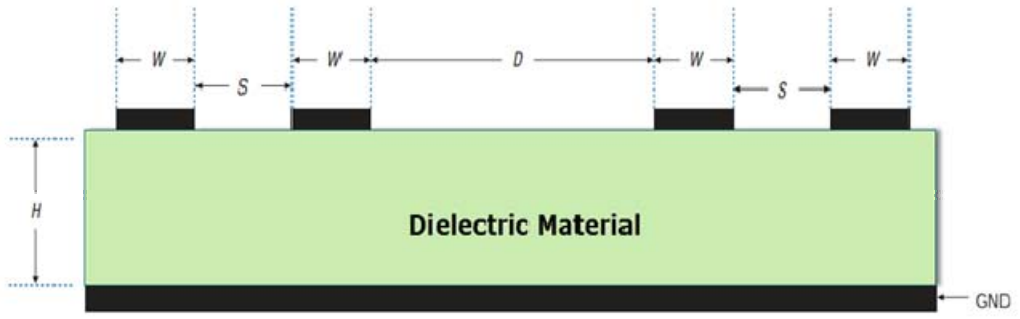


Figure 3: Decoupling Capacitor Placement Diagram

3.2 High-speed Signal Routing

As data rate is getting higher, good layout is essential to prevent signal from reflection.

- There are multiple 10Gbps differential signal pairs in the interface. To maximize the signal integrity using microstrip traces, make sure the distance between 2 differential pairs D is greater 2S (S is the separation between the differential signal) to minimize the crosstalk between the two differential pairs. Refer to the figure for the details of the geometry.



D = Distance between two differential pair signals;
W = Width of a trace in a differential pair;
S = Distance between the trace in a differential pair;
H = Dielectric height above the group plane.

Figure 4: PCB cross-section Geometries

- Differential pair should maintain symmetrical routing whenever possible. The intra-pair skew should be less than 5 mils.

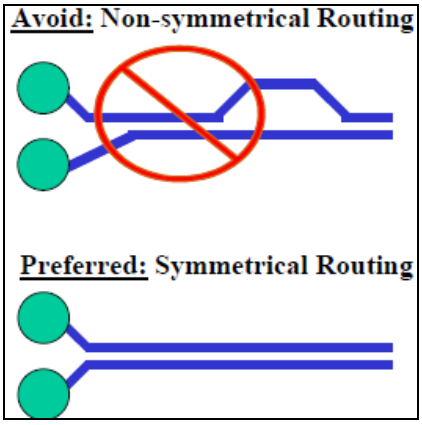


Figure 5: Layout Example of Differential Pair

- Wider trace width of each differential pair is recommended in order to minimize the loss, especially for long routing.
- For minimal coupling, isolation spacing between two differential pairs should be maximized. At least 3 times the spacing of one differential pair is recommended.

- Differential signals should be routed away from noise sources and other switching signals on the printed circuit board.
- It is preferable to route differential signals on the same layer of the printed circuit board, particularly for the input traces in source application.
- Stub creation should be avoided when placing shunt resistors on a differential pair.

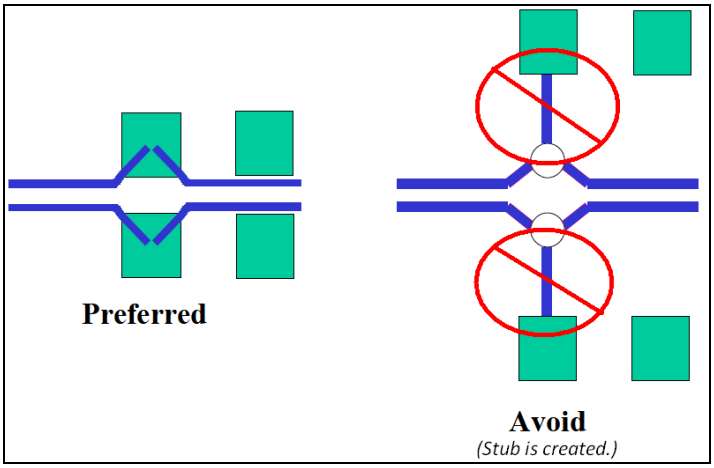


Figure 6: Shunt Resistor Placement

The "Config1" & "Config2" signals are sharing the same trace of the 10Gbps RX differential signal. According to the specification, the 2.0kohm series resistors, 1Mohm shunt resistors and a shunt capacitor are place between RX difference trace & the Config1/Config2 trace. If the placement of these components creates the shunted stub, the 10Gpbs signal quality will be affected by these stubs.

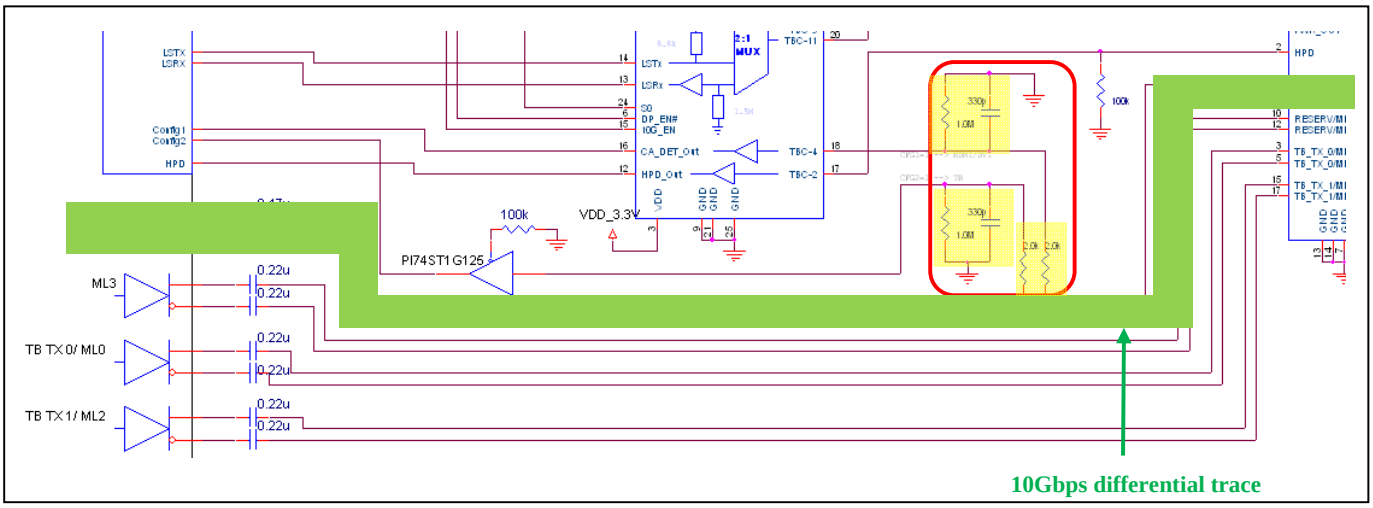


Figure 7: Components on Config1, Config2 and RX0 signal

Below is the suggestion of the components placement.

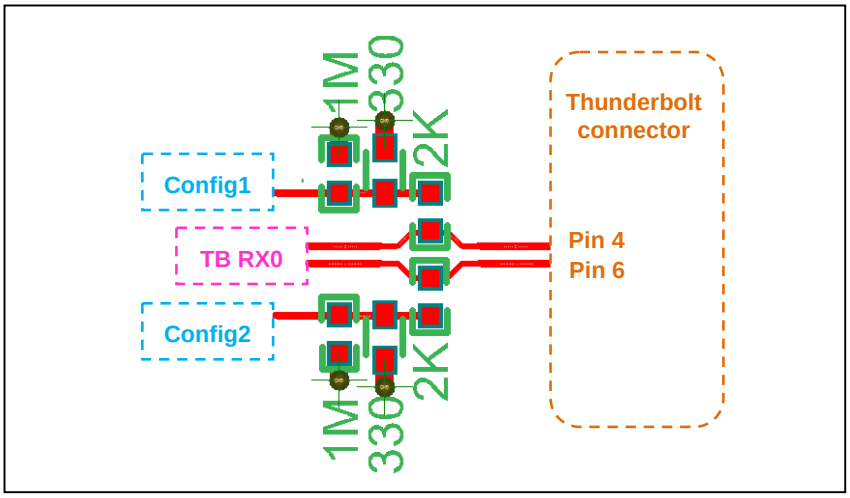


Figure 8: Components placement example of Config1, Config2 and RX0 signal Differential trace

- To minimize signal loss and jitter, tight bend is not recommended. All angles should be larger than or equal to 135 degrees.

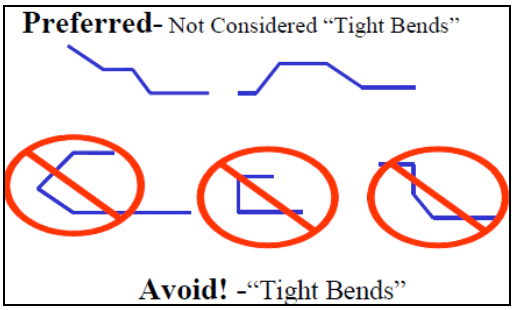


Figure 9: Acceptable Bends vs. Tight Bends

- AC coupling capacitor placement should be symmetrical.

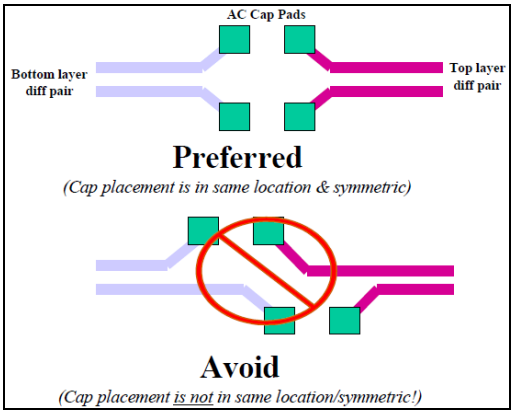


Figure 10: AC Capacitor Placement

- The use of vias should be avoided if possible. If using vias is a must, they should be used sparingly and must be placed symmetrically on a differential pair.

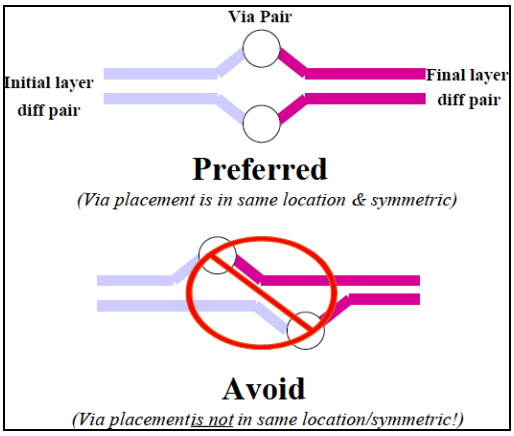


Figure 11: Via Placement

4 Typical Application Circuit

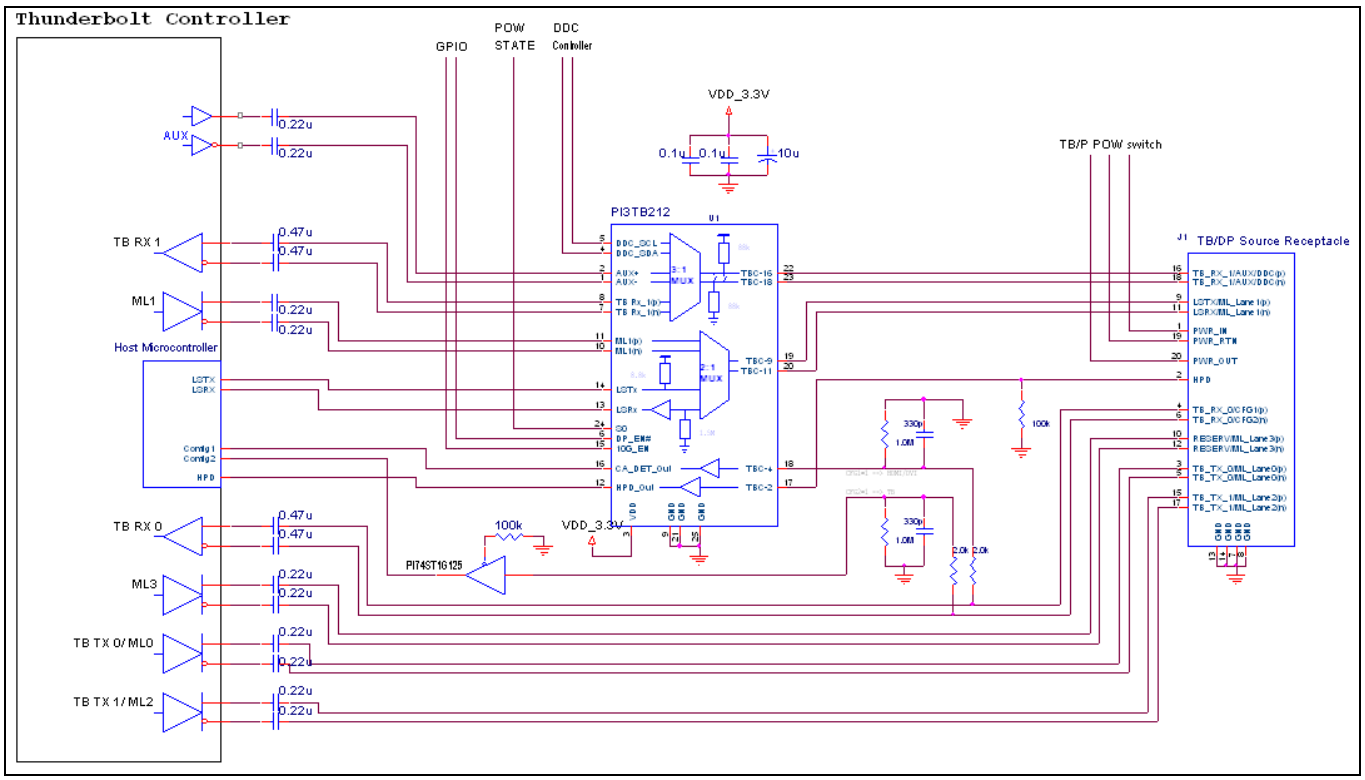


Figure 12: PI3TB212 Thunderbolt Source Application

5 Relative References

(1) Thunderbolt Interconnect Specification, June, 2012
(2) PCI Express Board Design Guidelines Draft, Intel Corporation, June 2003