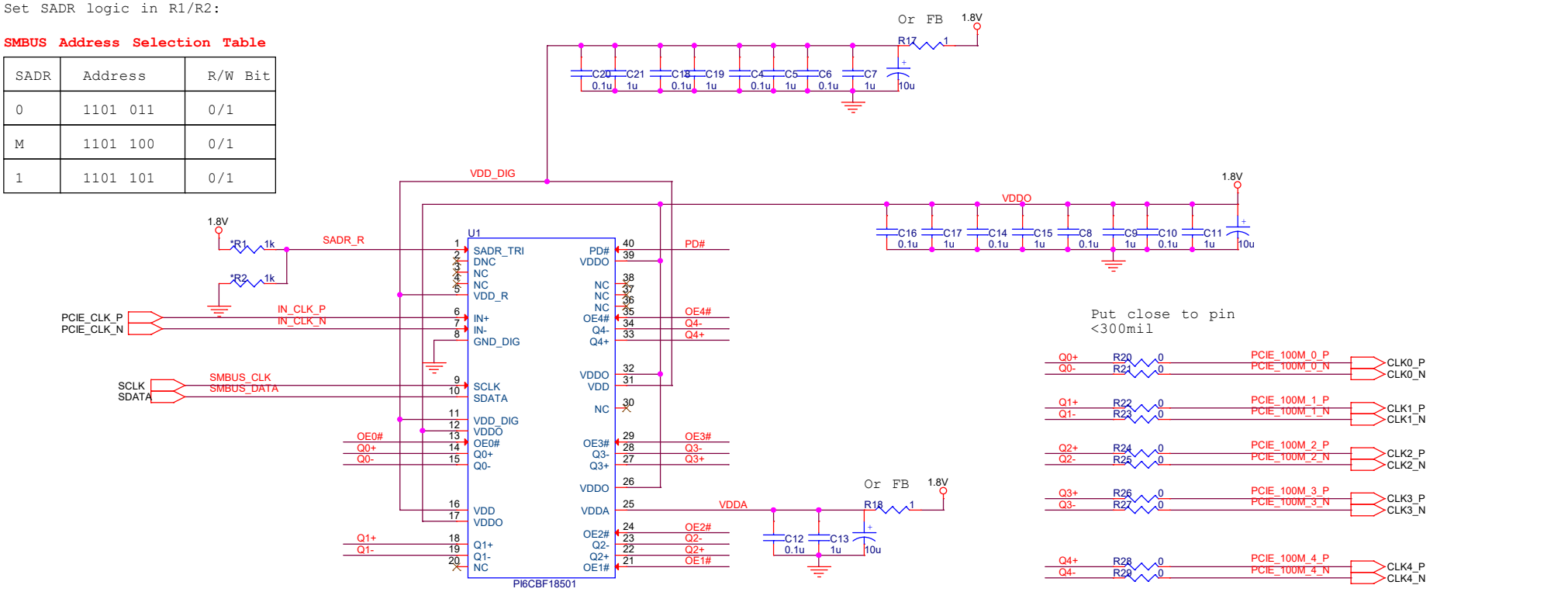
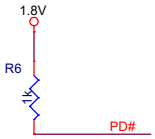
Set SADR logic in R1/R2:

SMBUS Address Selection Table

SADR	Address	R/W Bit
0	1101 011	0/1
M	1101 100	0/1
1	1101 101	0/1





OE0#

Make individual OEx# pull-up/down to enable/disable each output

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OE4#

App Note:

1. Each VDD pin needs 0.1u +1uF decoupling close to pin. (e.g.: VDD, VDDA, VDD_R...etc)
2. VDDA use small R=1~2 ohm or FB(ferrite bead)+C=10uF filtering for better DC/DC ripple noise rejection
3. This is LP_HCSL type output: serial 0ohm R is optional, but it can be replace in 5 to 15 ohm for the optimal fine tune the board RX end wavefrom for different trace length if needed
4. Note SMBUS address is power on latch once set;
5. Make LVDS clock, it needs AC coupling and then RX side use pull-up/down Rs to bias LVDS level, refer to datasheet;
6. OEx# pins have internal pull-down
7. Connect epad in 6 to 8 vias to GND plane

Title: PI6CBF18501 App. Schematic		
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