# ZXCT210 PSpice

# Model Validation Report

20/02/2024

# Version History

## ZXCT210

| Version | Details | Author | Date | REMARKS |
|---|---|---|---|---|
| 1.0 | PSpice Results | Sankalp | 24JAN2024 | Initial Release |
| 1.1 | PSpice Results | Sankalp | 20FEB2024 | Updated Results:-<br>i) Offset voltage vs Temperature<br>ii) Input bias currents vs Common mode volatge |

# Contents

# Spec Compliance Matrix

| PARAMETER | SYMBOL | TEST CONDITION | DATASHEET VALUE | | | PSPICE VALUE | UNIT |
|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | | |
| Common-Mode Input | VCM | TA = -40°C to +125°C | -0.3 | -- | 26 | (-0.3)-26 | V |
| Common – Mode Rejection | CMRR | VIN+ = 0V to 26V, VSENSE = 0mV,<br>TA = -40°C to +125°C | 100 | 120 | -- | 118 | dB |
| Offset voltage | VOS | VSENSE = 0mV | -- | +-0.55 | +-35 | +-35 | uA |
| Vos vs Temperature | dVos/dT | TA = -40°C to +125°C | -- | 0.1 | -- | 0.1 | uV/°C |
| Power supply rejection | PSRR | VS = 2.7V to 18V, VIN+ = 18V, VSENSE = 0mV | -- | +-0.1 | +-10 | +-0.1 | uV/V |
| Input bias current | IB | VSENSE = 0mV | -- | 28 | 35 | 28 | uA |
| Gain | G | -- | -- | 200 | -- | 200 | V/V |

# Spec Compliance Matrix

| PARAMETER | SYMBOL | TEST CONDITION | DATASHEET VALUE | | | PSPICE VALUE | UNIT |
|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | | |
| Gain Error | EG | A and B Version, VSENSE = -5mV to 5mV, TA = -40°C to +125°C | -- | +-0.03 | +-0.8 | +-0.4 | % |
| | | C Version, VSENSE = -5mV to 5mV, TA = -40°C to +125°C | -- | +-0.03 | +-0.8 | +-0.4 | |
| Swing to V+ Power-supply Rail | $V_{OH}$ | RL = 10kΩ to GND, TA = -40°C to +125°C | -- | (V+)-0.05 | (V+)-0.2 | (V+)-0.05 | V |
| Swing to GND | $V_{OL}$ | RL = 10kΩ to GND, TA = -40°C to +125°C | -- | (VGND) +0.005 | (VGND) +0.05 | (VGND)+0.005 | V |
| Operating voltage range | $V_S$ | TA = -40°C to +125°C | 2.7 | -- | 26 | 2.7-26 | V |
| Quiescent Current | $I_Q$ | VSENSE = 0mV | -- | 65 | 100 | 65 | uA |

# Analysis Parameter

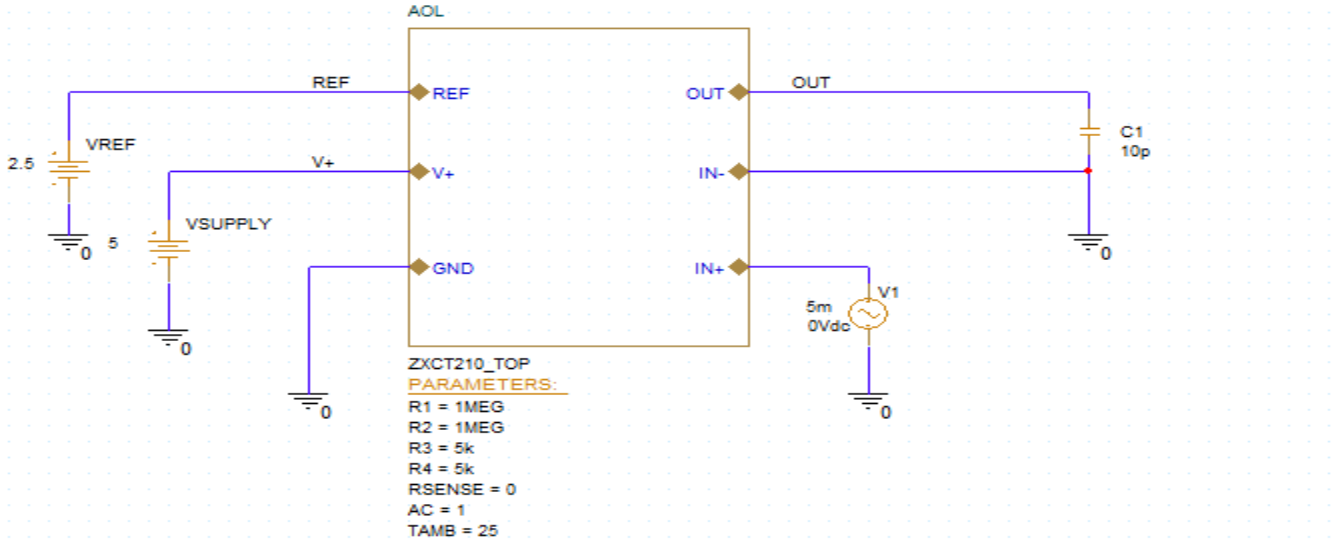
| Parameter | Value |
|---|---|
| VNTOL | 5u |
| ABSTOL | 1n |
| CHGTOL | 1p |
| ITL4 | 40 |
| TIME STEP | 10n |

Note: Remaining parameters are set to the default values of Allegro Pspice 17.4.

# AC Analysis

# Frequency Response Test Setup and Condition

**Test Condition: VSUPPLY=5V, VREF=2.5V, FREQ=10Hz – 10MHz**

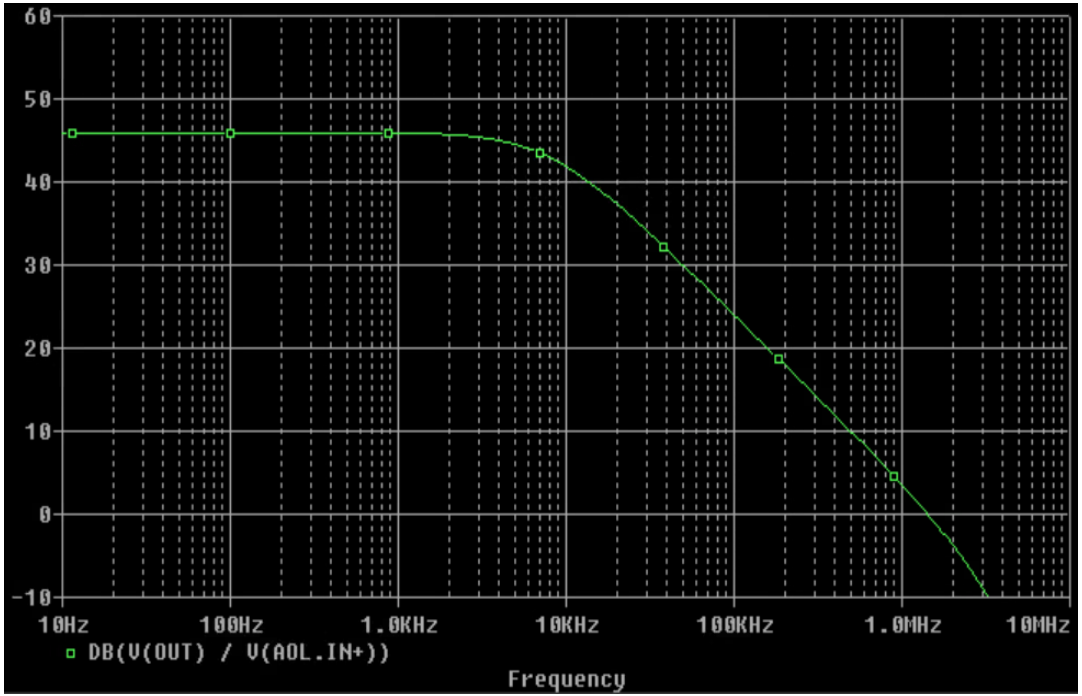



## Testbench Description

- The above testbench has been set-up to observe the frequency response of the device.
- Keep AC=1 : For AC analysis; Keep AC=0 : For transient analysis.
- Time taken for the simulation to complete which runs for the frequency range of 10Hz to 10MHz = Few seconds.

# PSpice Simulation Result / Datasheet

P-Spice Result




Datasheet

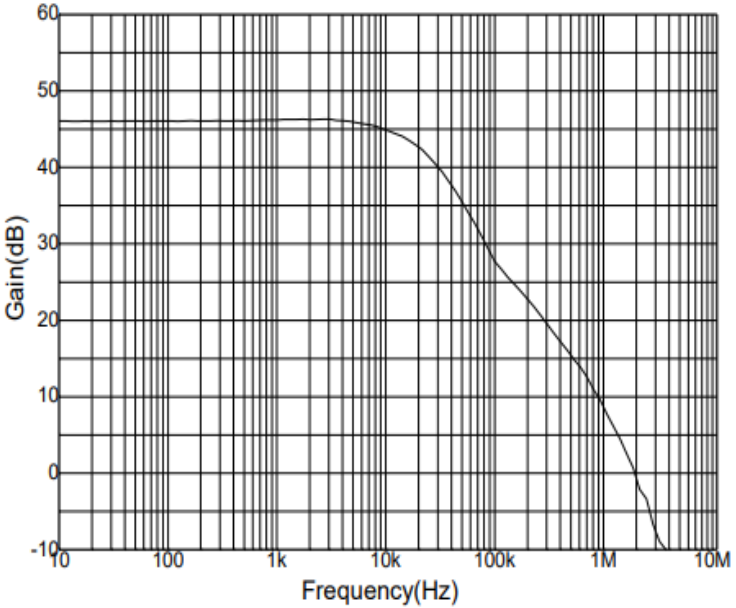
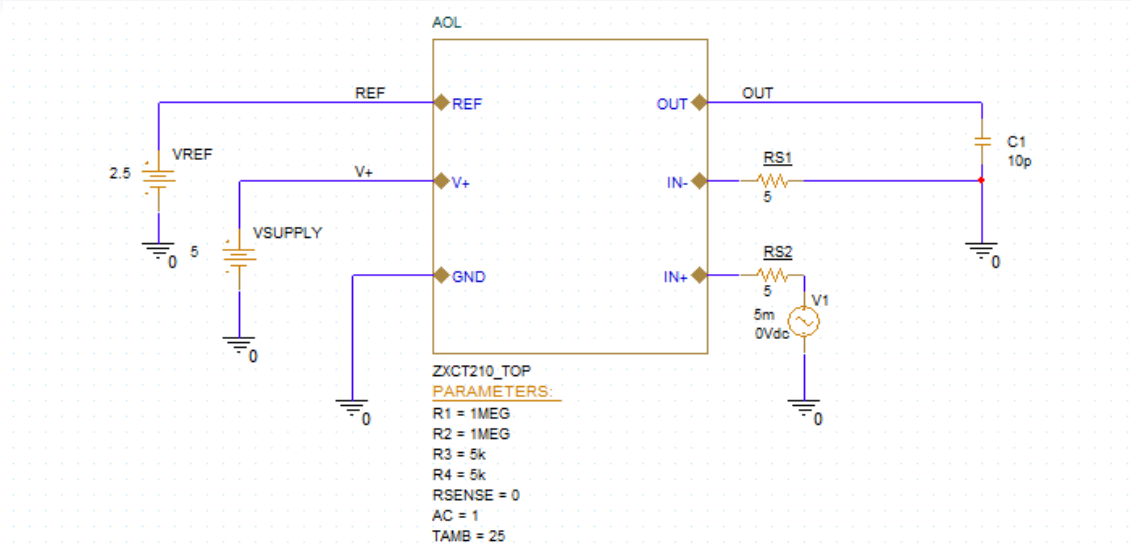



Figure 3. Gain vs. Frequency

# Gain Error Test Setup and Condition

**Test Condition: VSUPPLY=5V, VREF=2.5V, FREQ=10Hz – 10MHz**



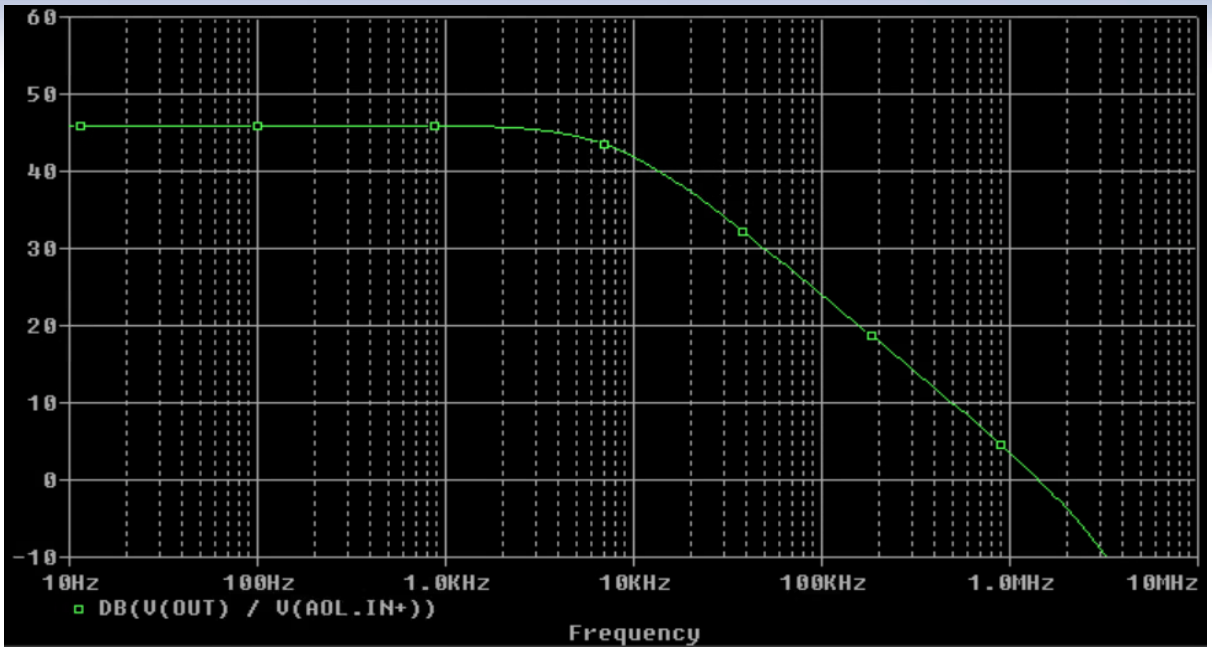

## Testbench Description

•The above testbench has been set-up to observe the frequency response of the device. The Error is inducted in the device by changing the values of the source resistors, RS1 & RS2

•Keep AC=1 : For AC analysis; Keep AC=0 : For transient analysis.

•Time taken for the simulation to complete which runs for the frequency range of 10Hz to 10MHz = Few seconds.

# PSpice Simulation Result




When Rs(=5Ω) is connected,
Gain = 45.977 dB = 198.60 V/V

When Rs (=5Ω) is not connected,
Gain = 46.003 dB = 199.52 V/V

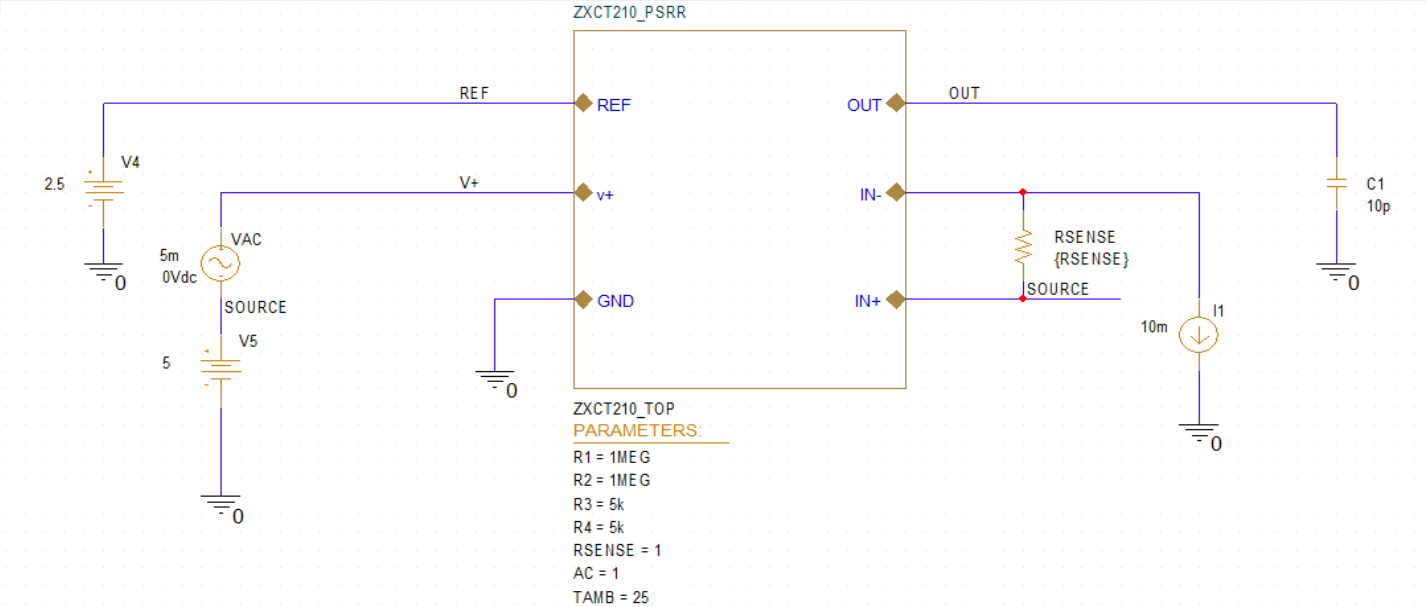
Therefore, the Gain Error =

{(199.52-198.60)/199.52}*100 = 0.4611%

| Part Number | Gain | $R_{INT}$ R3 and R4 | Gain Error Factor Equations | Gain Error % * |
|---|---|---|---|---|
| | | | | $R_S$ = 5Ω |
| ZXCT210 | 200 | 5kΩ | $\frac{1000}{R_S + 1000}$ | 0.4975% |

# PSRR Test Setup and Condition

**Test Condition: VSUPPLY=5V, VREF=2.5V, FREQ=10Hz – 100kHz**

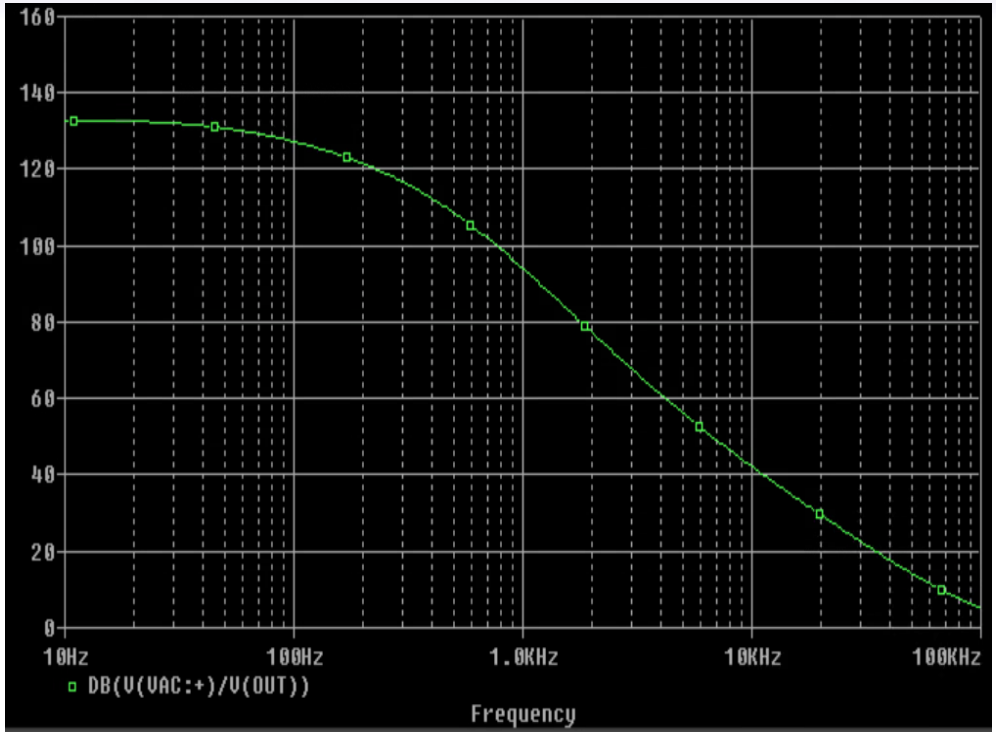



## Testbench Description

- The above testbench has been set-up to observe the PSRR characteristics of the device.
- Keep AC=1 : For AC analysis; Keep AC=0 : For transient analysis.
- Time taken for the simulation to complete which runs for the frequency range of 10Hz to 100KHz = Few seconds.

# PSpice Simulation Result / Datasheet

P-Spice Result




Datasheet

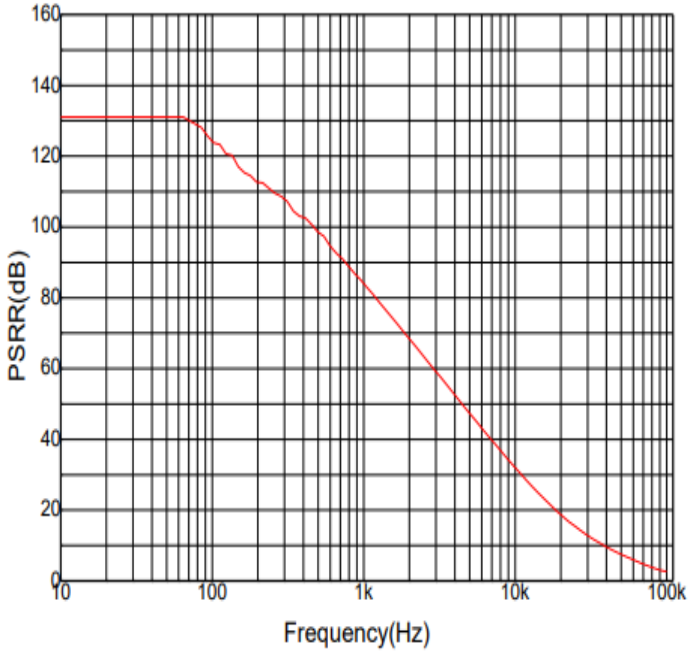
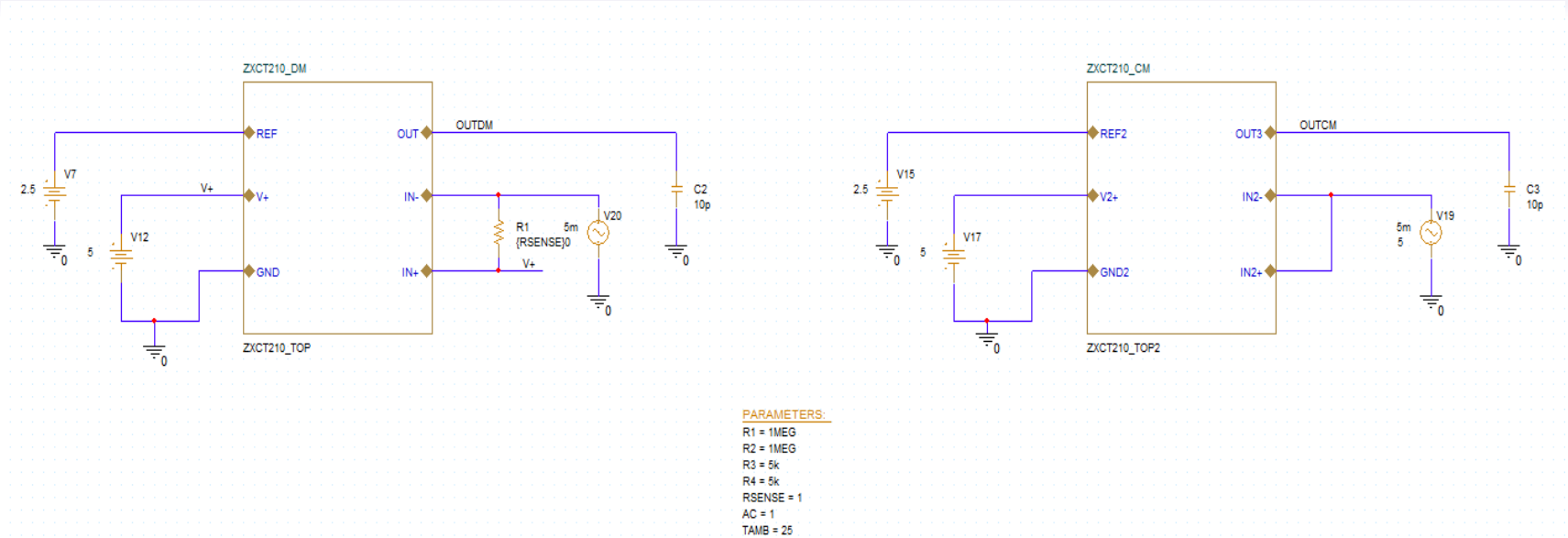



Figure 4. Power-Supply Rejection Ratio vs. Frequency

# CMRR Test Setup and Condition

**Test Condition: VSUPPLY=5V, VREF=2.5V, FREQ=10Hz – 1MHz**

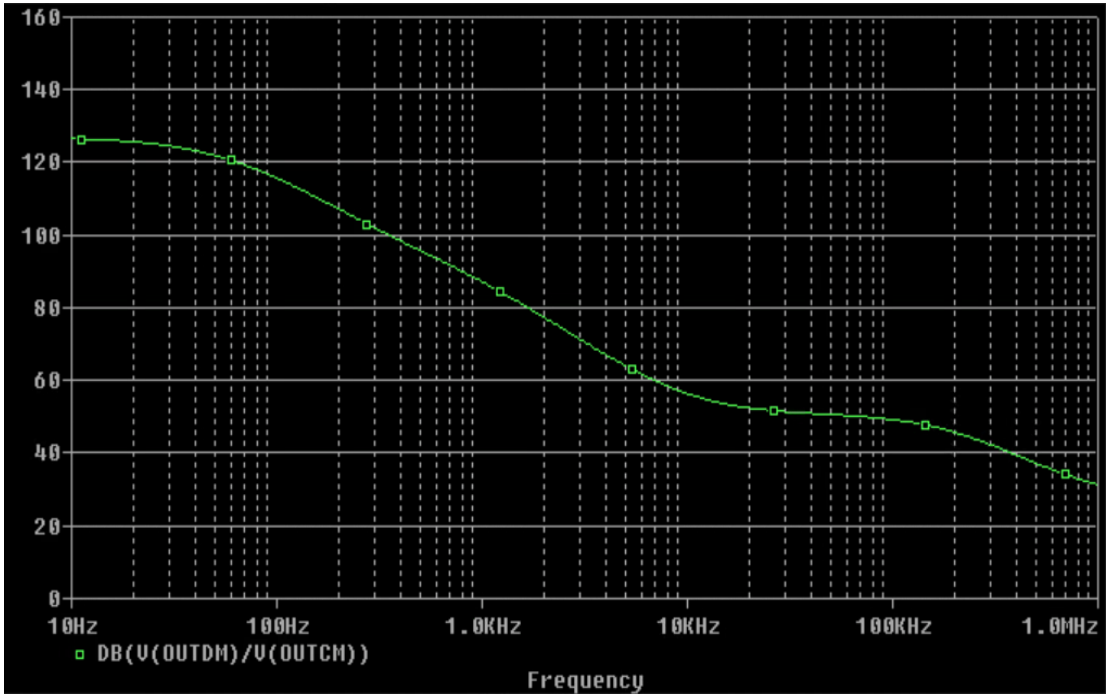



## Testbench Description

- The above testbench has been set-up to observe the CMRR vs frequency response of the device.
- Keep AC=1 : For AC analysis; Keep AC=0 : For transient analysis.
- Time taken for the simulation to complete which runs for the frequency range of 10Hz to 1MHz = Few seconds.

# PSpice Simulation Result / Datasheet

P-Spice Result




Datasheet

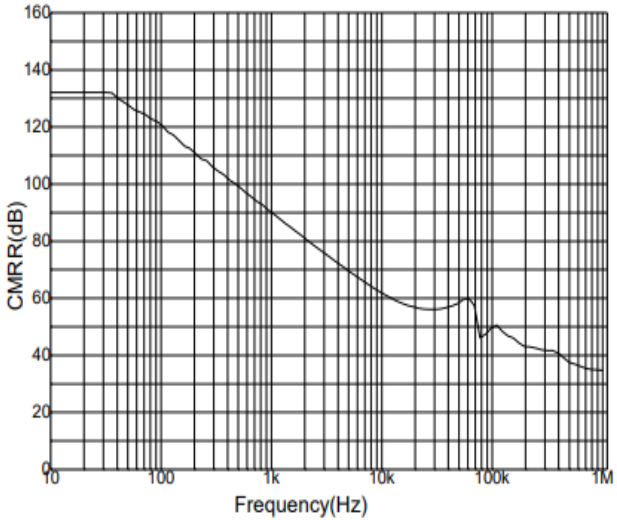
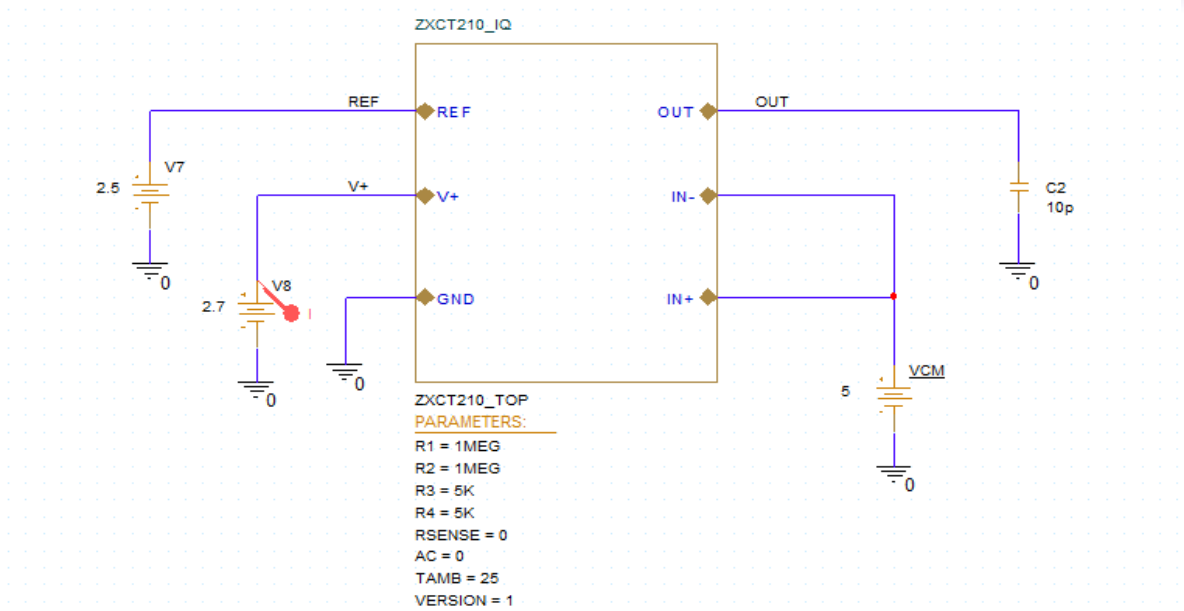



Figure 5. Common-Mode Rejection Ratio vs. Frequency

# Temperature variation

# Quiescent current vs Temperature

**Test Condition: VSUPPLY=2.7V, VREF=2.5V, COMMON MODE VOLTAGE (V_CM)=5V**



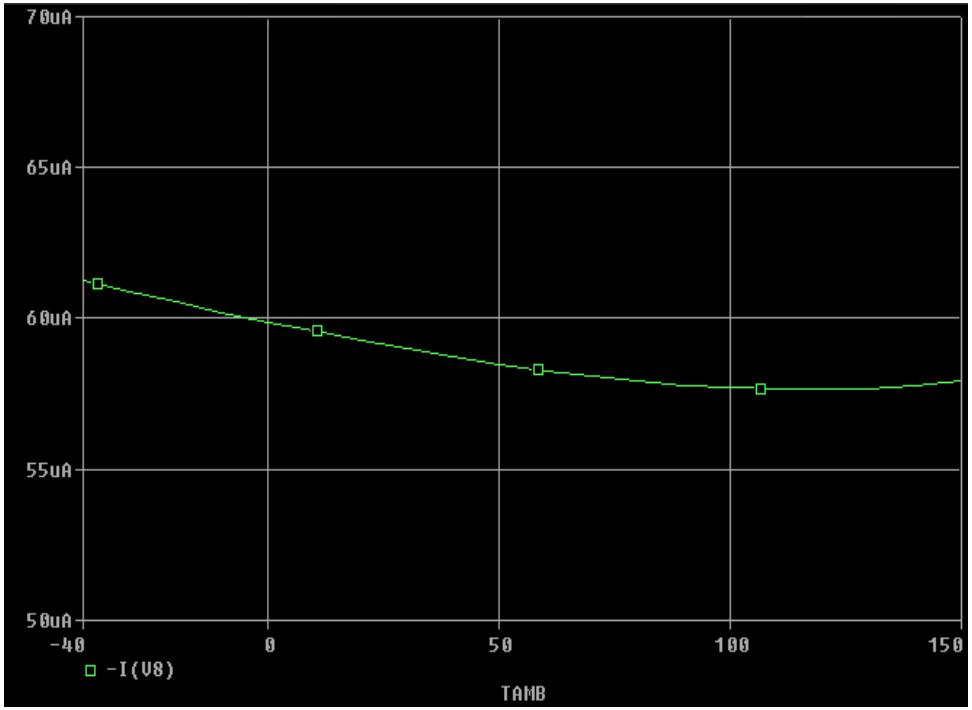

## Testbench Description

•The above testbench has been set-up to observe the variation of the Quiescent current with respect to temperature variation.

•Time taken for the simulation to complete = Few seconds.

# PSpice Simulation Result / Datasheet

P-Spice Result




Datasheet

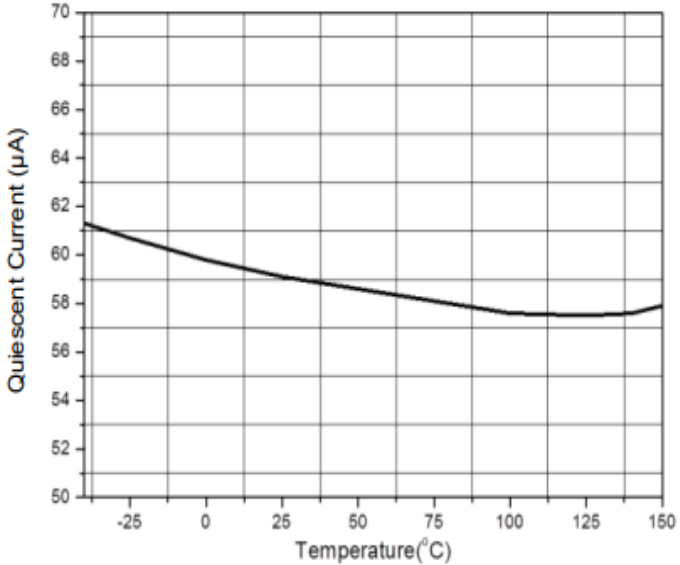
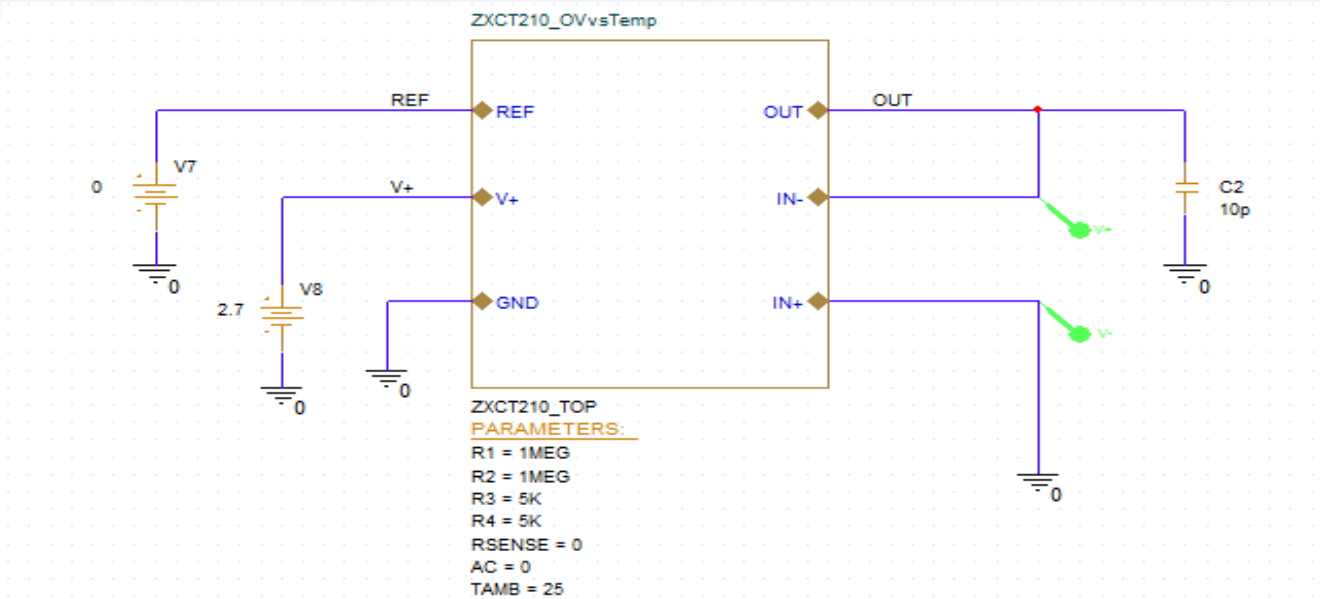



Figure 11. Quiescent Current vs. Temperature

# Offset voltage vs Temperature

**Test Condition: VSUPPLY=2.7V, VREF=0, V(IN+)=0**

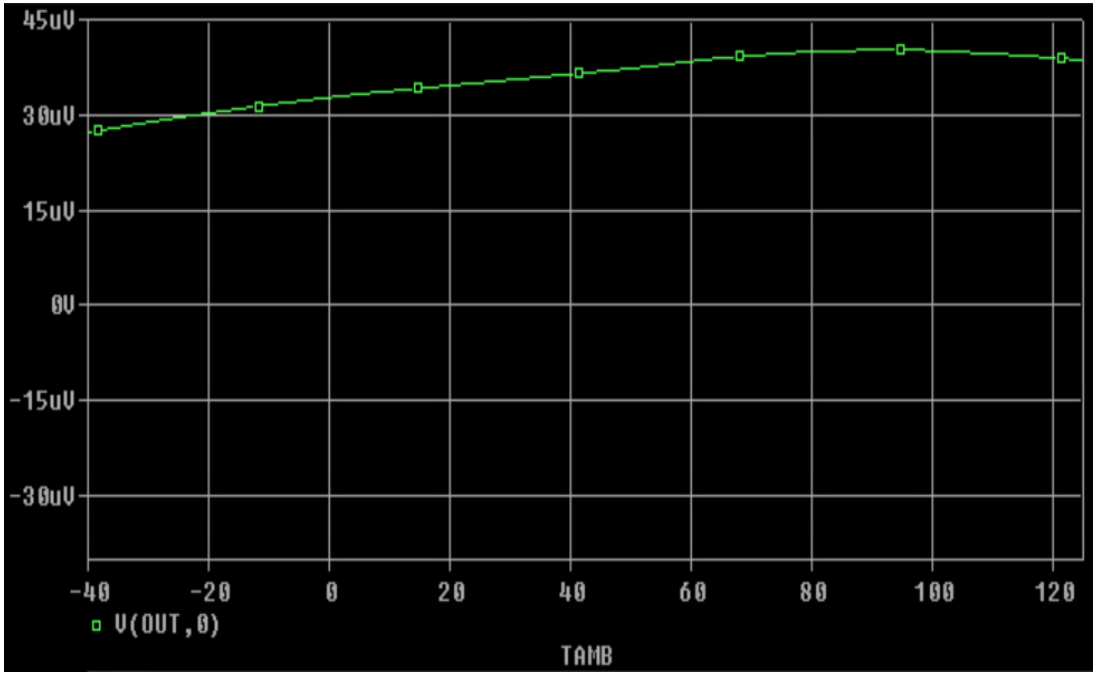



## Testbench Description

- The above testbench has been set-up to observe the variation of the Offset voltage with respect to temperature.
- Time taken for the simulation to complete = Few seconds.

# PSpice Simulation Result / Datasheet

P-Spice Result




Datasheet

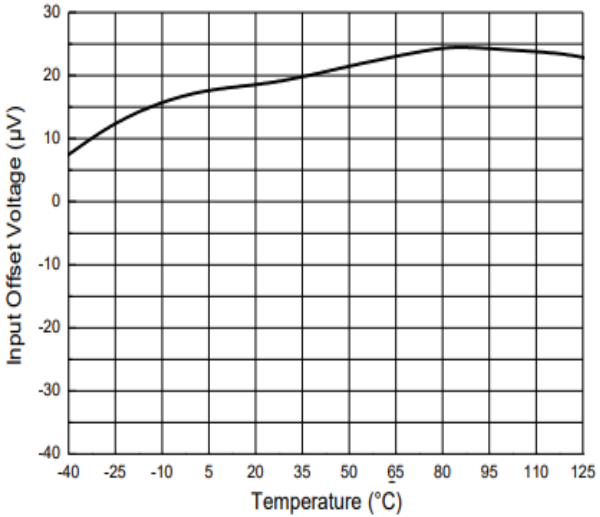
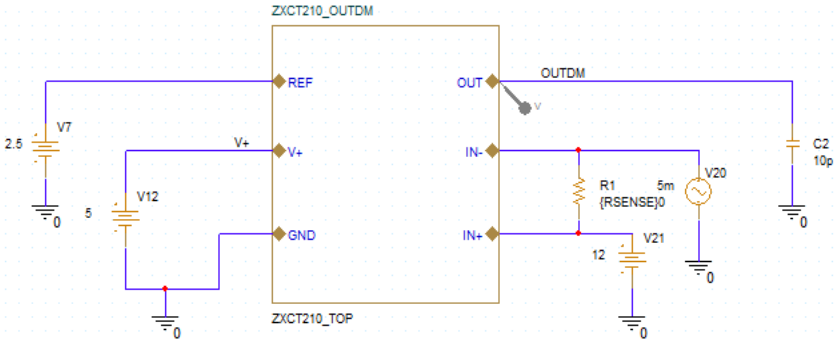
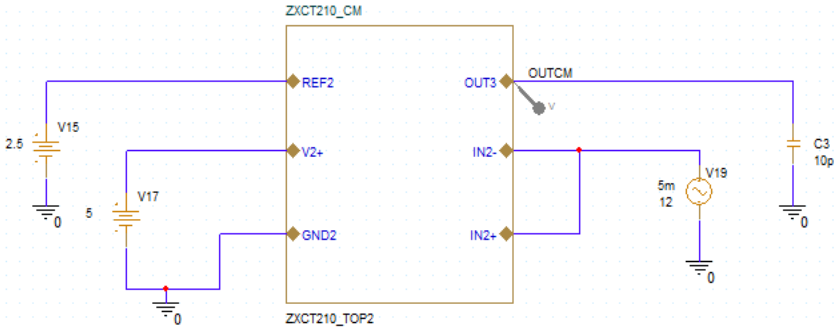



Figure 1. Offset Voltage vs. Temperature

# CMRR vs Temperature

**Test Condition: VSUPPLY=5V, VREF=2.5, V(IN+)=12V**



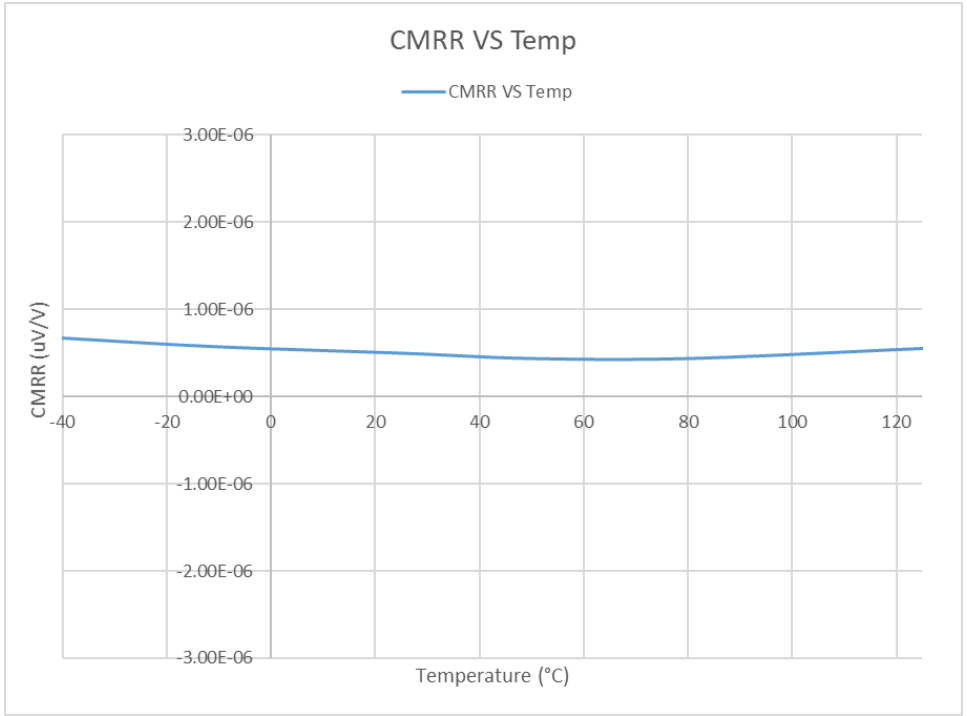




PARAMETERS:
R1 = 1MEG
R2 = 1MEG
R3 = 5k
R4 = 5k
RSENSE = 1
AC = 1
TAMB = 25
VERSION = 1

## Testbench Description

- The above testbench has been set-up to observe the variation of CMRR with respect to temperature.
- Keep AC=1 : For AC analysis; Keep AC=0 : For transient analysis.
- Time taken for the simulation to complete = Few seconds.

# PSpice Simulation Result / Datasheet




Datasheet

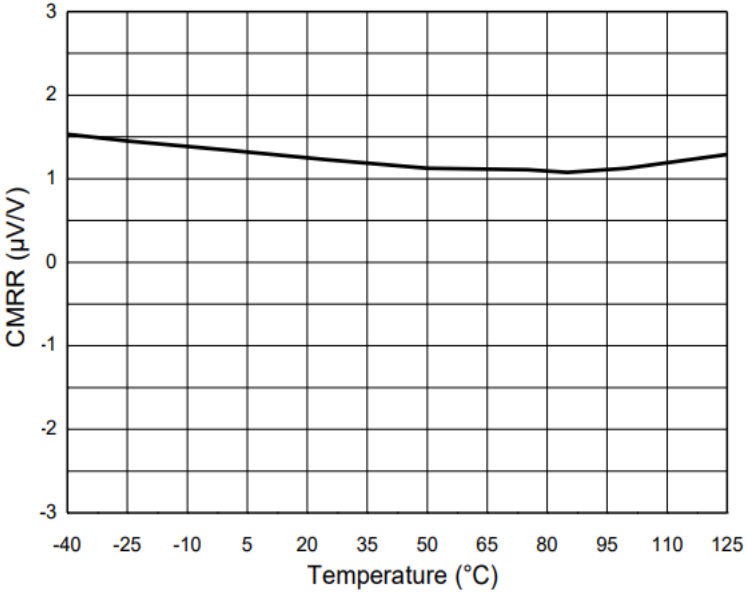
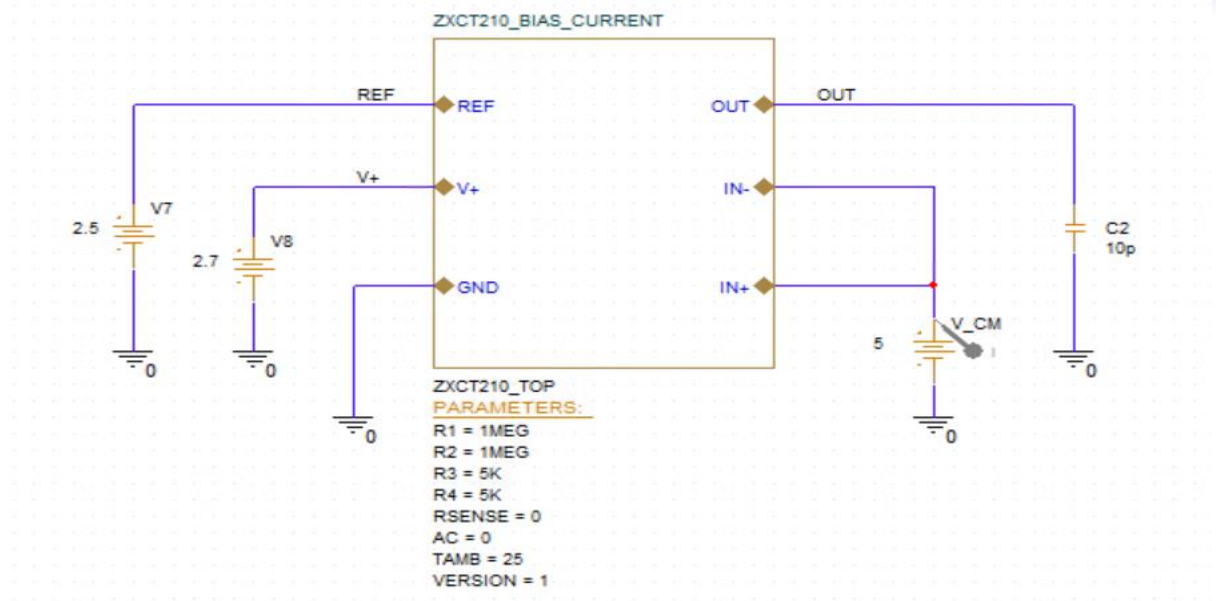



Figure 2. Common-Mode Rejection Ratio vs. Temperature

# DC Analysis

# Bias Current Test Setup 1 and Condition

**Test Condition: VSUPPLY=2.7V, VREF=2.5V, COMMON MODE VOLTAGE (V_CM)=5V**



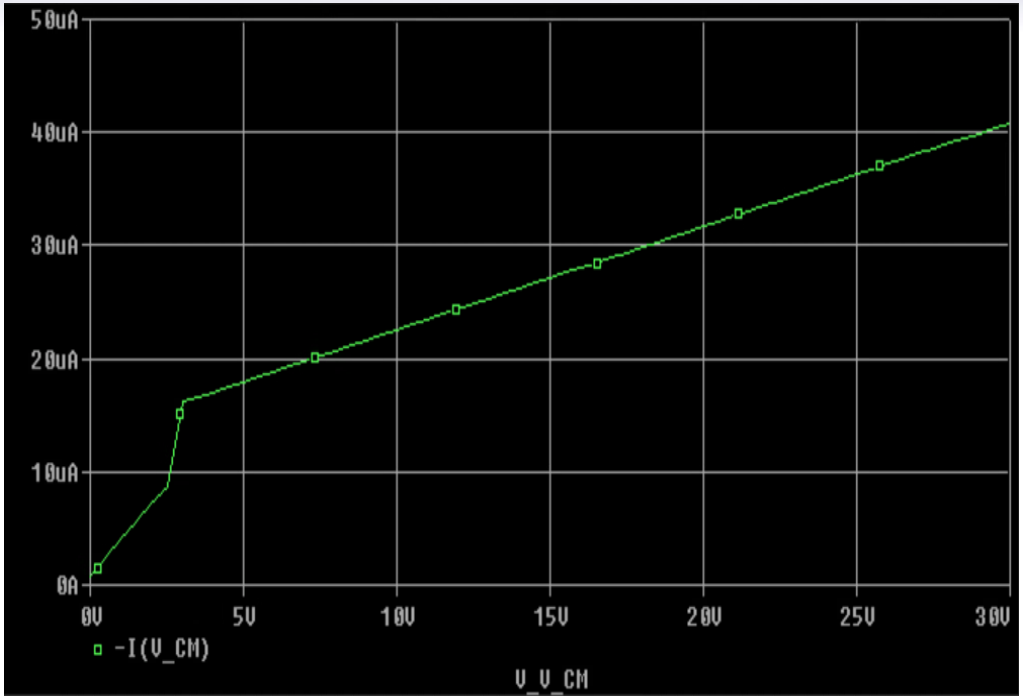

## Testbench Description

•The above testbench has been set-up to observe the variation of the input bias current with respect to the common mode voltage variation.

•Time taken for the simulation to complete = Few seconds.

# PSpice Simulation Result / Datasheet

P-Spice Result




Datasheet

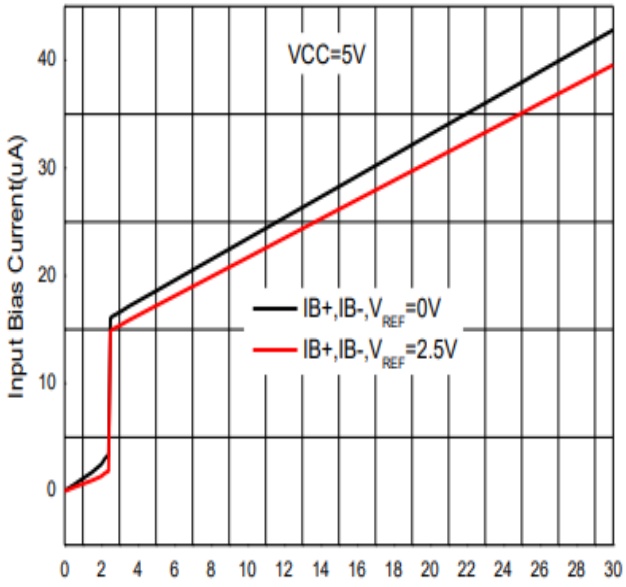
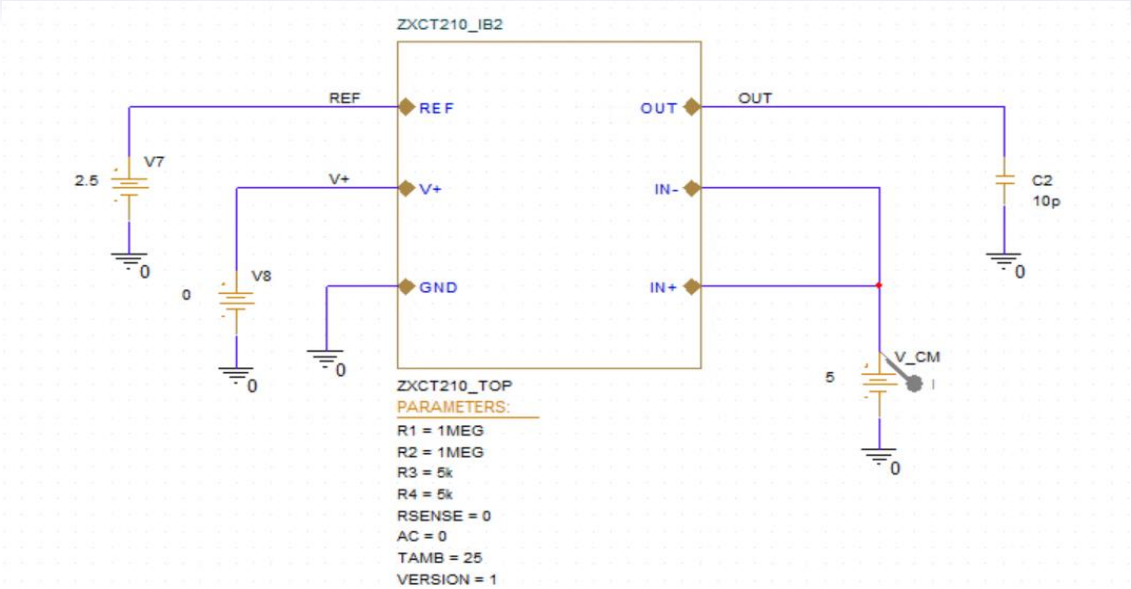



Figure 8. Input Bias Current vs. Common-Mode Voltage

# Bias Current Test Setup 2 and Condition

**Test Condition: VSUPPLY=0V, VREF=2.5V, COMMON MODE VOLTAGE (V_CM)=5**

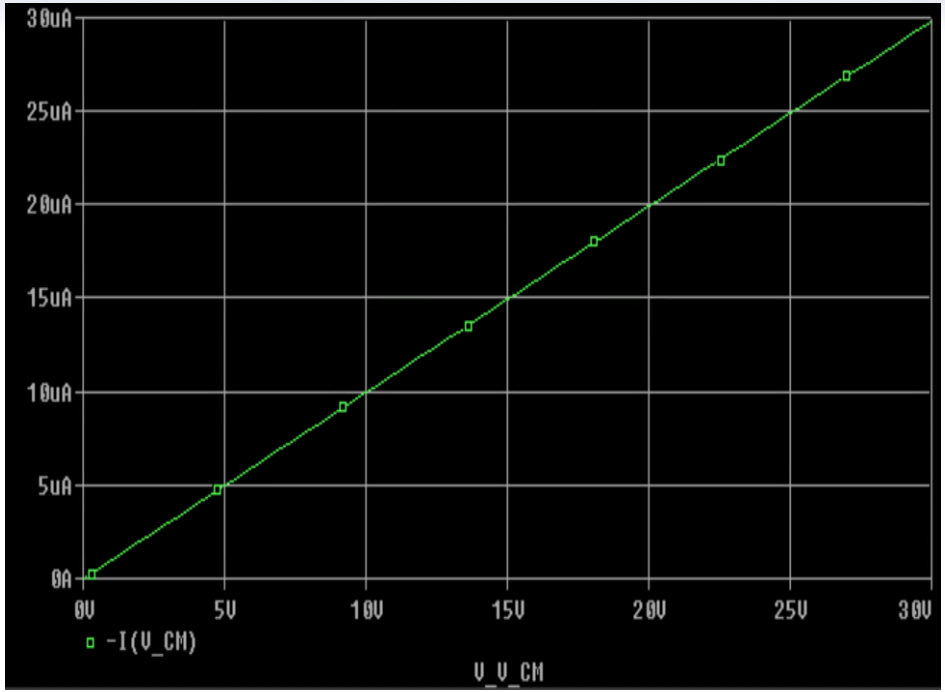



## Testbench Description

- The above testbench has been set-up to observe the variation of the input bias current with respect to the common mode voltage variation.
- Time taken for the simulation to complete = Few seconds.

# PSpice Simulation Result / Datasheet

P-Spice Result




Datasheet

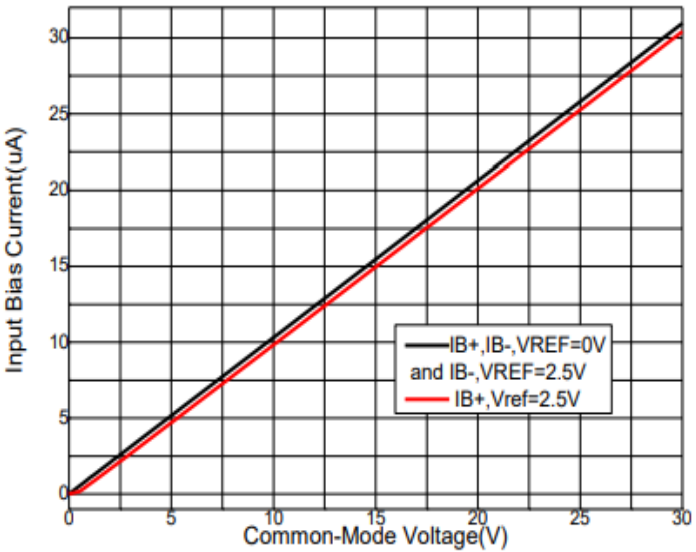
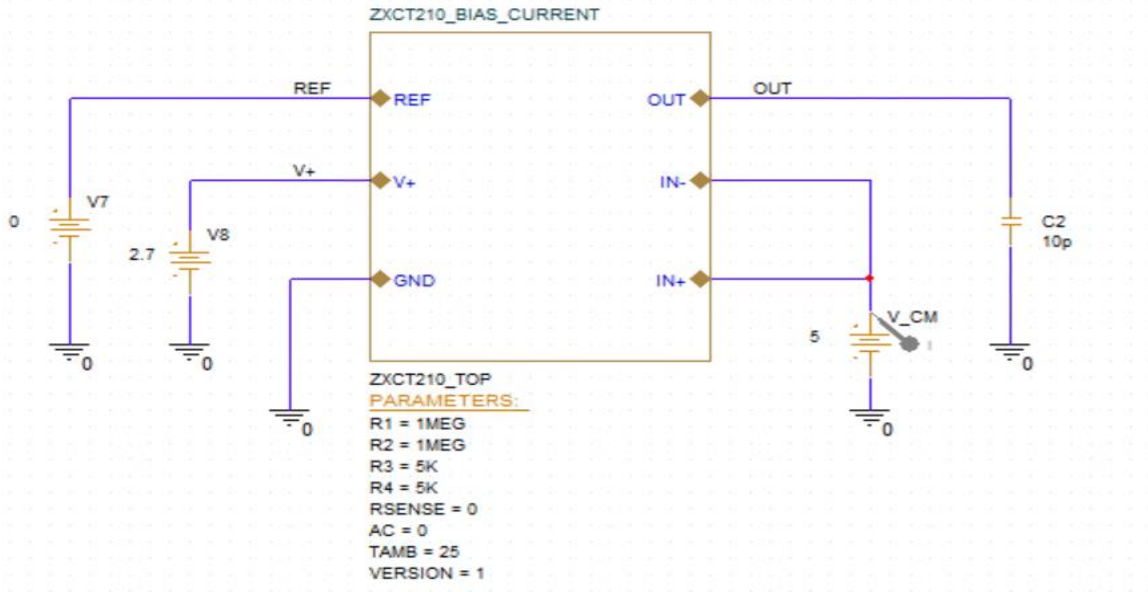



Figure 9. Input Bias Current vs. Common-Mode Voltage
With Supply Voltage=0V(Shutdown)

# Bias Current Test Setup 3 and Condition

**Test Condition: VSUPPLY=2.7V, VREF=0V, COMMON MODE VOLTAGE (V_CM)=5V**



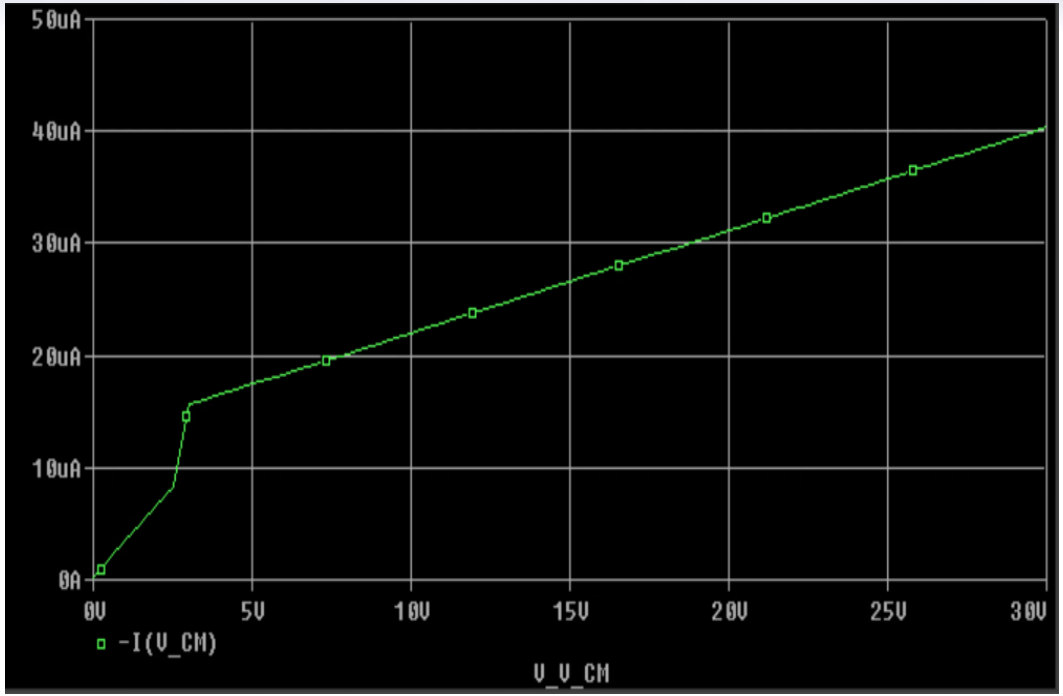

## Testbench Description

•The above testbench has been set-up to observe the variation of the input bias current with respect to the common mode voltage variation.

•Time taken for the simulation to complete = Few seconds.

# PSpice Simulation Result / Datasheet

P-Spice Result




Datasheet

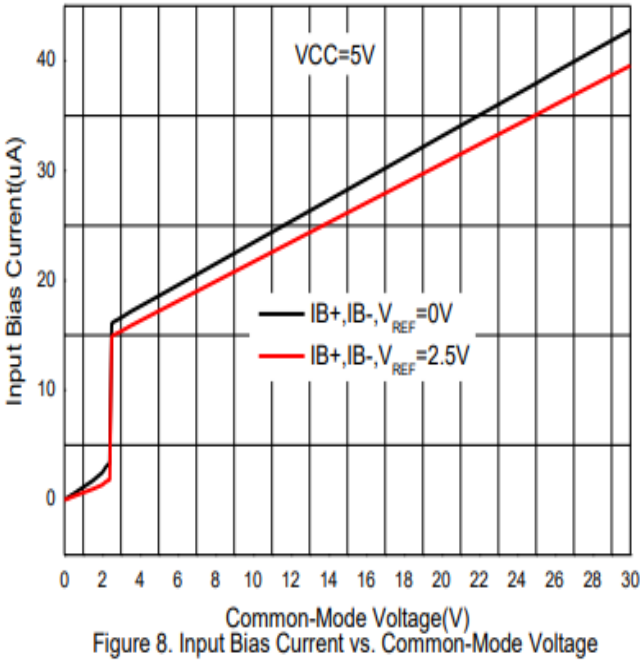
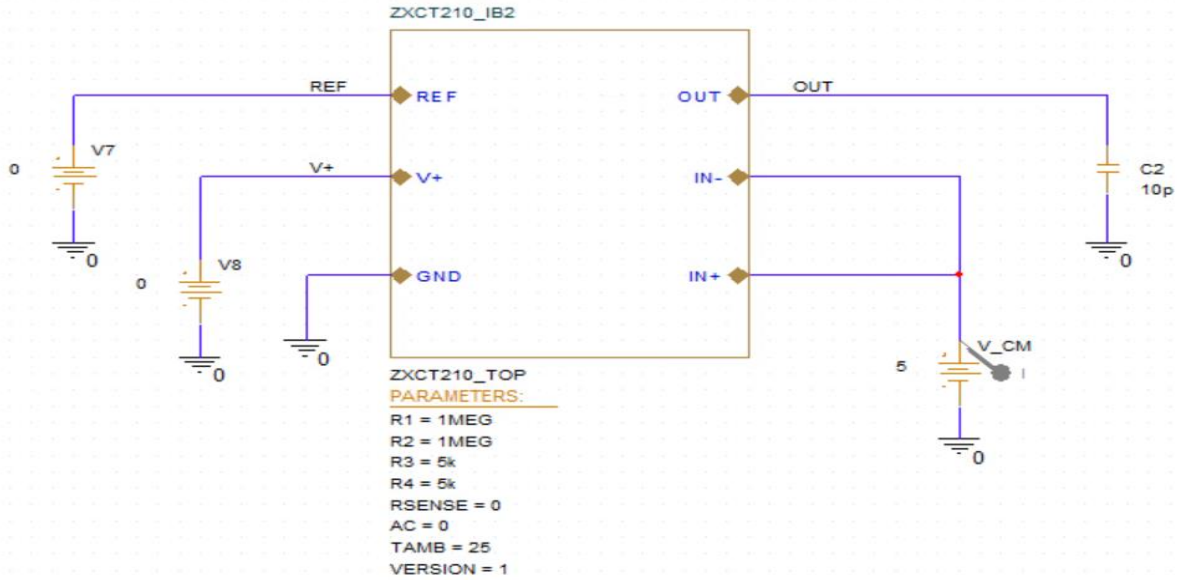



Figure 8. Input Bias Current vs. Common-Mode Voltage

# Bias Current Test Setup 4 and Condition

**Test Condition: VSUPPLY=0V, VREF=0V, COMMON MODE VOLTAGE (V_CM)=5V**



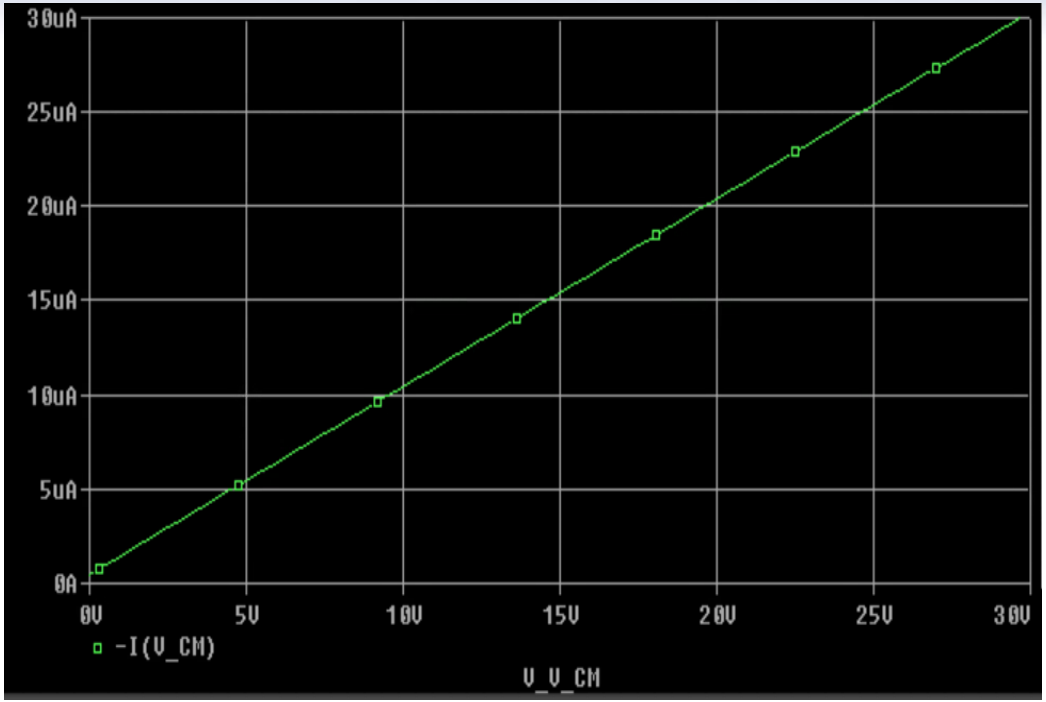

## Testbench Description

•The above testbench has been set-up to observe the variation of the input bias current with respect to the common mode voltage variation.

•Time taken for the simulation to complete = Few seconds.

# PSpice Simulation Result / Datasheet

P-Spice Result




Datasheet

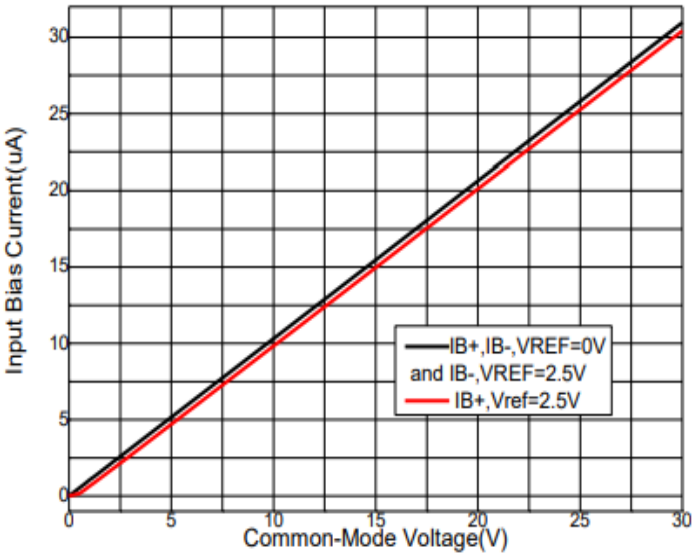
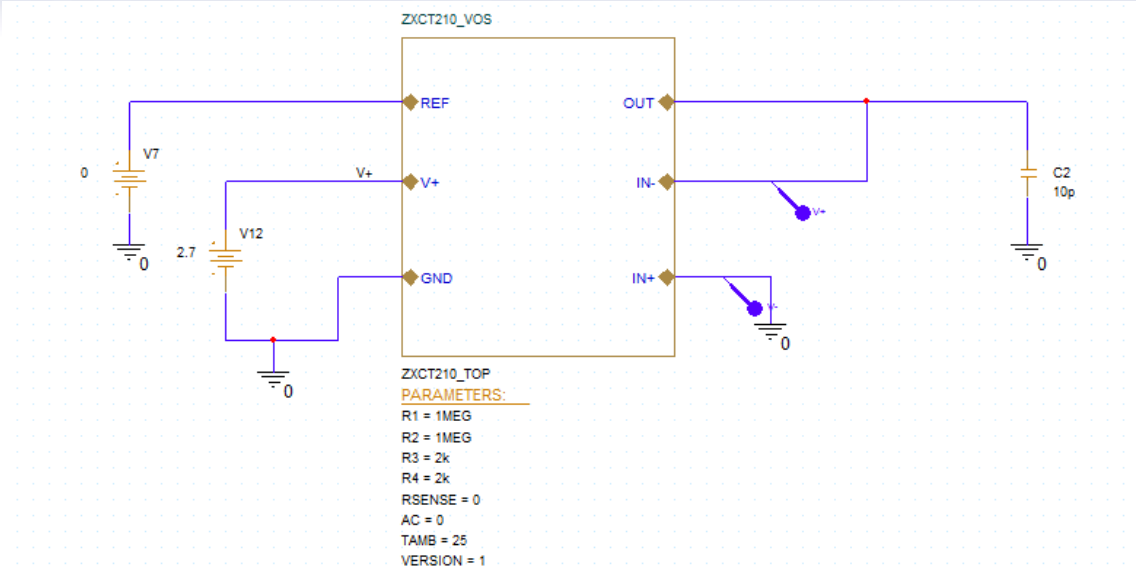



Figure 9. Input Bias Current vs. Common-Mode Voltage
With Supply Voltage=0V(Shutdown)

# Transient Analysis

# Offset voltage test setup

**Test Condition: VSUPPLY=2.7V, VREF=0V**

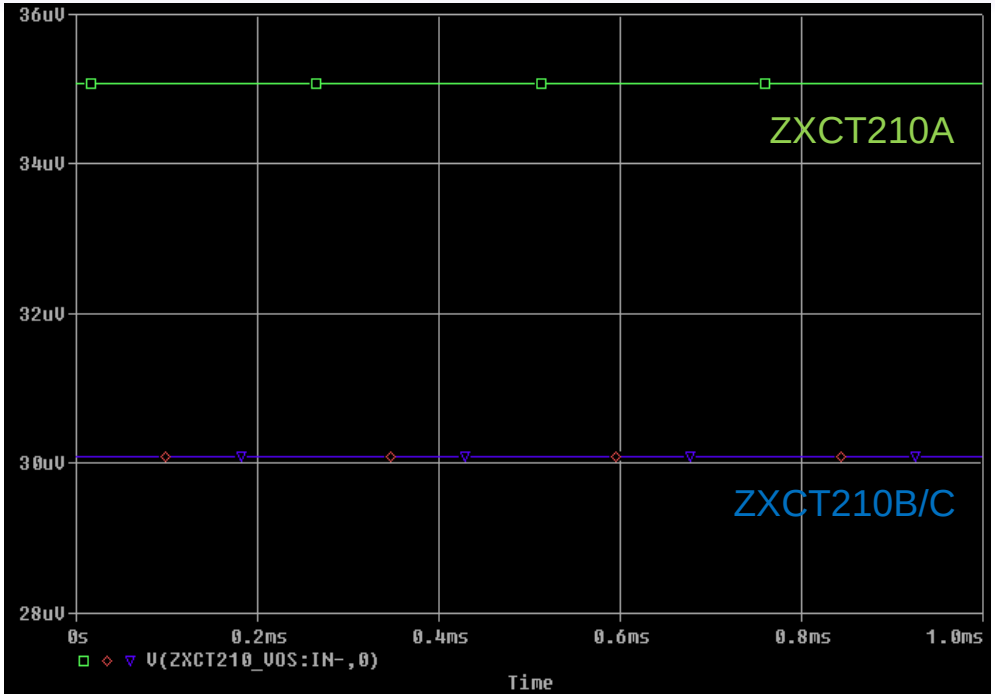



## Testbench Description

- The above testbench has been set-up to observe the offset voltage of ZXCT210 A, B & C version. Parameter "VERSION" is used to control the A(VERSION=1), B(VERSION=2), C(VERSION=3) versions.
- Keep AC=1 : For AC analysis; Keep AC=0 : For transient analysis.
- Time taken for the simulation to complete = Few seconds.

# PSpice Simulation Result / Datasheet

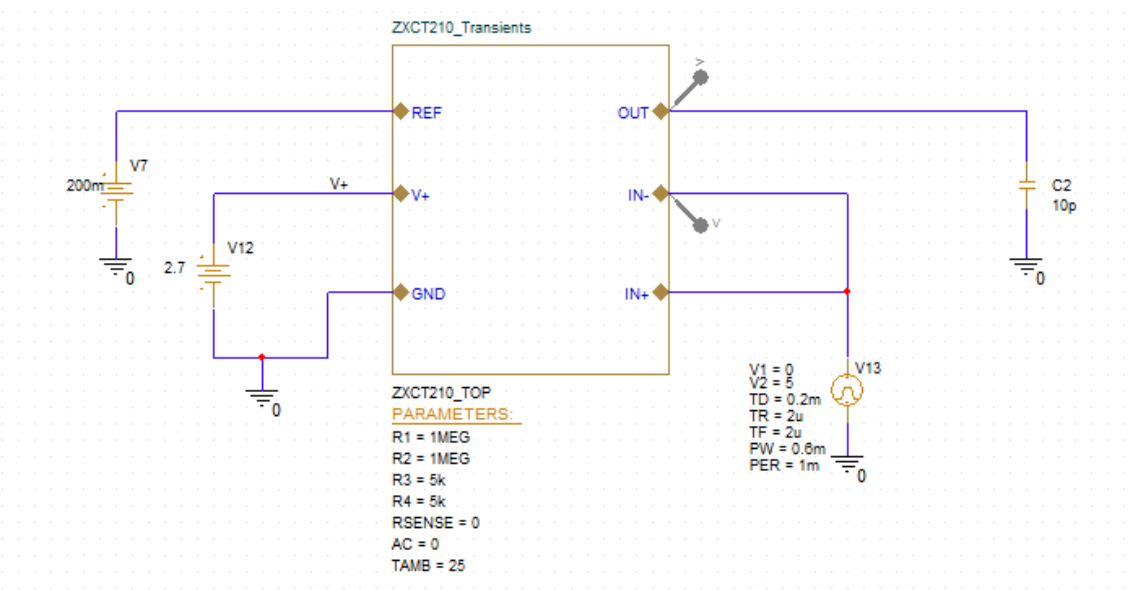
P-Spice Result




| Version | Datasheet Value | PSPICE Value |
|---|---|---|
| ZXCT210A | 35uV | 35uV |
| ZXCT210B | 30uV | 30.1uV |
| ZXCT210C | 30uV | 30.1uV |

# Common Mode Voltage Vs Transient Response Test Setup and Condition

**Test Condition: VSUPPLY=2.7V, VREF=200mV, COMMON MODE VOLTAGE (CM)=0V-5V-0V**

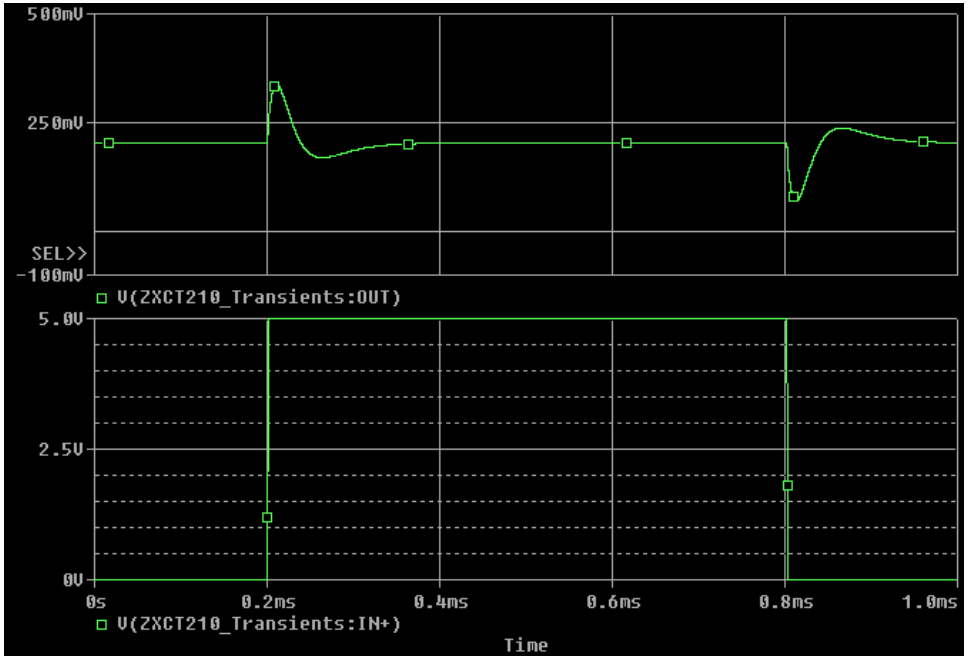



## Testbench Description

- The above testbench has been set-up to observe the transient response in case of common mode voltage.
- Keep AC=1 : For AC analysis; Keep AC=0 : For transient analysis.
- Time taken for the simulation to complete = Few seconds.

# PSpice Simulation Result / Datasheet

P-Spice Result




Datasheet

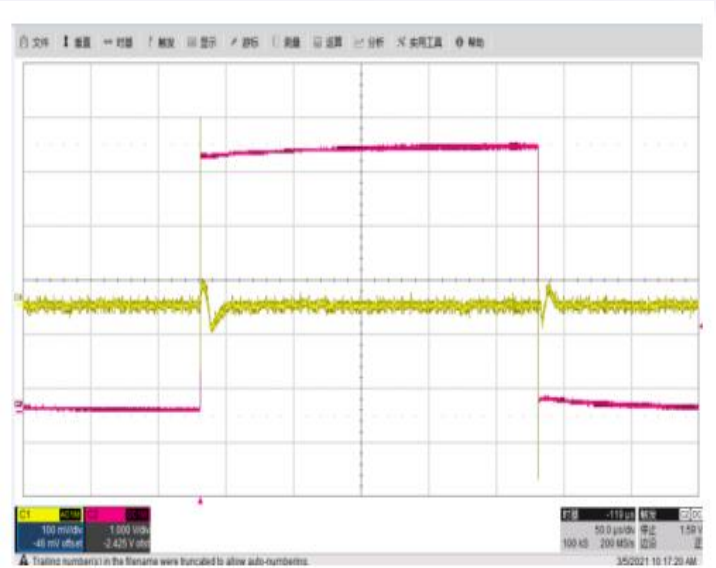
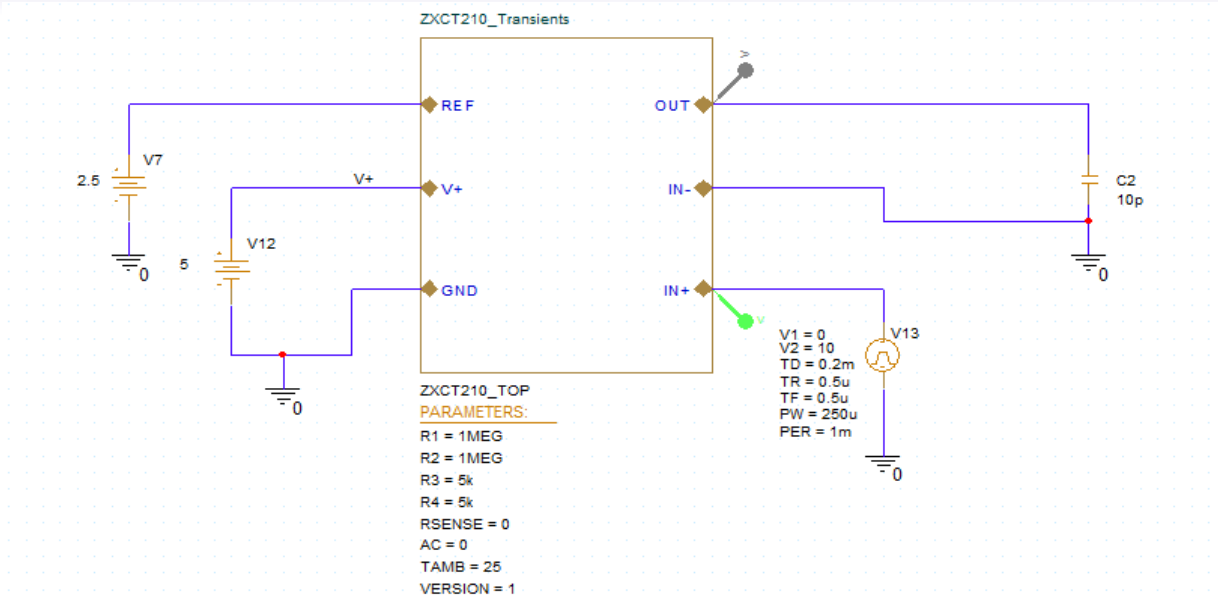


Figure 13 Common-Mode Voltage vs Transient Response

# Non Inverting Differential Input Overload Test Setup and Condition

**Test Condition: VSUPPLY=5V, VREF=2.5V, Input Voltage=0V-10V-0V**

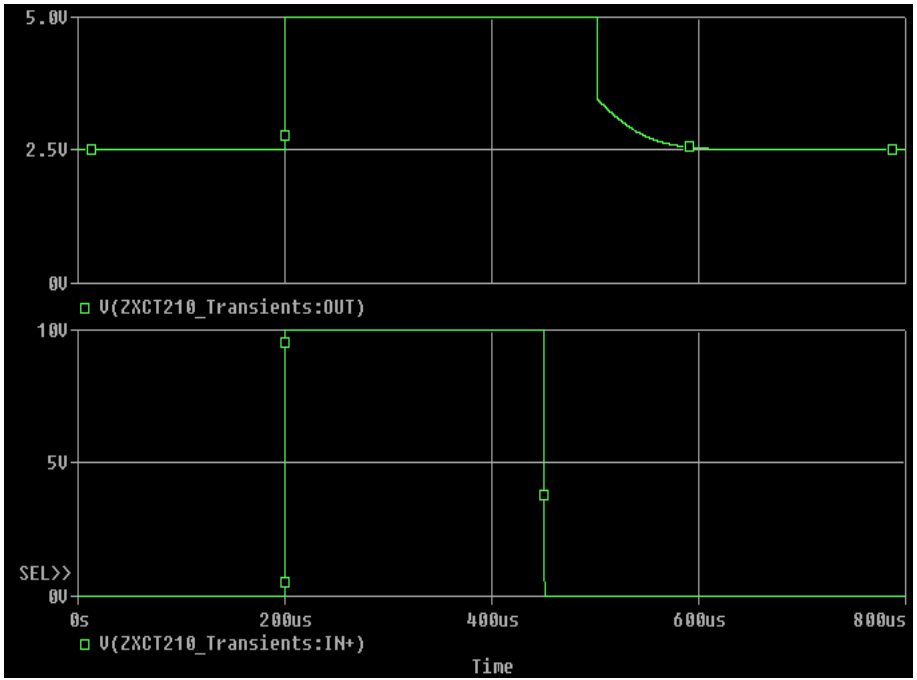



## Testbench Description

- The above testbench has been set-up to observe the response in non inverting input overload.
- Keep AC=1 : For AC analysis; Keep AC=0 : For transient analysis.
- Time taken for the simulation to complete = Few seconds.

# PSpice Simulation Result / Datasheet

P-Spice Result




Datasheet

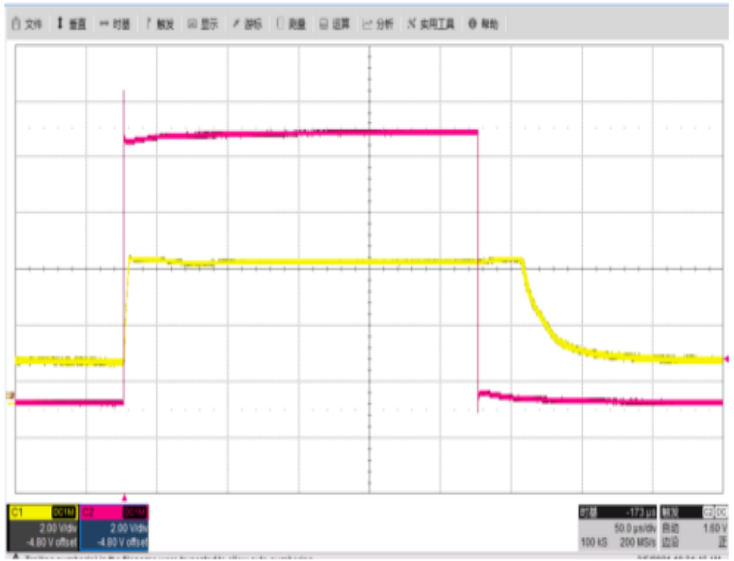
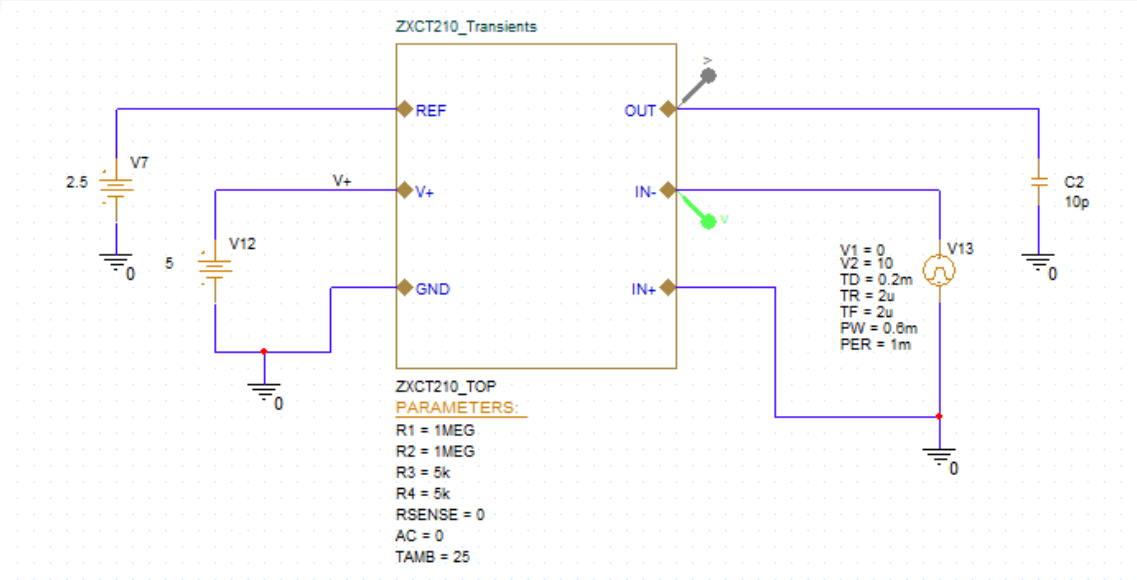


Figure14 Noninverting Differential Input Overload

# Inverting Differential Input Overload Test Setup and Condition

**Test Condition: VSUPPLY = 5V, VREF = 2.5V, Input Voltage = 0V-10V-0V**

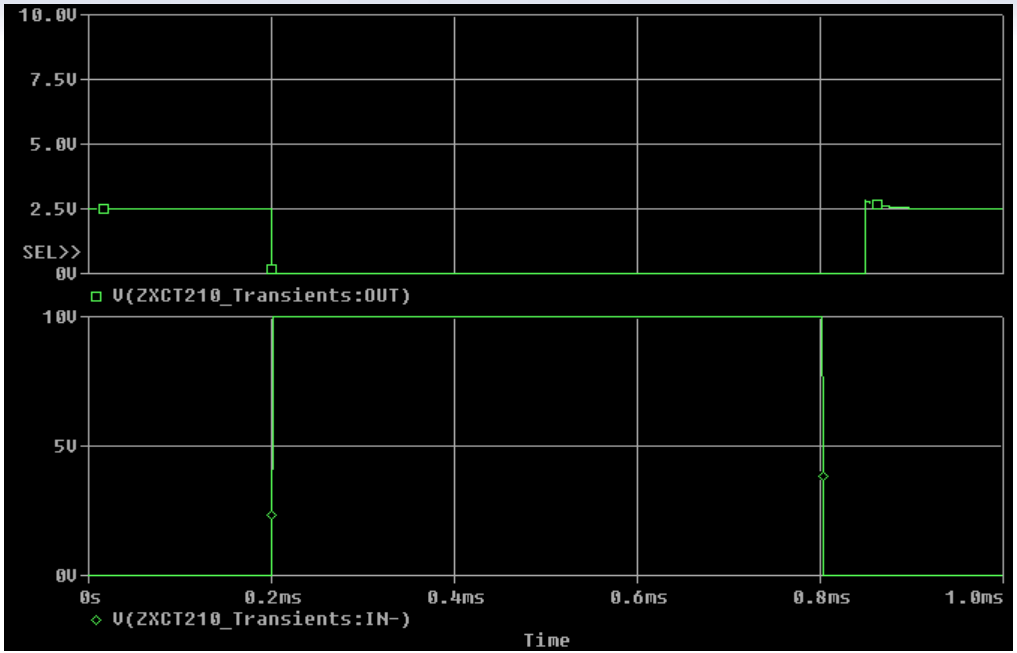



## Testbench Description

- The above testbench has been set-up to observe the response in inverting input overload.
- Keep AC=1 : For AC analysis; Keep AC=0 : For transient analysis.
- Time taken for the simulation to complete = Few seconds.

# PSpice Simulation Result / Datasheet

P-Spice Result




Datasheet

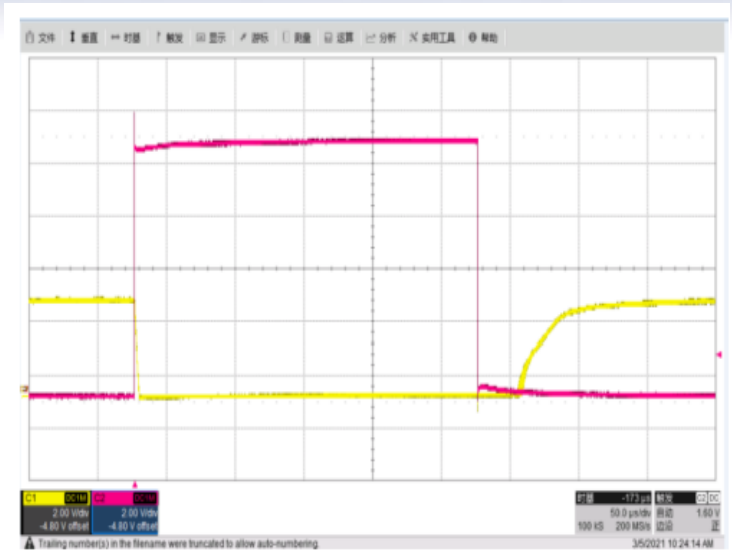


Figure 15 Inverting Differential. Input Overload

# THANK YOU