TRIPLE DC-DC CONVERTERS FOR 500mA AMOLED

Description

The AL3565 is a Power Management Integrated Chip (PMIC) with three programmable DC-DC converters via a simple one wire digital control to power supply bias 500mA AMOLED (Active Matrix Organic Light Emitting Diode) panel requiring three supply rails, V_{POS}, V_{NEG} and AV_{DD}.

The device integrates a buck-boost converter for V_{POS}, an inverting buck-boost converter for V_{NEG}, and a boost converter for AV_{DD}, which are suitable for power management of portable products operated under lithium-ion battery power.

The PRG (Programming Digital Control) pin allows programming the V_{POS} and V_{NEG} output voltage in steps of 100mV, and AV_{DD} in steps of 300mV. The AL3565 offers an excellent line and load regulation.

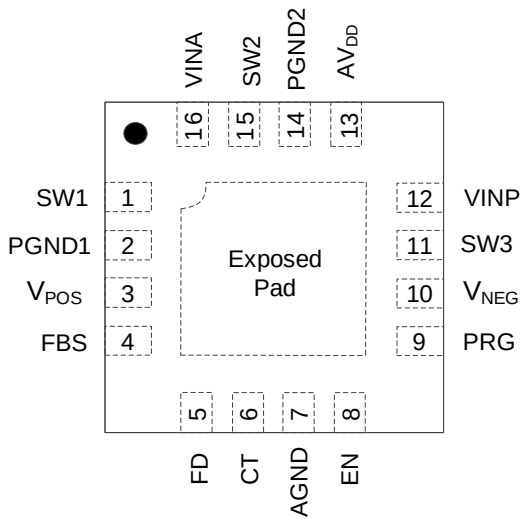
The AL3565 is available in U-QFN3030-16 (Type B) (3.0mm x 3.0mm) 16-pin package with exposed pad. Please contact us for WL-CSP and other package options.

Features

- Wide Input Voltage Range: 2.9V to 4.8V
- -40°C to + 85°C Operating Ambient Temperature
- V_{POS} – Buck-Boost Converter (Default 4.6V)
  - 4.6V to 5.4V, Programmable Output Voltage
  - 100mV Step Size
  - Up to 500mA Output Current
  - 0.5% Accuracy
- AV_{DD} – Boost Converter (Default 6.1V)
  - 5.8V to 7.9V, Programmable Output Voltage
  - 300mV Step Size
  - 100mA Output Current
  - 0.5% Accuracy
- V_{NEG} – Inverting Buck-Boost Converter (Default -2.5V)
  - -1.4V to -5.4V, Programmable Negative Voltage
  - 100mV Step Size
  - Up to 500mA Output Current
  - 0.5% Accuracy
- Excellent Line and Transient Regulations
- Short-Circuit Protection (SCP)
- Thermal Shutdown Protection
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**
- **For automotive applications requiring specific change control (i.e. parts qualified to AEC-Q100/101/104/200, PPAP capable, and manufactured in IATF 16949 certified facilities), please contact us or your local Diodes representative. https://www.diodes.com/quality/product-definitions/**

Pin Assignments

Top View



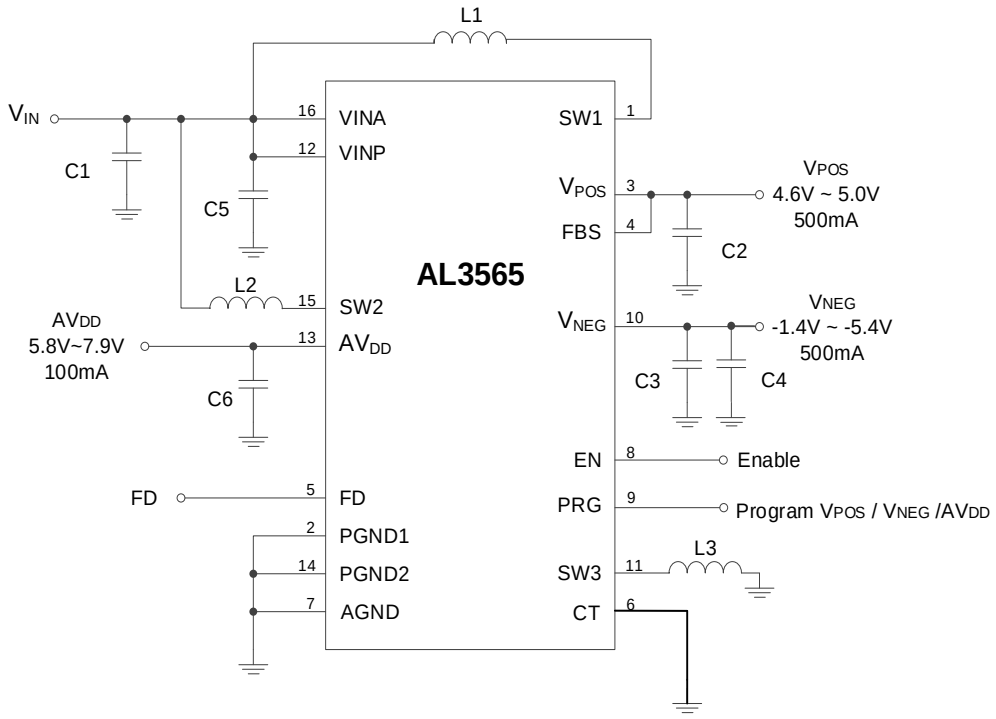
U-QFN3030-16 (Type B)

Applications

- AMOLED display panel power supply bias

Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

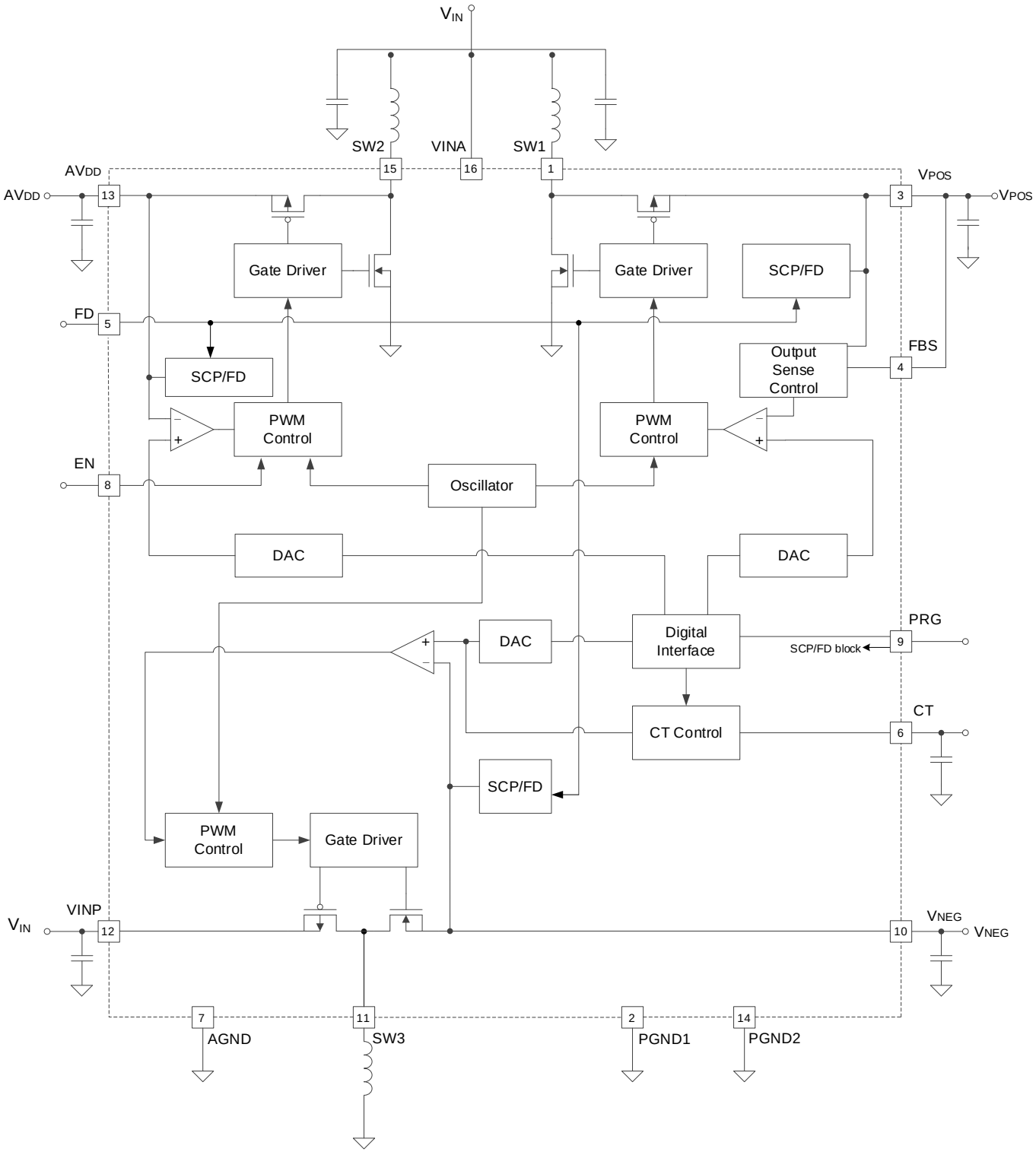
Typical Applications Circuits



Pin Descriptions

Pin Number	Pin Name	Description
1	SW1	Boost converter switch pin
2	PGND1	Boost converter power ground
3	V_{POS}	Boost converter output (V_{POS})
4	FBS	Boost converter sense pin
5	FD	Fast Discharge circuit function selection. High level enables the fast discharge function; low level sets V_{POS}, V_{NEG} and AV_{DD} high impedance without output.
6	CT	Must tie to ground
7	AGND	Analog ground
8	EN	Enable boost converter (AV_{DD})
9	PRG	Programming control pin, digital control V_{POS}, V_{NEG} and AV_{DD} output voltage
10	V_{NEG}	Inverting buck-boost output (V_{NEG})
11	SW3	Inverting buck-boost switching pin
12	VINP	Inverting buck-boost converter power stage supply voltage
13	AV_{DD}	Boost converter output voltage pin (AV_{DD})
14	PGND2	Boost converter power ground
15	SW2	Boost converter switching pin
16	VINA	Supply voltage for the device
—	Exposed Pad	Connect to the Ground layers on the PCB

Functional Block Diagram



Absolute Maximum Ratings

Symbol	Parameter	Ratings	Unit
VINP, VINA	Supply pin voltage	-0.3 to 6.5	V
SW1	Switch pin voltage	-0.3 to 6.5	
FBS	Feedback sense pin voltage	-0.3 to 6.5	
SW2	Switch pin voltage	-0.3 to 12.0	
V_{POS}	V_{POS} pin voltage	-0.3 to 6.5	
AV_{DD}	AV_{DD} pin voltage	-0.3 to 12.0	
V_{NEG}	V_{NEG} pin voltage	-6.5 to 0.3	
SW3	Switch pin voltage	-6.5 to 6.5	
PRG, EN, FD	PRG, EN, FD pin voltage	-0.3 to 6.5	
CT	CT pin voltage	-0.3 to 6.5	
T_J	Operating junction temperature	-40 to +150	°C
T_{ST}	Storage temperature	-65 to +150	

Caution: Stresses greater than those listed under *Absolute Maximum Ratings* can cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to *Absolute Maximum Ratings* for extended periods can affect device reliability.
Semiconductor devices are ESD sensitive and may be damaged by exposure to ESD events. Suitable ESD precautions should be taken when handling and transporting these devices.

ESD Ratings

Symbol	Parameter		Value	Unit
V_{ESD}	Electrostatic discharge	Human body model ESD protection	±2000	V
		Charge device mode ESD protection	1000	V

Package Thermal Data

Package	θ_{JC} Thermal Resistance Junction-to-Case	θ_{JA} Thermal Resistance Junction-to-Ambient	P_{DIS} T_A = +25°C, T_J = +125°C
U-QFN3030-16 (Type B)	3.3°C/W	42.9°C/W (Note 4)	1.5W

Recommended Operating Conditions

Symbol	Parameter	Min	Max	Unit
V_{IN}	Input supply voltage range	2.9	4.8	V
T_A	Operating ambient temperature range	-40	+85	°C

Note: 4. Test condition for U-QFN3030-16 (Type B): device mounted on 25.4mm x 25.4mm FR-4 PCB (10mm x 10mm 1oz copper, minimum recommended pad layout on top layer and thermal vias to bottom layer ground plane). For better thermal performance, larger copper pad for heatsink is needed.

Electrical Characteristics (V_{IN} = 3.7V, PRG = 3.7V, EN = 3.7V, V_{POS} = 4.6V, V_{NEG} = -2.5V, AV_{DD} = 6.1V, T_A = -40°C to +85°C, typical values are at T_A = +25°C, unless otherwise specified.)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Input Supply Section							
V_{IN}	Input voltage	—	T_A = -40°C to +85°C	2.9	3.7	4.8	V
V_{UVLO}	Undervoltage lockout threshold	V_{IN} falling	—	2.7	—	2.8	V
		V_{IN} rising	—	2.75	—	2.86	V
I_{SD}	Shutdown current	PRG = GND, EN = GND, sum of current flowing into VINA and VINP		—	0.3	1	µA
V_{POS} – Boost/Buck-Boost Converter							
V_{VPOS}	V_{POS} voltage	Default voltage	—	—	4.6	—	V
		Output accuracy	T_A = +25°C, No load	-0.5	—	0.5	%
			T_A = -40°C to +85°C, No load	-0.8	—	0.8	%
		Output range (100mV/step)	—	4.6	—	5.0	V
$R_{DS(on)1N}$	Switch on-resistance (nMOS)	$I_{(SW1)}$ = 200mA	—	—	250	—	mΩ
$R_{DS(on)1P}$	Rectifier on-resistance (pMOS)		—	—	350	—	mΩ
f_{SW1}	Switching frequency	I_{VPOS} = 500mA	—	—	1.5	—	MHz
I_{SW1}	Switch current limit	Inductor peak current	—	1.1	1.4	1.8	A
V_{SCP_VPOS}	Short-circuit threshold in operation	Percentage of V_{POS}	—	—	90	—	%
t_{SCP_VPOS}	Short-circuit detection time in operation	—	—	—	1	—	ms
V_T	FBS sense threshold	FBS increasing	—	200	300	400	mV
		FBS decreasing	—	100	200	300	mV
R_{DCHG1}	Discharge resistance	PRG = GND, FD = V_{IN} I_{VPOS} = 1mA	—	—	70	—	Ω
V_{RIPPLE_VPOS}	V_{POS} output voltage ripple	V_{IN} = 3.7V, V_{POS} = 4.6V I_{POS} = 500mA	—	—	20	—	mV
I_{LEAK_VPOS}	V_{POS} and FBS leakage, no discharge	FD = GND, PRG = GND	$V_{POS} \le V_{IN}$	—	0.1	—	µA
—	Line regulation	I_{POS} = 500mA	—	—	0.03	—	%/V
—	Load regulation	V_{IN} = 3.7V 0mA ≤ I_{POS} ≤ 500mA	100mA ≤ I_{POS} ≤ 500mA	—	0.08	—	%/A
			0mA ≤ I_{POS} ≤ 500mA	—	0.1	—	
AV_{DD} – Boost Converter							
V_{AVDD}	V_{AVDD} voltage	Default voltage	—	—	7.6	—	V
		Output accuracy	T_A = +25°C, No load	-0.5	—	0.5	%
			T_A = -40°C to +85°C, No load	-1.0	—	1.0	%
		Output range (300mV/step)	—	5.8	—	7.9	V
$R_{DS(on)2N}$	Switch on-resistance (nMOS)	$I_{(SW2)}$ = 100mA	—	—	300	—	mΩ
$R_{DS(on)2P}$	Rectifier on-resistance (pMOS)		—	—	450	—	mΩ
f_{SW2}	Switching frequency	I_{AVDD} = 100mA	—	—	1.5	—	MHz
V_{SCP_AVDD}	Short-circuit threshold in operation	Percentage of nominal AV_{DD}	—	—	90	—	%
t_{SCP_AVDD}	Short-circuit detection time in operation	—	—	—	1	—	ms
I_{SW2}	Switch current limit	Inductor peak current	—	0.45	0.65	0.85	A
V_{RIPPLE_AVDD}	AV_{DD} output voltage ripple	V_{IN} = 3.7V, AV_{DD} = 7.6V I_{AVDD} = 100mA	—	—	20	—	mV
I_{LEAK_AVDD}	AV_{DD} leakage, no discharge	FD = GND, EN = GND	$AV_{DD} \le V_{IN}$	—	0.3	—	µA
R_{DCHG2}	Discharge resistance	EN = GND, FD = V_{IN} I_{AVDD} = 1mA	—	—	70	—	Ω
—	Line regulation	I_{AVDD} = 30mA	—	—	0.05	—	%/V
—	Load regulation	0mA ≤ I_{AVDD} ≤ 100mA	50mA ≤ I_{AVDD} ≤ 100mA	—	0.5	—	%/A
			0mA ≤ I_{AVDD} ≤ 100mA	—	0.5	—	

Electrical Characteristics (V_{IN} = 3.7V, PRG = 3.7V, EN = 3.7V, V_{POS} = 4.6V, V_{NEG} = -2.5V, AV_{DD} = 6.1V, T_A = -40°C to +85°C, typical values are at T_A = +25°C, unless otherwise specified.) (continued)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{NEG} – Inverting Buck-Boost Converter							
V_{VNEG}	V_{VNEG} voltage	Default voltage	—	—	-4.0	—	V
		Output accuracy	T_A = +25°C	-0.5	—	0.5	%
			T_A = -40°C to +85°C	-0.8	—	0.8	%
		Output range (100mV/step)	—	-1.4	—	-5.4	V
$R_{DS(on)3P}$	Switch on-resistance (pMOS)	$I_{(SW3)}$ = 200mA	—	—	200	—	mΩ
$R_{DS(on)3N}$	Rectifier on-resistance (nMOS)		—	—	300	—	mΩ
f_{SW3}	Switching frequency	I_{NEG} = 500mA	—	—	1.5	—	MHz
I_{SW3}	Switch current limit	Inductor peak current	—	1.5	2.0	2.75	A
V_{SCP_VNEG}	Short-circuit threshold in operation	Voltage increase from nominal V_{NEG}	—	—	530	—	mV
	Short-circuit threshold in startup	—	—	—	250	—	mV
t_{SCP_VNEG}	Short-circuit detection time in operation	—	—	—	1	—	ms
	Short-circuit detection time in startup	—	—	—	10	—	ms
I_{LEAK_VNEG}	V_{NEG} leakage, no discharge	FD = GND, EN = GND	V_{NEG} = 0V	—	0.1	—	μA
V_{RIPPLE_VNEG}	V_{NEG} output voltage ripple	V_{IN} = 3.7V, V_{NEG} = -4.0V I_{AVDD} = 500mA	—	—	20	—	mV
R_{DCHG3}	Discharge resistance	PRG = GND, FD = V_{IN} I_{VNEG} = 1mA	—	—	70	—	Ω
—	Line regulation	I_{NEG} = 500mA	—	—	0.03	—	%/V
—	Load regulation	V_{NEG} = -5V 1mA ≤ I_{NEG} ≤ 500mA	100mA ≤ I_{NEG} ≤ 500mA	—	1.6	—	%/A
			1mA ≤ I_{NEG} ≤ 500mA	—	2.0	—	
Logic Interface (PRG, EN, FD)							
V_{IH}	Logic input high level voltage	—	—	1.2	—	—	V
V_{IL}	Logic input low level voltage	—	—	—	—	0.4	V
R	Pulldown resistance	—	—	250	500	900	kΩ
Other							
T_{SHDN}	Thermal shutdown	Junction temperature	—	—	+150	—	°C
T_{HYS}	Thermal shutdown hysteresis	—	—	—	+10	—	°C
PRG Timing Interface Section (PRG, EN, FD)							
t_{INIT}	Initialization time			—	300	—	μs
t_{STORE}	Data storage time			30	—	80	μs
t_{LOW}	Low-level pulse duration			2	10	25	μs
t_{HIGH}	High-level pulse duration			2	10	25	μs
t_{OFF}	Shutdown time			30	—	80	μs

Performance Characteristics (V_{IN} = 3.7V, T_A = +25°C with components as Figure 20, unless otherwise specified.)

Test conditions: AV_{DD} = 7.6V, EN = HIGH, PRG = LOW

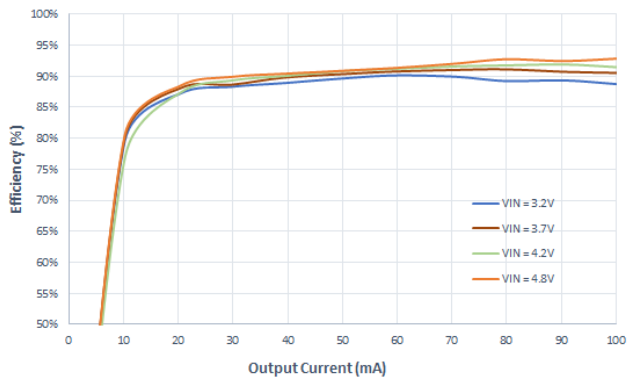


Figure 1. AV_{DD} Efficiency vs. Output Current

V_{POS} = 4.6V, V_{NEG} = -4V, EN = LOW, PRG = HIGH

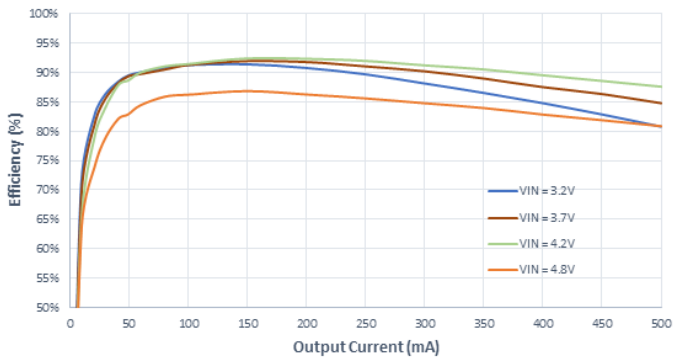


Figure 2. V_{POS} & V_{NEG} Efficiency vs. Output Current

Test conditions: V_{IN} = 3.7V, No Load, PRG = HIGH, EN = LOW

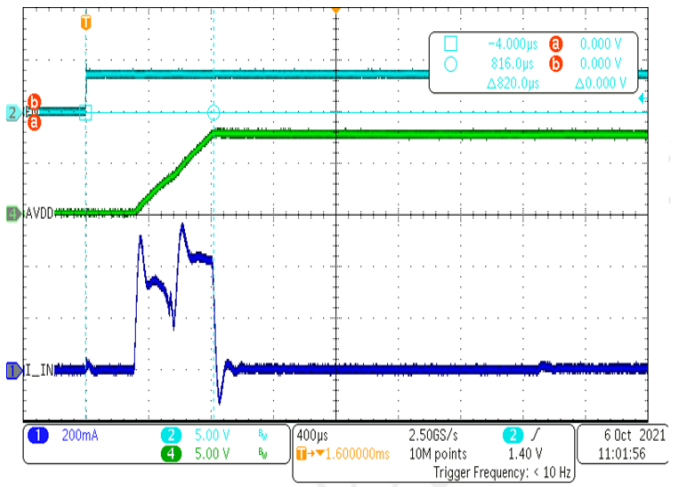


Figure 3. AV_{DD} Startup Waveform

V_{IN} = 3.7V, No Load, PRG = LOW, EN = HIGH

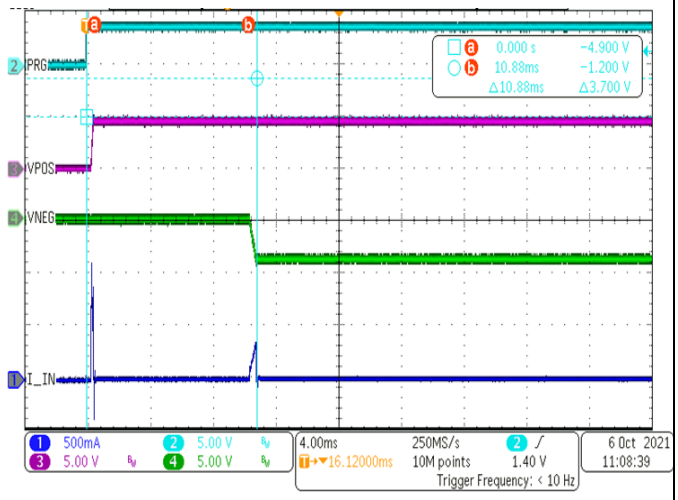


Figure 4. V_{POS} & V_{NEG} Startup Waveform

Test conditions: V_{POS} V_{NEG} with Fast Discharge (FD) = OFF

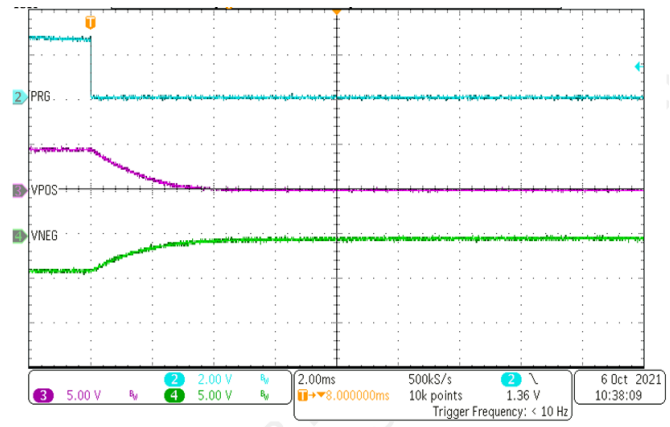


Figure 5. V_{POS} & V_{NEG} Shutdown Waveform with FD ON

V_{POS} V_{NEG} with Fast Discharge (FD) = ON

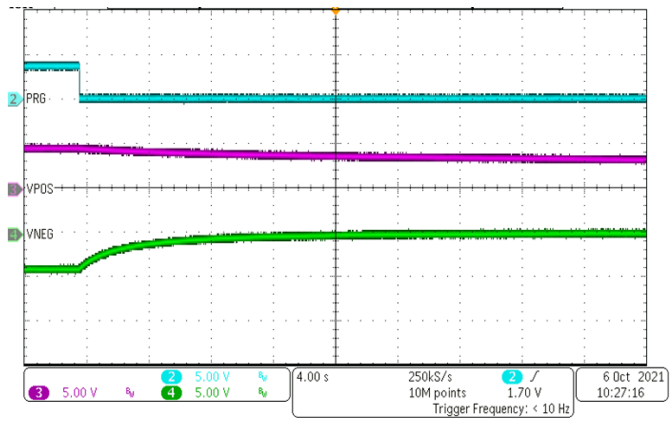


Figure 6. V_{POS} & V_{NEG} Shutdown Waveform with FD OFF

Performance Characteristics (V_{IN} = 3.7V, T_A = +25°C with components as Figure 20, unless otherwise specified.) (continued)

Test conditions: V_{POS} Boost, V_{POS} = 4.6V / 100mA load

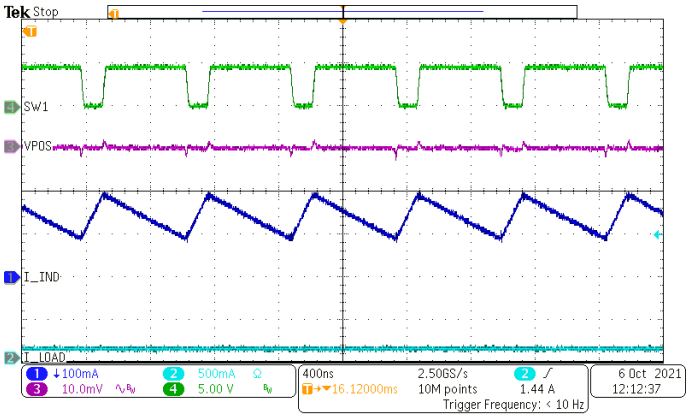


Figure 7. Switch Pin, V_{POS} Output Ripple, Inductor & Output Current

V_{POS} Boost, V_{POS} = 4.6V / 300mA load

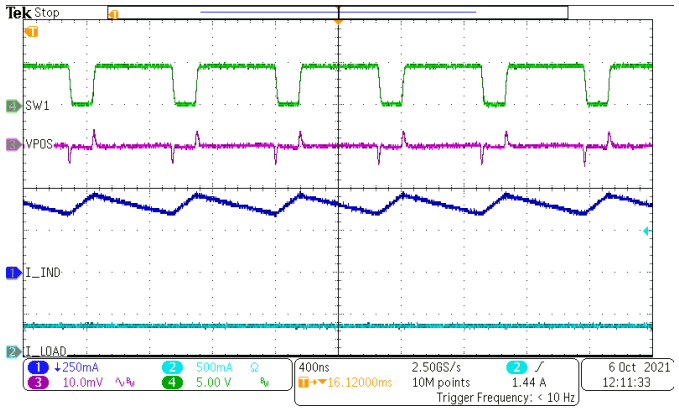


Figure 8. Switch Pin, V_{POS} Output Ripple, Inductor & Output Current

Test conditions: V_{POS} Boost, V_{POS} = 4.6V / 500mA load

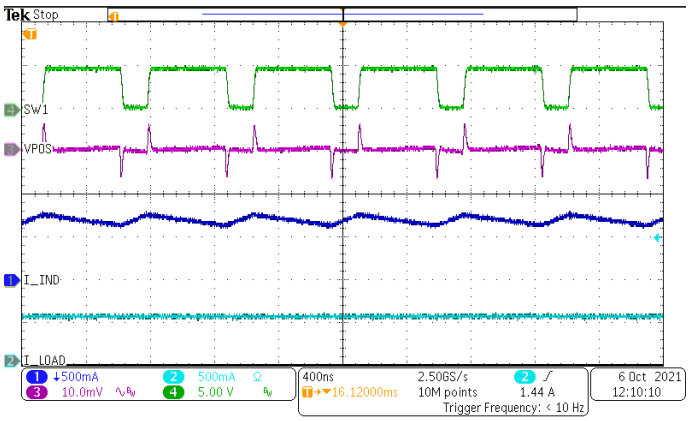


Figure 9. Switch Pin, V_{POS} Output Ripple, Inductor & Output Current

V_{NEG} = -4.0V / 100mA load

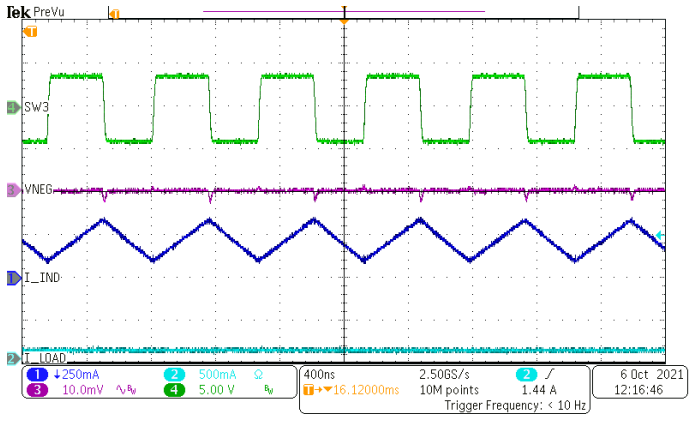


Figure 10. Switch Pin, V_{NEG} Output Ripple, Inductor & Output Current

Test conditions: V_{NEG} = -4.0V / 300mA load

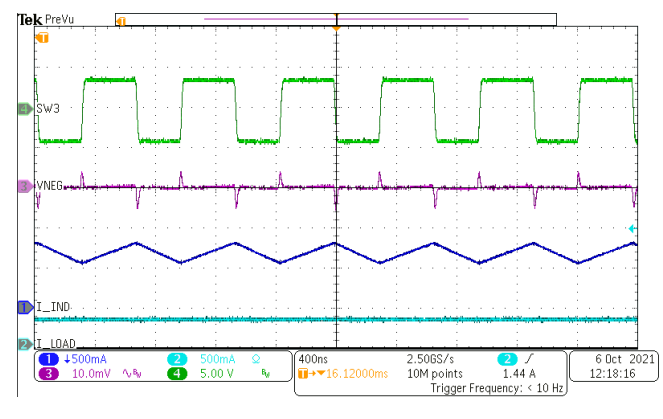


Figure 11. Switch Pin, V_{NEG} Output Ripple, Inductor & Output Current

V_{NEG} = -4.0V / 500mA load

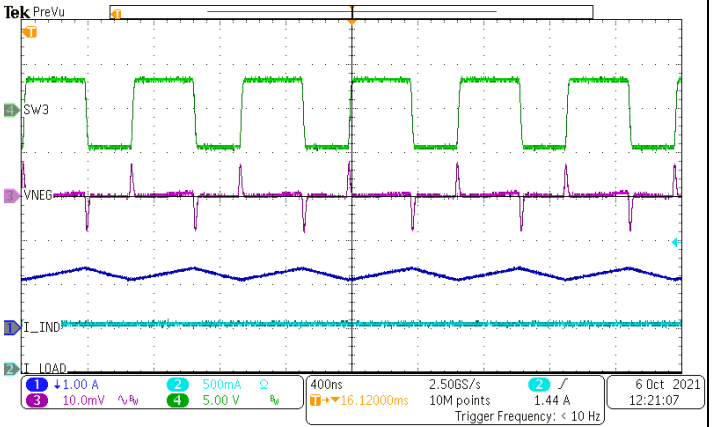


Figure 12. Switch Pin, V_{NEG} Output Ripple, Inductor & Output Current

Performance Characteristics (V_{IN} = 3.7V, T_A = +25°C with components as Figure 20, unless otherwise specified.) (continued)

Test conditions: AV_{DD} = 7.6V / 50mA load

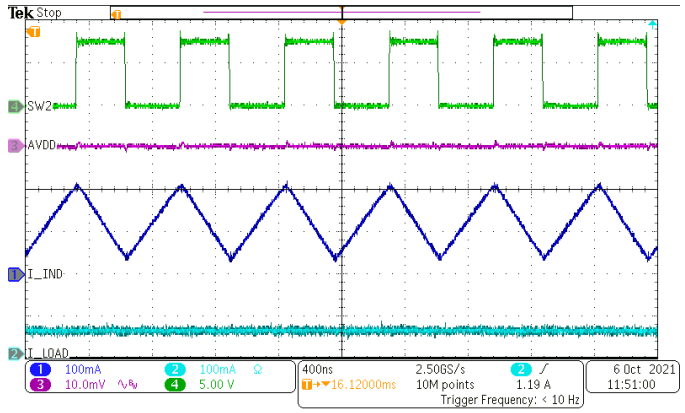


Figure 13. Switch Pin, AV_{DD} Output Ripple, Inductor & Output Current

AV_{DD} = 7.6V / 100mA load

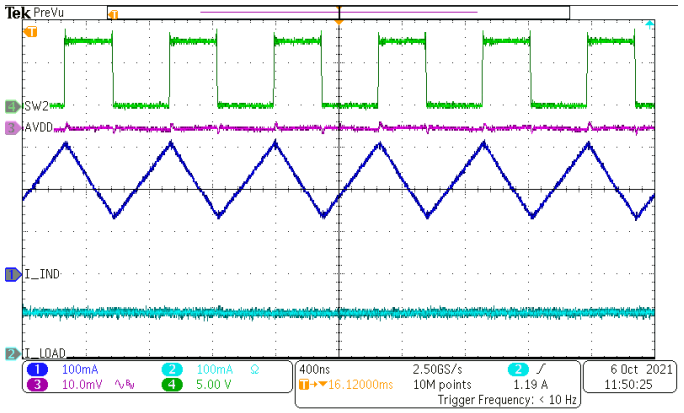


Figure 14. Switch Pin, AV_{DD} Output Ripple, Inductor & Output Current

Function Description

The AL3565 consists of two boost converters and an inverting buck-boost converter. The V_{POS}, V_{NEG} and AV_{DD} outputs are all programmable through the PRG digital pin. The V_{POS} output range is from 4.6V to 5.0V, default 4.6V. The V_{NEG} output range is from -5.4V to -1.4V, default -2.5V. The AV_{DD} output range is from 5.8V to 7.9V, default 6.1V. Fast discharge function is on/off controlled by FD pin

1.0 Startup Sequence, Soft-Start and Shutdown

The device features a soft-start function to limit the inrush current. The AV_{DD} boost converter is enabled when EN goes high. When PRG goes high, the V_{POS} boost/buck-boost converter starts and 10ms later the inverting buck-boost converter (V_{NEG}) starts with its default value. The typical startup sequence with fast discharge is shown in Figure 15. The AV_{DD} boost converter, and the V_{POS} boost converter operate independently. The AV_{DD} boost converter does not require the V_{POS} boost converter to be in regulation in order for it to start.

Before the first startup, the output discharge is undefined and the output discharge is activated by PRG rising edge, following the FD configuration. When the converters shut down, the outputs are discharged if FD function is enabled or the outputs are high impedance if FD function is disabled.

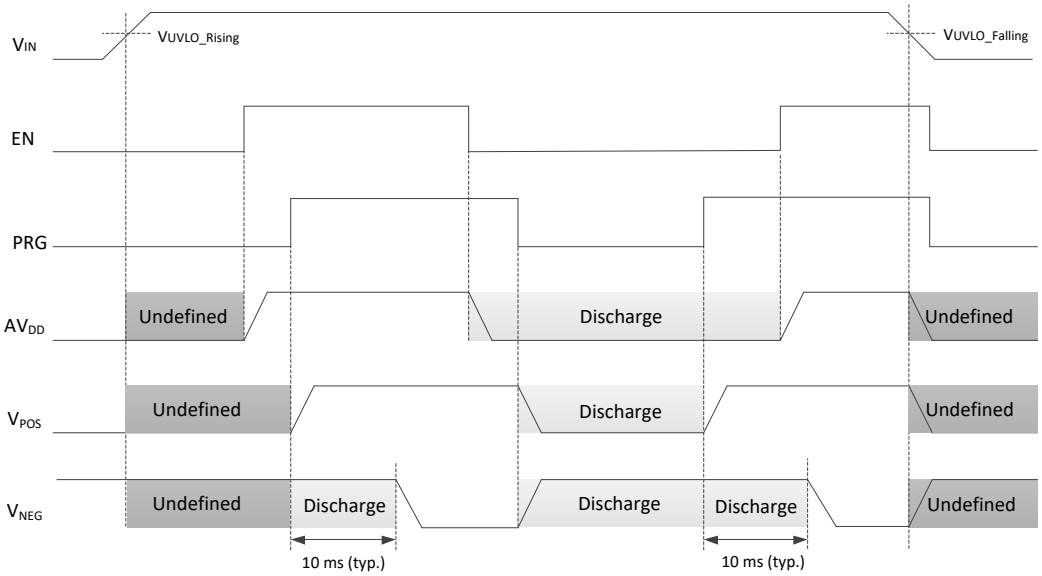


Figure 15. Startup and Shutdown Sequence with Fast Discharge

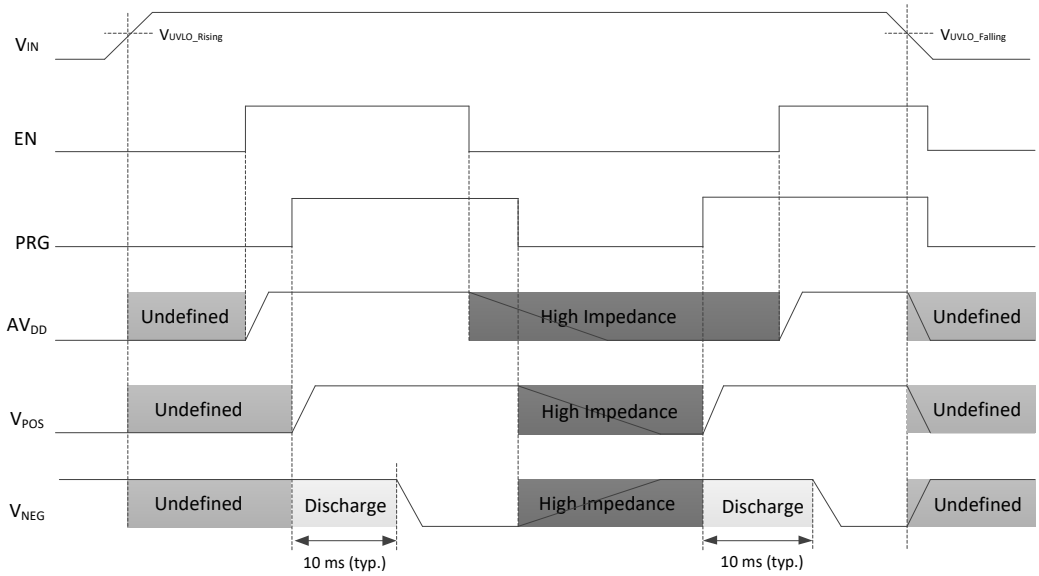


Figure 16. Startup and Shutdown Sequence Without Fast Discharge

Function Description (continued)

1.1 Programming V_{POS}, V_{NEG} and AV_{DD} Output Voltage through PRG Pin

All the output voltage of AL3565 can be programmed through PRG pin. If programming is not required the PRG pin can also be used as a standard enable pin. Once the device is enabled, AL3565 starts with its default values. The interface counts the rising edges applied to the PRG pin and sets the new values. Table 1 to 3 listed the mapping for the rising edge numbers and the corresponding the output voltage.

The settings are stored in a volatile memory, they are reset as follows:

- A power cycle resets all settings to default values.
- Enabling the V_{POS} boost/buck-boost converter sets the output discharge. (The output discharge function is controlled by FD pin.)
- If PRG is low for a min. t_{OFF}, V_{NEG} will be reset to default value and V_{POS} will be reset to default value.
- If EN and PRG are low at the same time for min. t_{OFF}, AV_{DD} will be reset to its default value. If EN is low and PRG is high, AV_{DD} retains its programmed value.

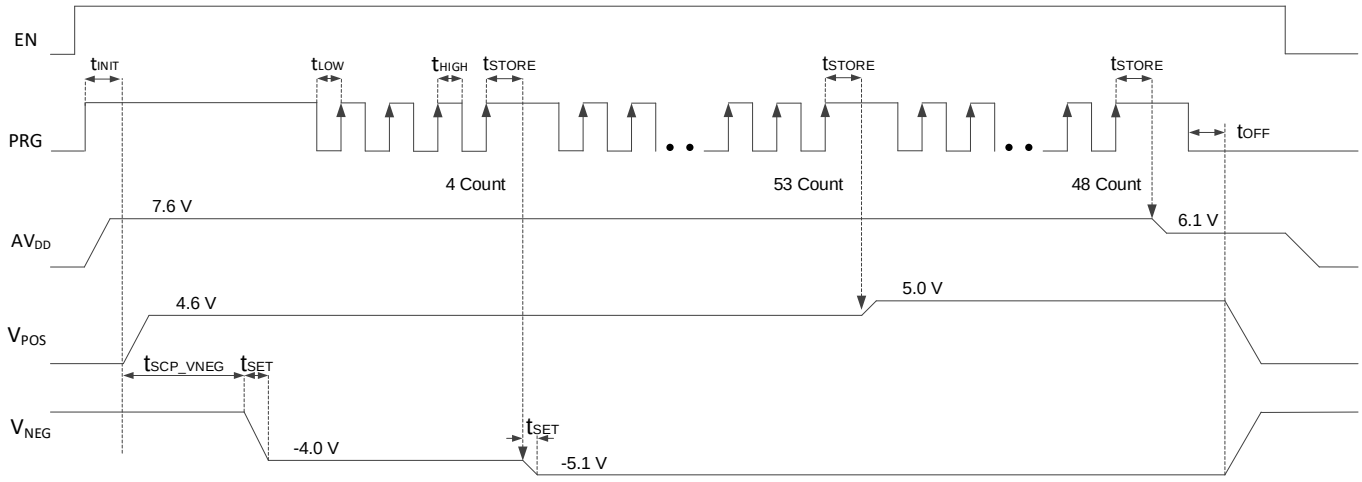


Figure 17. Digital Interface Using PRG Pin

Function Description (continued)

2.0 V_{POS} – Boost/Buck-Boost Converter

The boost/buck-boost converter V_{POS} uses a fixed-frequency current-mode topology. Its default output voltage V_{POS} is (4.6V) for AL3565. V_{POS} can be programmed through the digital PRG pin. For higher output voltage accuracy, connect the output sense pin (FBS) directly to the positive terminal of the main output capacitor. If not used, the FBS pin shall be tied to ground.

2.1 V_{POS} – Asynchronous Buck-Boost Mode

When V_{POS} is close to V_{IN}, AL3565 enters asynchronous buck-boost mode. In this mode, the high-side power pMOS channel is turned off completely and the power pMOS body diode is used for the conduction.

2.2 V_{POS} – Boost Converter, Output Sense (FBS pin)

The positive output boost circuitry has a dedicated output pin (FBS). If FBS is floating or tied to ground, the positive output boost circuitry senses the output through the V_{POS} pin.

2.3 V_{POS} Voltage Control by PRG Pin

When the PRG pin is pulled high while the device is enabled, V_{POS} will rise to its default voltage of 4.6V. While the device is enabled, the digital programming interface counts the number of rising edges applied to the PRG pin. Table 1 shows the pulse count for a corresponding programmed V_{POS} voltage. V_{POS} can be programmed in 100mV steps.

Bit / Rising Edges	V_{POS}
Default	4.6V
54	4.7V
55	4.8V
56	4.9V
57	5.0V
64	4.6V

Table 1. Programing Table for AL3565 V_{POS}

Function Description (continued)

3.0 AV_{DD} – Boost Converter

Boost converter uses a fixed-frequency current-mode topology. Its default output voltage AV_{DD} is (6.1V) for AL3565. AV_{DD} can be programmed through the digital PRG pin.

3.1 AV_{DD} Voltage Control by PRG Pin

Once the device is enabled using the EN pin, AV_{DD} will rise to its default value. While the device is enabled, the digital programming interface counts the number of rising edges applied to the PRG pin. Table 2 shows the pulse count for a corresponding programmed AV_{DD} voltage. AV_{DD} can be programmed in 300mV steps.

Bit / Rising Edges	AV_{DD}
Default	7.6V
42	7.9V
43	7.6V
44	7.3V
45	7.0V
46	6.7V
47	6.4V
48	6.1V
49	5.8V

Table 2. Programing Table for AL3565 AV_{DD}

Function Description (continued)

4.0 V_{NEG} – Inverting Buck-Boost Converter

The inverting buck-boost converter uses a peak current PWM control topology. Its default output voltage V_{NEG} is (-2.5V) for AL3565. V_{NEG} can be programmed through the digital PRG pin.

4.1 V_{NEG} Voltage Control by PRG Pin

When the PRG pin is pulled high while the device is enabled, V_{NEG} will fall to its default value. While the device is enabled, the digital programming interface counts the number of rising edges applied to the PRG pin. Table 3 shows the pulse count for a corresponding programmed V_{NEG} voltage. V_{NEG} can be programmed in 100mV steps.

Bit / Rising Edges	V_{VNEG}	Bit / Rising Edges	V_{VNEG}
Default	-4.0V	21	-3.4V
1	-5.4 V	22	-3.3V
2	-5.3 V	23	-3.2V
3	-5.2 V	24	-3.1V
4	-5.1V	25	-3.0V
5	-5.0V	26	-2.9V
6	-4.9V	27	-2.8V
7	-4.8V	28	-2.7V
8	-4.7V	29	-2.6V
9	-4.6V	30	-2.5V
10	-4.5V	31	-2.4V
11	-4.4V	32	-2.3V
12	-4.3V	33	-2.2V
13	-4.2V	34	-2.1V
14	-4.1V	35	-2.0V
15	-4.0V	36	-1.9V
16	-3.9V	37	-1.8V
17	-3.8V	38	-1.7V
18	-3.7V	39	-1.6V
19	-3.6V	40	-1.5V
20	-3.5V	41	-1.4V

Table 3. Programing Table for AL3565 V_{NEG}

Function Description (continued)

5.0 FD Control

When PRG is pulled high, the fast discharge (FD) function will be initialized to its default state according to the FD pin. If the FD pin is connected to GND, fast discharge is disabled and all outputs are high impedance. If the FD pin is connected to HIGH (HIGH > 1.2V), fast discharge is enabled and all outputs are discharged.

The fast discharge function can also be controlled through the PRG pin, which would override the FD pin connection setting. Table 4 shows the pulse rising edges count for a corresponding programmed FD function (ON/OFF).

Bit / Rising Edges	FD Pin	FD	Comment
Default / 0	HIGH	ON	Using FD pin
	GND	OFF	Using FD pin
50	X	ON	Using PRG pin
51	X	OFF	Using PRG pin

Table 4. Programming Table for FD Control

Only in the "Yellow Highlighted" area, we can use pulses applied to PRG pin to disable/enable fast discharge, no matter how FD pin is configured. As shown, V_{NEG} always needs Fast Discharge active at power-up.

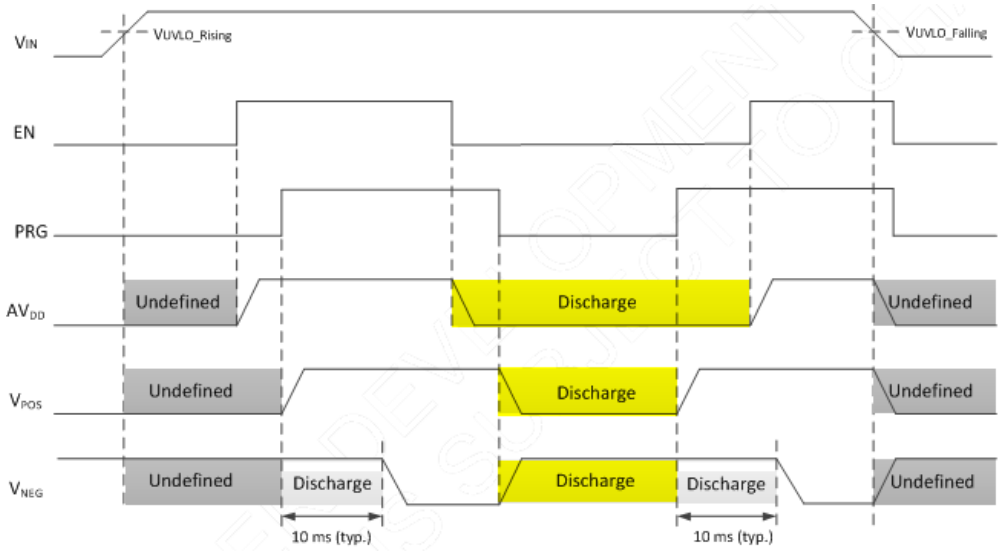


Figure 18. Fast Discharge sequence with FD = high, but discharge can be disabled by PRG (Table 4) in yellow highlighted area

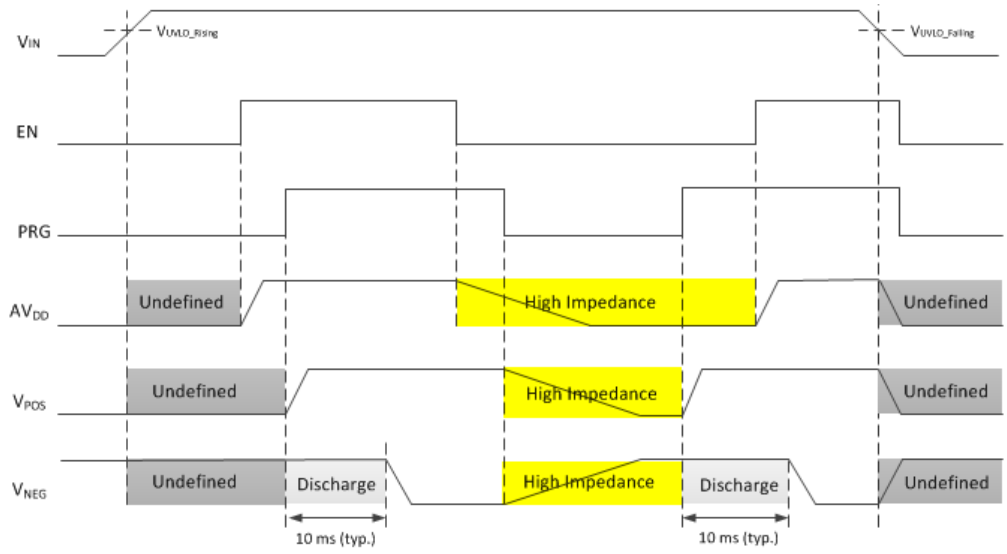


Figure 19. Without Fast Discharge sequence with FD = low, but discharge can be enabled by PRG (Table 4) in yellow highlighted area

Function Description (continued)

6.0 Short-Circuit Protection (SCP)

AL3565 detects short and shuts down in one of the below conditions:

- AV_{DD} falls below 90% of its programmed voltage for more than 1ms after power-up: shutdown $V_{POS}/V_{NEG}/AV_{DD}$
- V_{POS} falls below 90% of its programmed voltage for more than 1ms after power-up: shutdown $V_{POS}/V_{NEG}/AV_{DD}$
- V_{NEG} rises above 500mV of its programmed voltage longer than 1ms: shutdown $V_{POS}/V_{NEG}/ AV_{DD}$
- V_{NEG} > 200mV (during startup) when V_{NEG} is enabled (10ms after PRG = HIGH): shutdown V_{POS} and V_{NEG} only

The shutdown state is latched, and the input and outputs are disconnected. To restart the device, V_{IN} must cycle below UVLO or EN and PRG have to be low at the same time for 80µs (t_{OFF} max spec) or longer.

See Section 7 – *Inductor/Capacitor Selection* for recommended inductor & capacitor values.

6.1 Thermal Shutdown

The AL3565 device enters thermal shutdown if its junction temperature exceeds +150°C (typical). During thermal shutdown none of the device's functions are available, but the programming data is not lost. When the temperature decreases to +140°C (typical), the device automatically restarts performing the startup sequencing with the same voltages and programming as programmed before the thermal shutdown.

Application Information

7.0 Inductor/Capacitor Selection

The AL3565 is designed for supplying power to AMOLED display in smart phone applications. The circuit inputs power from a single-cell Li-ion battery and generates an adjustable power supply AV_{DD}, an adjustable positive output voltage V_{POS} and an adjustable negative output voltage V_{NEG}.

The AV_{DD} boost converter typically requires a 10µH inductor, V_{POS} and V_{NEG} require a 4.7µH. The input and output capacitors are usually ceramic capacitors. Table 5 lists the recommended component for typical circuit configurations. Please contact us for any further components optimizations on either efficiency or sizes.

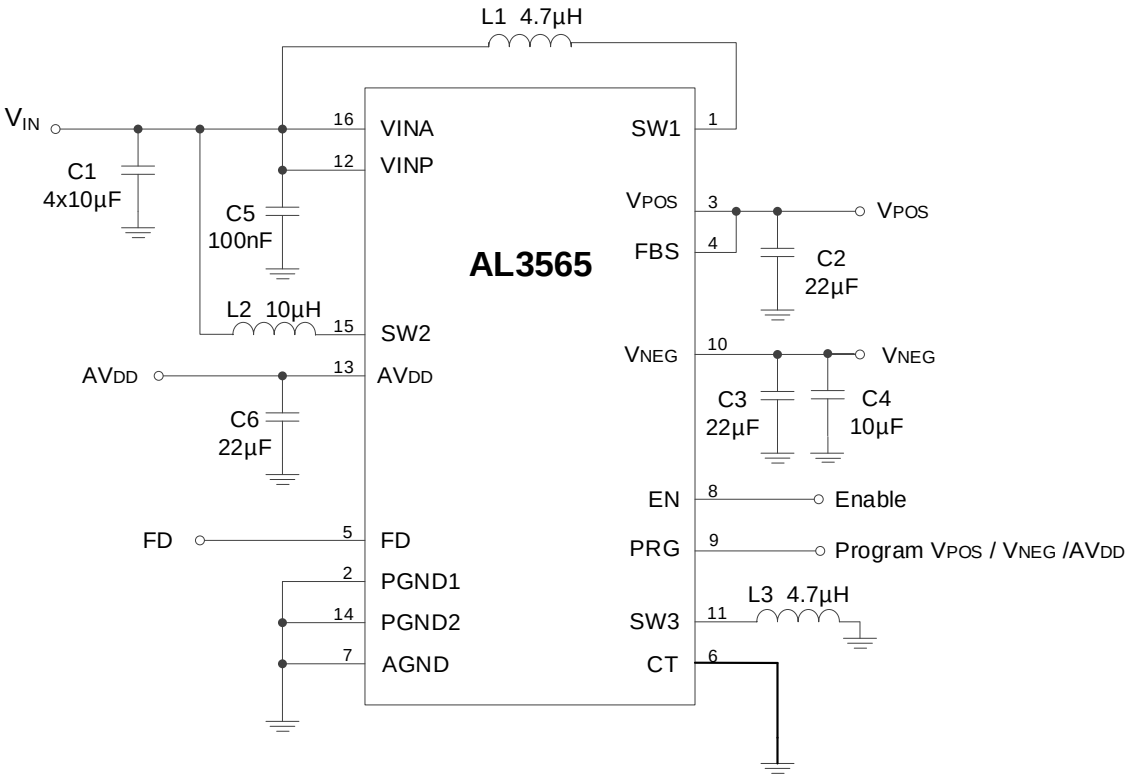


Figure 20. Typical Application Circuit

The AL3565 is designed to operate with the input voltage ranging from 2.9V to 4.8V. If the input supply is located more than a few centimeters from the AL3565, additional bulk capacitors may be needed. The (4) 10µF (C1) capacitors shown in the typical application circuit are a common choice.

Component	Designator	Value	Part Number	Manufacturer
AV_{DD} inductor	L2	10µH±20%	DFE252012C-100M	TOKO
V_{POS} and V_{NEG} inductor	L1, L3	4.7µH±20%	DFE252012F-4R7M	muRata
			DFE252012P-4R7N	TOKO
V_{IN} capacitor	C1	10µF±20% / 10V / 0805	GRM219R61A106ME47	muRata
AV_{DD} capacitor	C6	22µF±20% / 25V / 0805	CL21A226MPCLRNC	muRata
V_{POS} capacitor	C2	22µF±20% / 25V / 0805	CL21A226MPCLRNC	muRata
V_{NEG} capacitor	C3, C4	22µF±20% / 25V / 0805 10µF±20% / 25V / 0805	CL21A226MPCLRNC GRM219R61A106ME47	muRata

Table 5. Component Selection Table

Application Information (continued)

8.0 Layout Guidelines

1. Place the input capacitor on VINP and the output capacitor on V_{NEG} as close as possible to device. Use short and wide traces to connect the input capacitor on VINP and the output capacitor on V_{NEG}.
2. Place the output capacitor on V_{POS} and AV_{DD} as close as possible to device. Use short and wide traces to connect the output capacitor on V_{POS} and AV_{DD}.
3. Connect the ground of CT capacitor with AGND (pin 7) directly.
4. Connect input ground and output ground on the same board layer, not through via hole.
5. Connect AGND, PGND1 and PGND2 with exposed thermal pad.

8.1 Layout Example

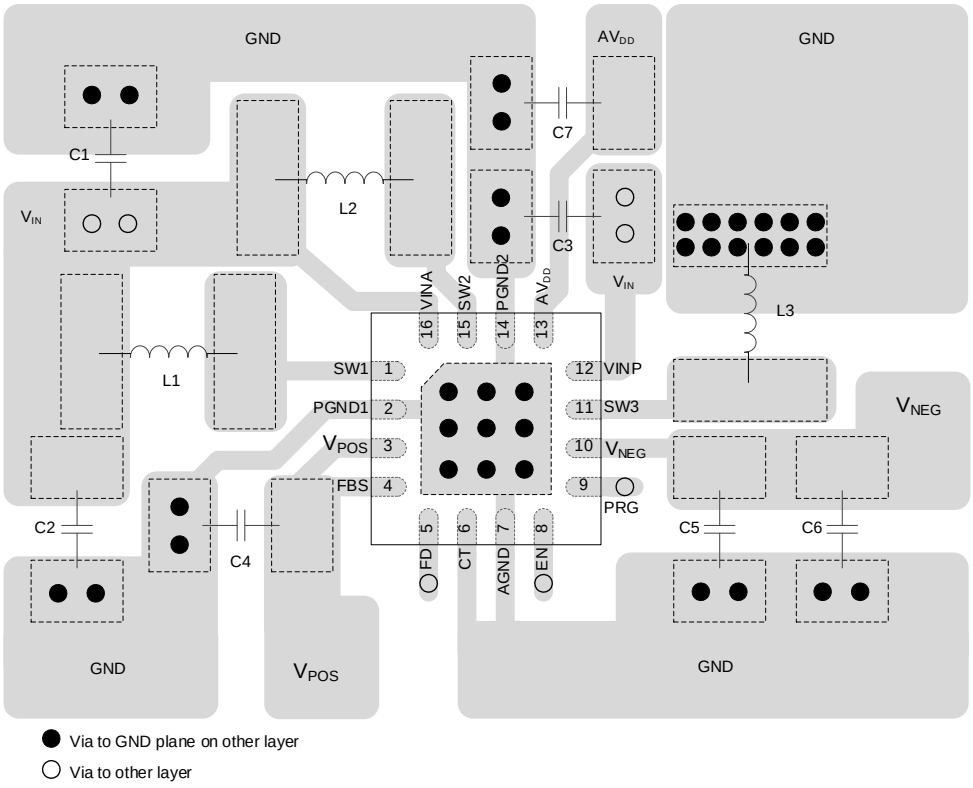
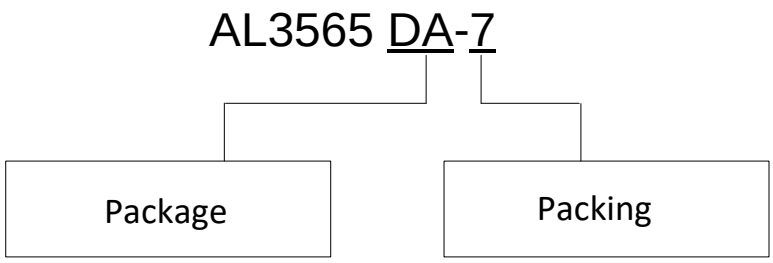


Figure 21. Recommended PCB Layout

Design Tools

- Demo Board
- Calculator
- Demo Board Gerber File of PCB Layout Reference
- PSPICE

Ordering Information



DA : U-QFN3030-16 (Type B) 7 : Tape & Reel

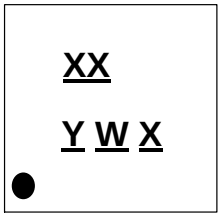
Part Number	Part Number Suffix	Package Code	Package (Note 5)	Packing	
				Qty.	Carrier
AL3565DA-7	-7	DA	U-QFN3030-16 (Type B)	1,500	Tape & Reel

Note: 5. For packaging details, go to our website at https://www.diodes.com/design/support/packaging/diodes-packaging/.

Marking Information

U-QFN3030-16 (Type B)

(Top View)



XX : Identification Code

Y : Year : 0 to 9 (ex: 3 = 2023)

W : Week : A to Z : week 1 to 26;
a to z : week 27 to 52;
z represents week 52 and 53

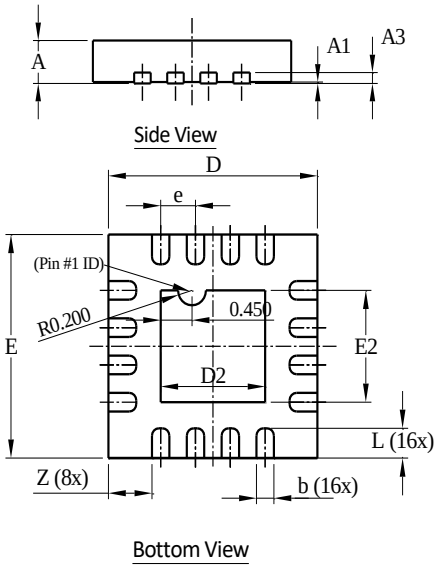
X : A to G : Green

Part Number	Package	Identification Code
AL3565DA-7	U-QFN3030-16 (Type B)	S9

Package Outline Dimensions

Please see http://www.diodes.com/package-outlines.html for the latest version.

U-QFN3030-16 (Type B)

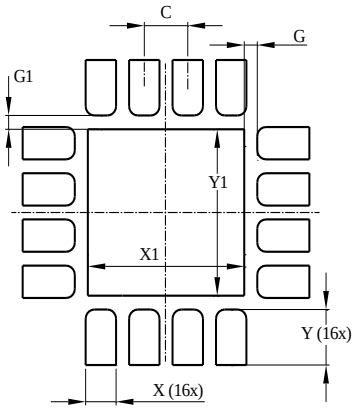


U-QFN3030-16 Type B			
Dim	**Min**	**Max**	**Typ**
A	0.55	0.65	0.60
A1	0	0.05	0.02
A3	-	-	0.15
b	0.18	0.28	0.23
D	2.95	3.05	3.00
D2	1.40	1.60	1.50
E	2.95	3.05	3.00
E2	1.40	1.60	1.50
e	-	-	0.50
L	0.35	0.45	0.40
Z	-	-	0.625
All Dimensions in mm			

Suggested Pad Layout

Please see http://www.diodes.com/package-outlines.html for the latest version.

U-QFN3030-16 (Type B)



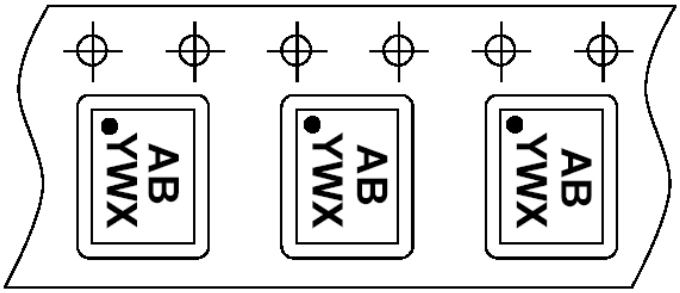
Dimensions	Value (in mm)
C	0.500
G	0.150
G1	0.150
X	0.350
X1	1.800
Y	0.600
Y1	1.800

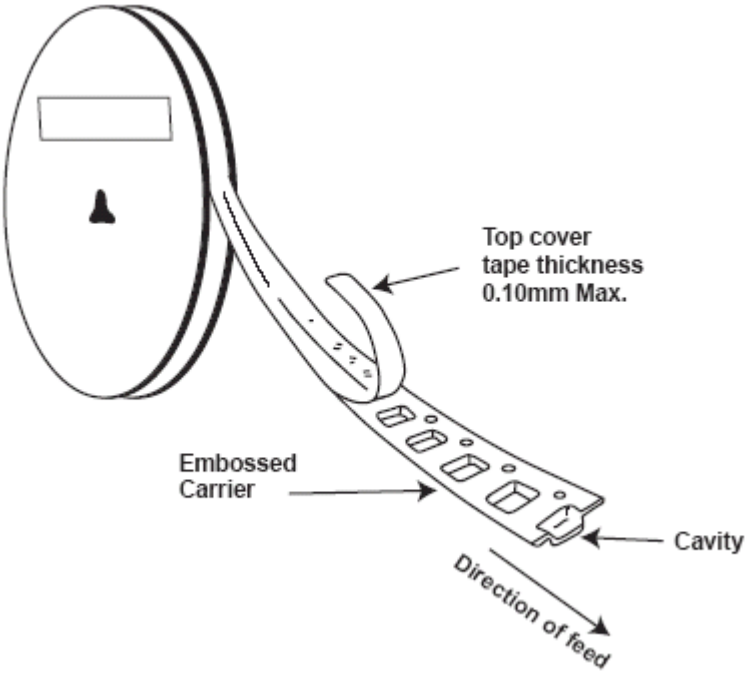
Mechanical Data

- Moisture Sensitivity: Level 1 per JESD22-A113
- Terminals: Finish - Preplated NiPdAu, Solderable per JESD22-B102 (e4)
- Weight: 0.017 grams (Approximate)

Taping Orientation

The taping orientation of other package type can be found on our website at https://www.diodes.com/assets/Packaging-Support-Docs/ap02007.pdf.





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