Description

The AL8890/AL88902 is a synchronous buck converter with internal compensation and switching frequency adjustable up to 2.5MHz. The device integrates a 120mΩ high-side power MOSFET and a 55mΩ low-side power MOSFET to provide high-efficiency DC-DC conversion.

The AL8890 enables a continuous load current of up to 3.5A (the AL88902 up to 2.5A) with efficiency as high as 95% in enhanced biased. The device features current-mode control operation, which enables easy loop stabilization supporting a wide range of output loading, suitable for both CV (constant voltage) and CC (constant current) applications.

The AL8890/AL88902 simplifies board layout and reduces space requirements with its high switching frequency and use of smaller size inductor and built-in MOSFET, making it ideal for power management.

The AL8890/AL88902 is available in wettable flank U-QFN4040-16/SWP (Type UXB) package.

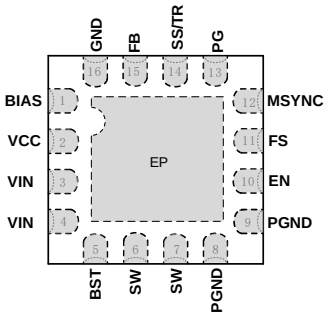
Features

- V_{IN} 3.8V to 60V
- Wide V_{OUT} Range: 0.8V to near 100% of V_{IN}
- V_{OUT} 1% Accuracy
- V_{FB} Adjustable Through SS/TR Pin
- Synchronous Rectification > 95% Efficiency @12V
  - High-Side (120mΩ) Power MOSFET
  - Low-Side (55mΩ) Power MOSFET
- Low Quiescent Current 43μA
- Switching Frequency 300kHz to 2.5MHz
- Force PWM or PFM Mode Through MYSNC
- Synchronization to External Clock
- Programmable Startup Control
  - Startup with Pre-Biased Output
  - External Soft-Start with Tracking
  - High-Voltage Enable Pin with High Precision
- Protection and Diagnosis Functions
  - Power-Good (PG) Detection
  - Thermal Shutdown Protection
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**
- **An automotive-compliant part is available under separate datasheet (AL8890Q/AL88902Q)**

Pin Assignments

(3D Step File Available)

(Top View – Not to Scale)



U-QFN4040-16/SWP (Type UXB)

Device Information

Orderable Part Number	Package	Body Size (Typ)
AL8890FVBW-13	U-QFN4040-16/SWP (Type UXB)	4.0mm × 4.0mm
AL88902FVBW-13	U-QFN4040-16/SWP (Type UXB)	4.0mm × 4.0mm

Applications

- LED lighting systems
- Telecommunications
- White appliances
- Network systems

Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

Typical Applications Circuit

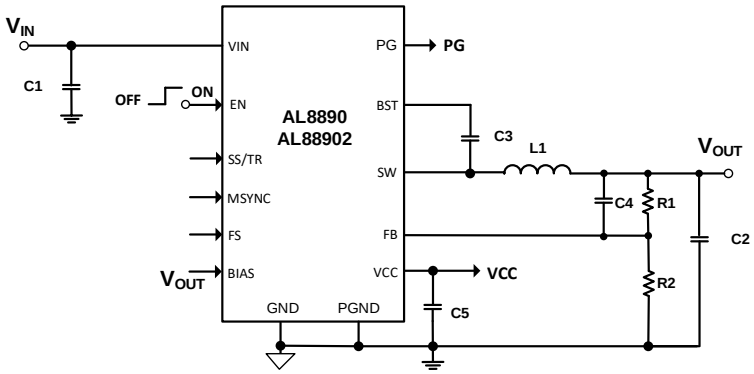


Figure 1. Typical Application Circuit for Constant Voltage Output

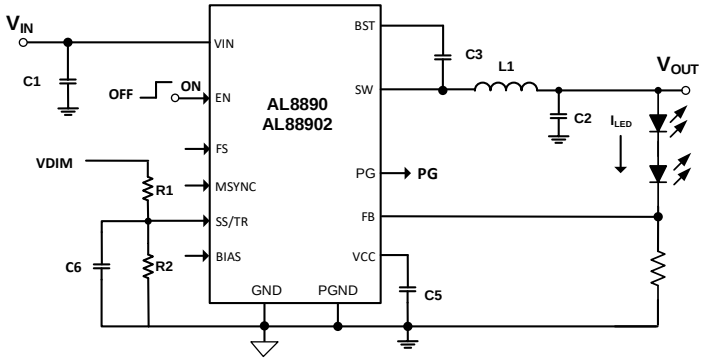


Figure 2. Typical Application Circuit for Constant Current Output

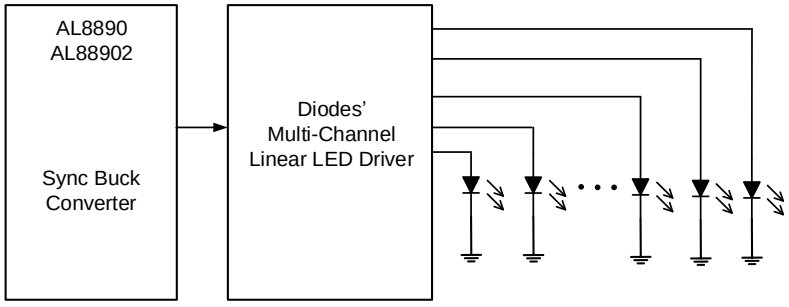


Figure 3. Typical Application for Two-Stage LED Driver

Pin Descriptions

Pin Name	Pin Number	Function
BIAS	1	The internal regulator will draw current from BIAS instead of VIN when BIAS is tied to a voltage higher than 4.4V. For output voltages of 5V to 15V, this pin can be tied to V_{OUT}. If this pin is tied to a supply other than V_{OUT}, use a 1µF local bypass capacitor on this pin. If no supply is available, this pin should be tied to PGND.
VCC	2	Internal 5V LDO output pin to connect an additional capacitor. Connect a 1µF (typical) capacitor as close as possible to the VCC and PGND. This pin is not active when EN is low.
VIN	3, 4	Power Input. VIN supplies the power to the IC, as well as the step-down converter switches. Drive VIN with a 3.8V to 60V power source. Bypass VIN to GND with a suitably large capacitor to eliminate noise on the input to the IC. See *Input Capacitor*.
BST	5	High-Side Gate Drive Boost Input. BST supplies the drive for the high-side n-channel MOSFET with a 0.1µF or greater capacitor from SW to BST to power the high-side switch.
SW	6, 7	Power Switching Output. SW is the switching node that supplies power to the output. Connect the output LC filter from SW to the output load. Note that a capacitor is required from SW to BST to power the high-side switch.
PGND	8, 9	Power Ground. Connect PGND plane and EXPOSED PAD with as many via for thermal and efficiency performance.
EN	10	Enable Input. EN is a digital input that turns the regulator on or off. Drive EN high to turn on the regulator and low to turn it off. Connect directly to VIN for automatic startup.
FS	11	This pin sets the oscillator switching frequency using a resistor, R_{FS}, from FS pin to GND. The frequency of operation can be programmed from 300kHz to 2.5MHz. Connect FS to VCC or HIGH for a default frequency of 500kHz.
MSYNC	12	Connect MSYNC to VCC or HIGH for forced PWM. Connect MSYNC to GND for PFM operation. Apply an external clock source for synchronization with positive edge trigger and PWM.
PG	13	Open drain power-good output that is pulled to GND when the output voltage is out of its regulation limits or during soft-start interval. There is an internal 5MΩ pullup resistor.
SS/TR	14	The SS/TR pin controls the soft-start and sequence of the output. A single capacitor from SS/TR to GND determines the output ramp rate. See the *Enable, Soft-Start, Tracking, Sequencing, and Disable* section for more application detail about soft-start, output tracking, and sequencing. If SS/TR is tied to VCC, then an internal soft-start of 1.7ms will be used. For CC mode applications, apply a reference voltage to the pin.
FB	15	Feedback Input. FB senses the output voltage and regulates it. Drive FB with a resistive divider connected to it from the output voltage to this pin. The feedback regulation voltage is 0.8V. See *Setting the Output Voltage*.
GND	16	Analog ground that is used for the controller. Single point connection to the EPAD.
Exposed Thermal Pad	—	Connect to ground plane for adequate heat sinking and noise reduction.

Absolute Maximum Ratings (Note 4)

Symbol	Parameter	Rating	Unit
V_{IN}	Supply Voltage	-0.3 to +70	V
V_{SWS}	Switch Node Static Voltage	-0.3 to V_{IN} + 0.3	V
V_{SWT}	Switch Node Transient Voltage	-2.5 to V_{IN} + 2	V
V_{EN}	Enable/UVLO Voltage	-0.3V to + 70	V
V_{BST}	Bootstrap Voltage	V_{SW} - 0.3 to V_{SW} + 6.0	V
V_{BIAS}	Bias Voltage	-0.3 to +18	V
V_{CC}	VCC Voltage	-0.3V to +6.0	V
V_{FB}	Feedback Voltage	-0.3V to +6.0	V
V_{FS}	Frequency Adjust	-0.3V to +6.0	V
V_{PG}	Power-Good Voltage	-0.3V to +6.0	V
$V_{SS/TR}$	Soft-Start/Tracking	-0.3V to +6.0	V
V_{MSYNC}	Synchronization and MODE	-0.3V to +6.0	V
T_{ST}	Storage Temperature	-65 to +150	°C
T_J	Junction Temperature	+150	°C
T_L	Lead Temperature	+300	°C
ESD Susceptibility (Note 5)			
HBM	Human Body Model	±2000	V
CDM	Charged Device Model	±1000	V

Notes: 4. Stresses greater than those listed under *Absolute Maximum Ratings* can cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to *Absolute Maximum Ratings* for extended periods can affect device reliability. For transient pulse duration, use 20ns at switch node.
5. Semiconductor devices are ESD sensitive and can be damaged by exposure to ESD events. Suitable ESD precautions should be taken when handling and transporting these devices.

Thermal Resistance

Package	Symbol	Parameter	JEDEC (Note 6)	Unit
U-QFN4040-16/SWP (Type UXB)	θ_{JA}	Junction to Ambient	32	°C/W
	θ_{JC}	Junction to Case	6	°C/W

Note: 6. Device mounted on FR-4 substrate, 1” sq. PC board, 2oz copper, with minimum recommended pad layout.

Recommended Operating Conditions (Note 7)

Symbol	Parameter	Min	Max	Unit
V_{IN}	Supply Voltage	3.8	60	V
V_{BIAS}	Bias Voltage	3.8	15	V
T_A	Operating Ambient Temperature Range	-40	+105	°C

Note: 7. The device function is not guaranteed outside of the recommended operating conditions.

Functional Block Diagram

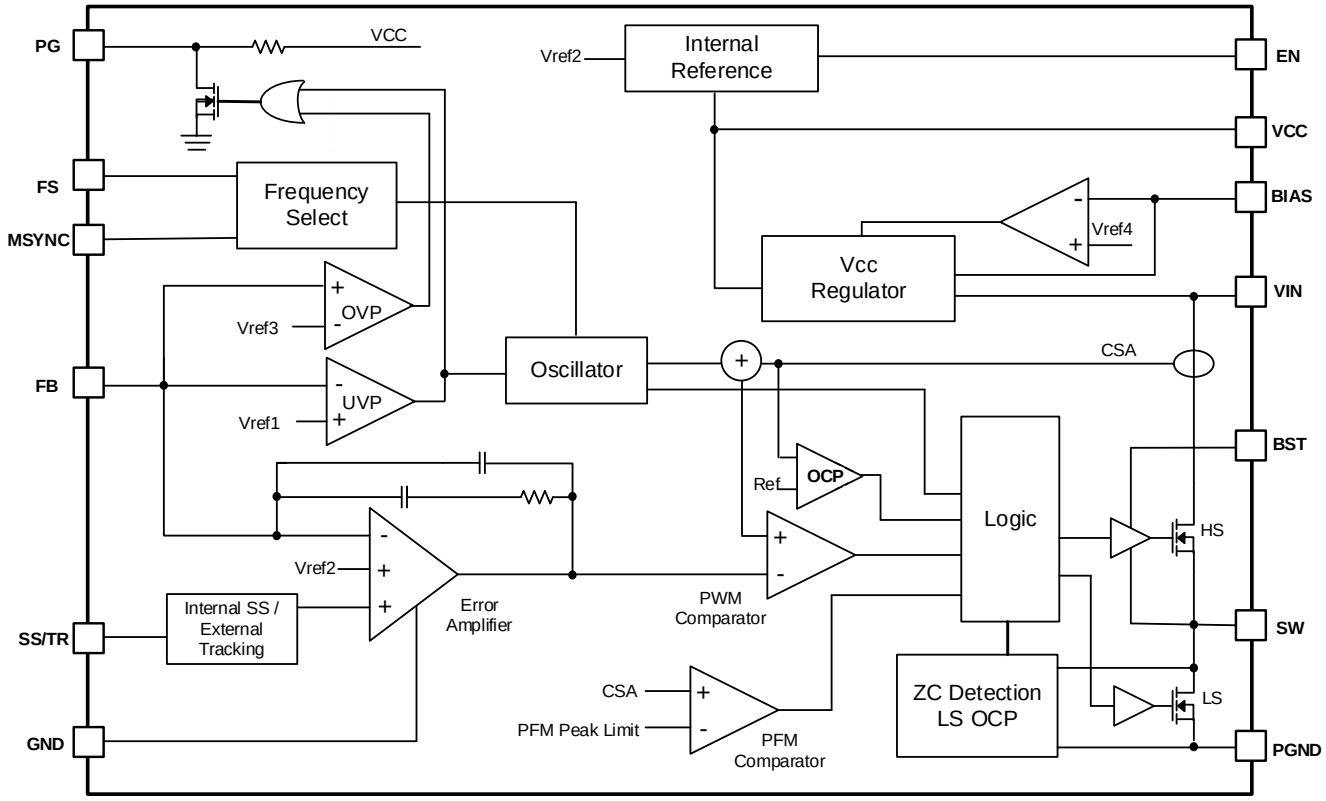


Figure 4. Functional Block Diagram

Electrical Characteristics (V_{IN} = 48V, V_{OUT} = 5V, f_{SW} = 500kHz, BOM = Table 1, unless otherwise specified. Min/Max limits apply across the recommended junction temperature range, -40°C to +105°C, unless otherwise specified.)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
UVLO	VCC Undervoltage Lockout Threshold	—	—	3.5	3.75	V
	Hysteresis	—	—	50	—	mV
I_{SHDN}	Shutdown Supply Current	V_{EN} = 0, V_{IN} = 60V	—	2.2	8	μA
I_Q	Supply Current (Quiescent)	V_{EN} = 2.0V, V_{FB} = 0.85V	—	43	75	μA
VCC	5V LDO Output	V_{IN} = 6V to 60V	4.4	4.8	5.3	V
I_{VCC}	VCC Output Current Limit	—	—	40	80	mA
V_{BIAS}	Rising Edge Bias Switchover Voltage	—	—	4.5	4.7	V
	Falling Edge Bias Switchover Voltage	—	4.05	4.25	—	V
$R_{DS(ON)1}$	High-Side Switch On-Resistance	—	—	120	210	mΩ
$R_{DS(ON)2}$	Low-Side Switch On-Resistance	—	—	55	95	mΩ
$R_{DISCHARGE}$	SW Soft Discharge On-Resistance	—	—	10	—	kΩ
I_{LIMIT}	HS Peak Current Limit (AL8890)	V_{IN} > 4.5V, Tested under Test Mode	4.3	4.8	5.3	A
		V_{IN} < 4.5V, Tested under Test Mode	—	3.2	—	A
I_{PFMPK}	PFM Peak Current Limit (AL8890)	Tested under Test Mode	—	1.35	1.6	A
I_{LIMIT}	HS Peak Current Limit (AL88902)	V_{IN} > 4.5V, Tested under Test Mode	3.4	3.8	4.2	A
		V_{IN} < 4.5V, Tested under Test Mode	—	3.2	—	A
I_{PFMPK}	PFM Peak Current Limit (AL88902)	Tested under Test Mode	—	1.0	1.2	A
I_{ZC}	Zero Cross Current Threshold	—	—	0	—	A
I_{LIMIT_NEG}	LS Valley Current Limit	—	-3.3	-2.5	-1.7	A
Hiccup Time	Time Delay Cycle Before Next Soft-Start	—	—	8	—	t_{SS}
I_{SW_LKG}	Switch Leakage Current	V_{EN} = 0, V_{SW} = 0, V_{IN} = 60V	—	—	1	μA
f_{SW}	Oscillator Frequency	FS = VCC, Default	440	500	560	kHz
		R_{FS} = 845kΩ	240	300	360	
		R_{FS} = 57.6kΩ	2200	2500	2800	
MSYNC	Synchronization Range	—	300	—	2500	
V_{MSYNC_RISING}	MSYNC Rising Threshold	—	1.4	—	—	V
$V_{MSYNC\_FALLING}$	MSYNC Falling Threshold	—	—	—	0.8	V
MSYNC PW	MSYNC Pulse Width	—	—	250	—	ns
t_{ON}	Minimum On-Time	—	—	115	—	ns
t_{OFF}	Minimum Off-Time	V_{FB} = 760mV	—	125	—	ns
V_{FB}	Feedback Voltage	V_{IN} = 3.8V to 60V	788	800	808	mV
		SS/TR = 0.1V	—	100	—	mV
t_{SS}	Soft-Start Period	SS/TR = VCC	—	1.7	—	ms
I_{SS}	Soft-Start Charging Current	SS/TR = 0	0.75	1.00	1.25	μA
PG_{UV_FALL}	Undervoltage Falling Threshold	Percent of Output Regulation, Fault	87	90	93	%
PG_{UV_RISE}	Undervoltage Rising Threshold	Percent of Output Regulation, Good	92	95	99	%
PG_{OV_RISE}	Overvoltage Rising Threshold	Percent of Output Regulation, Fault	107	110	114	%
PG_{OV_FALL}	Overvoltage Falling Threshold	Percent of Output Regulation, Good	102	105	108	%
PG Pullup	PG Pullup Resistor	—	—	5	—	MΩ

Electrical Characteristics (V_{IN} = 48V, V_{OUT} = 5V, f_{SW} = 500kHz, BOM = Table 1, unless otherwise specified. Min/Max limits apply across the recommended junction temperature range, -40°C to +105°C, unless otherwise specified.) (continued)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
PG Low	PG Low Voltage	I_{PG} = -3mA	—	100	300	mV
PG Delay	PG Rising Edge Delay	—	—	1.5	—	ms
	PG Falling Edge Delay	—	—	2	—	μs
V_{EN_TH}	EN Rising Threshold	—	1.38	1.45	1.52	V
	Hysteresis	—	—	100	—	mV
R_{EN}	EN Input Resistance	—	—	40	—	MΩ
T_{SHDN}	Thermal Shutdown (Note 8)	—	—	+165	—	°C
T_{HYS}	Thermal Hysteresis (Note 8)	—	—	+20	—	°C

Note: 8. Compliance to the datasheet limits is assured by one or more methods: production test, characterization, and/or design.

Typical Performance Characteristics (T_A = +25°C, VIN = 12V, VOUT = 5V, f_{SW} = 400kHz, BOM = Table 1, unless otherwise specified.)

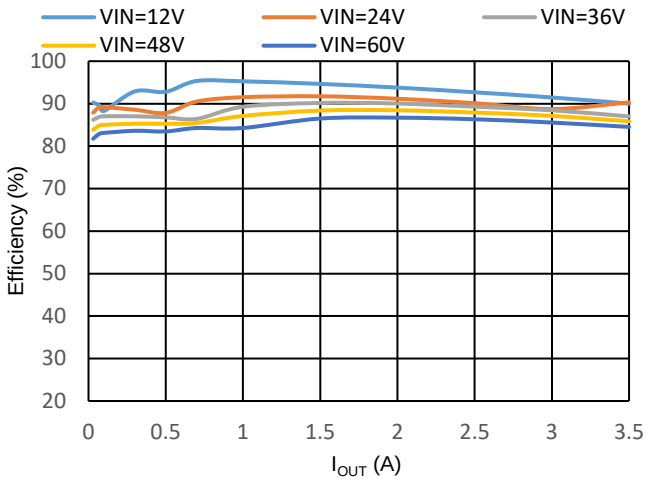


Figure 5. PFM Efficiency vs. Output Current

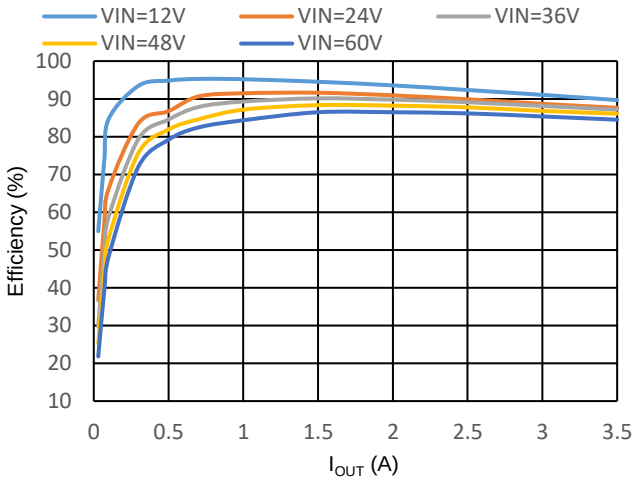


Figure 6. PWM Efficiency vs. Output Current

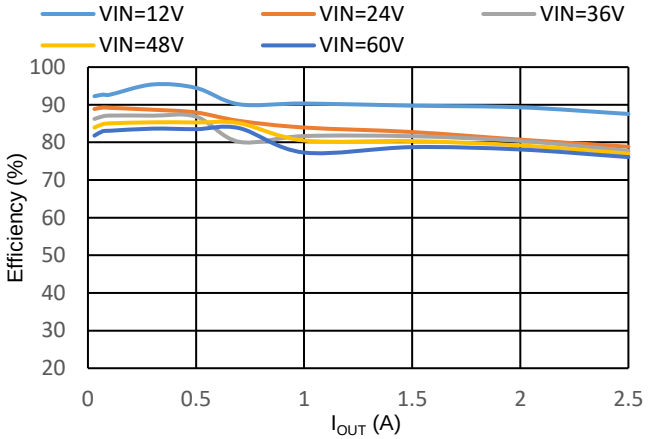


Figure 7. PFM Efficiency vs. Output Current, f_{SW} = 2.2MHZ

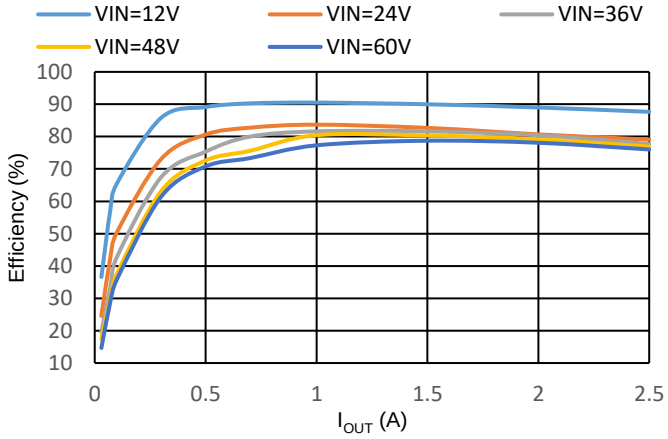


Figure 8. PWM Efficiency vs. Output Current, f_{SW} = 2.2MHZ

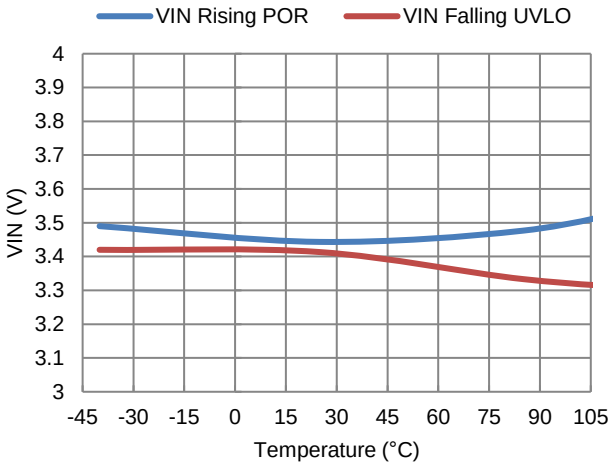


Figure 9. VIN POR and UVLO vs. Temperature

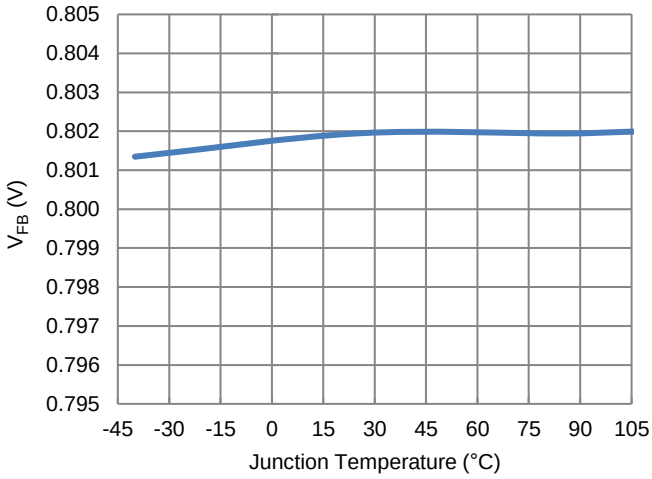


Figure 10. Feedback Voltage V_{FB} vs. Junction Temperature

Typical Performance Characteristics (T_A = +25°C, VIN = 12V, VOUT = 5V, f_{SW} = 400kHz, BOM = Table 1, unless otherwise specified.) (continued)

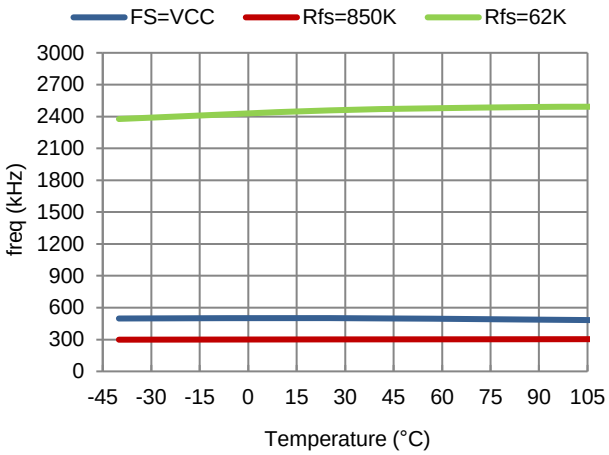


Figure 11. Frequency vs. Temperature

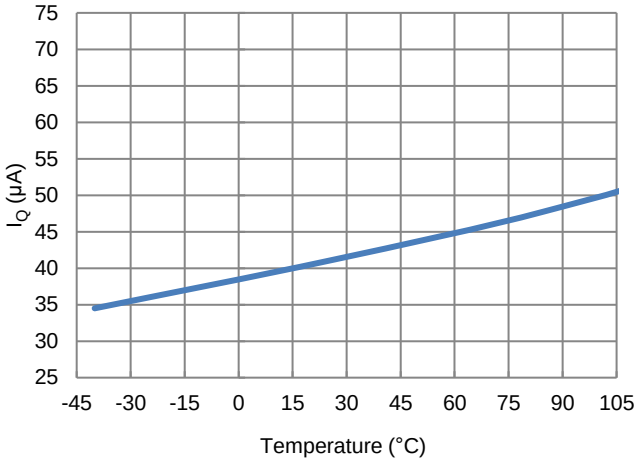


Figure 12. I_Q vs. Temperature, I_{OUT} = 0

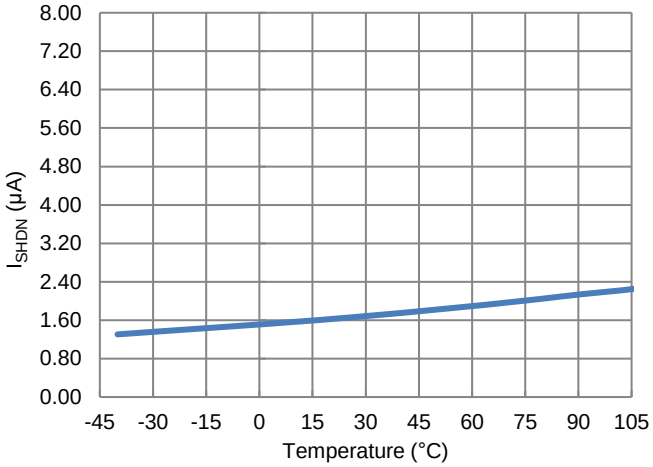


Figure 13. I_{SHDN} vs. Temperature

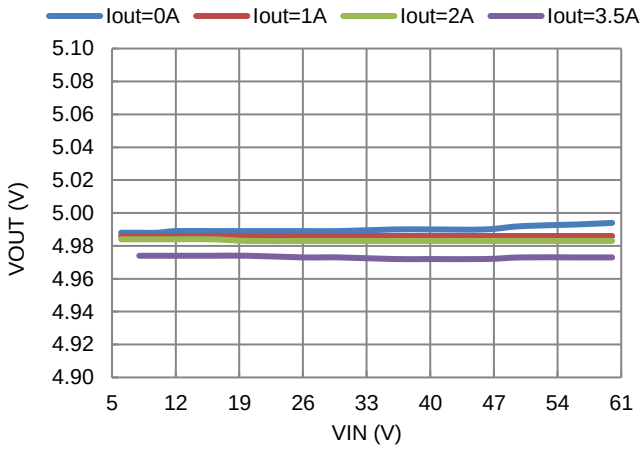


Figure 14. PWM Line Regulation

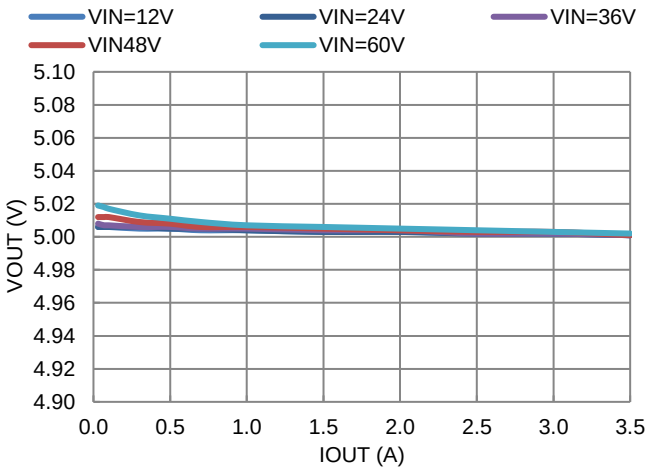


Figure 15. PWM Load Regulation

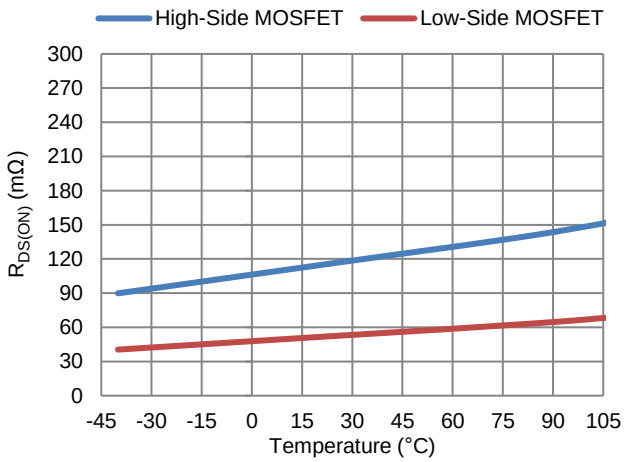


Figure 16. Power MOSFET $R_{DS(ON)}$ vs. Temperature

Typical Performance Characteristics (T_A = +25°C, VIN = 12V, VOUT = 5V, f_{SW} = 400kHz, BOM = Table 1, unless otherwise specified.) (continued)

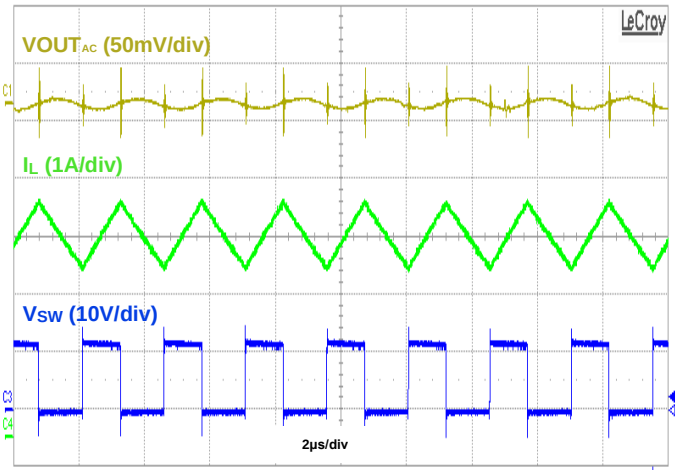


Figure 17. Output Ripple, VIN = 12V, VOUT = 5V @3.5A, PFM

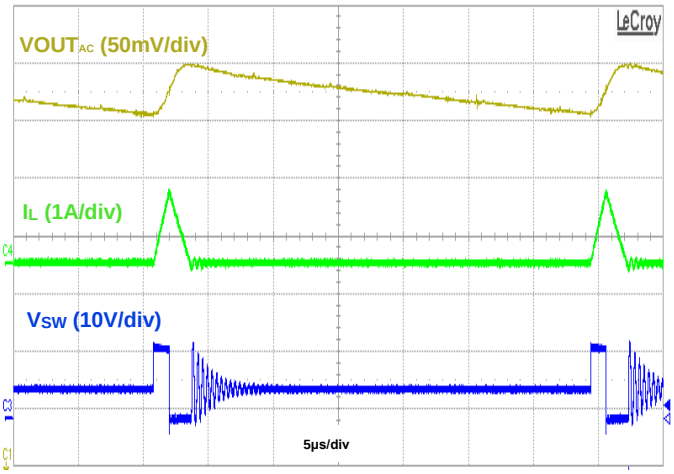


Figure 18. Output Ripple, VIN = 12V, VOUT = 5V @50mA, PFM

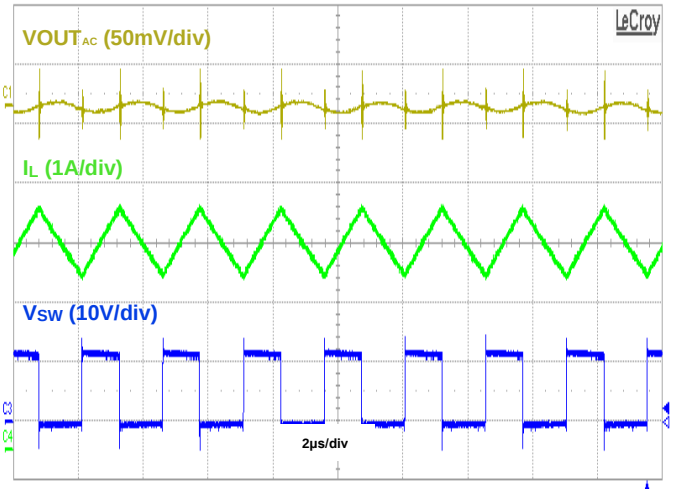


Figure 19. Output Ripple, VIN = 12V, VOUT = 5V @3.5A, PWM

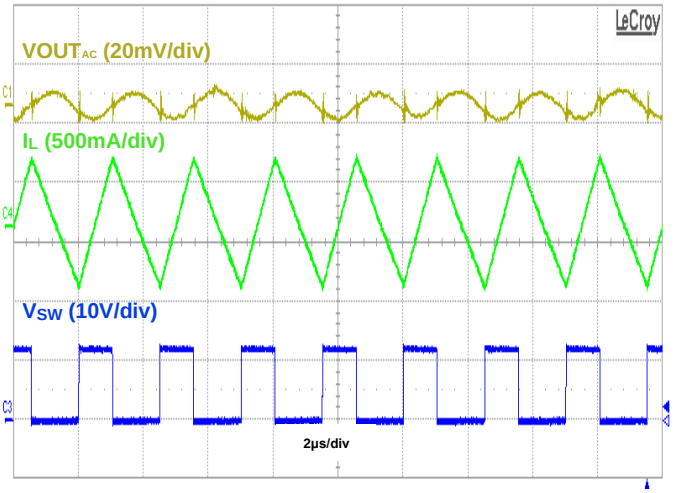


Figure 20. Output Ripple, VIN = 12V, VOUT = 5V @50mA, PWM

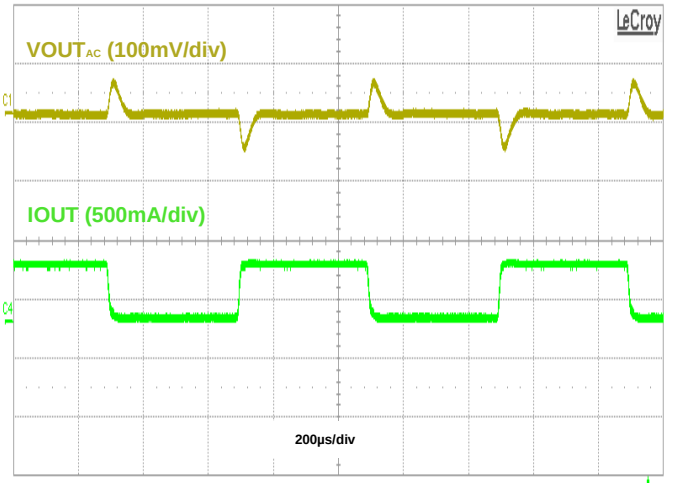


Figure 21. Load Transient, IOUT = 50mA to 500mA to 50mA, PWM

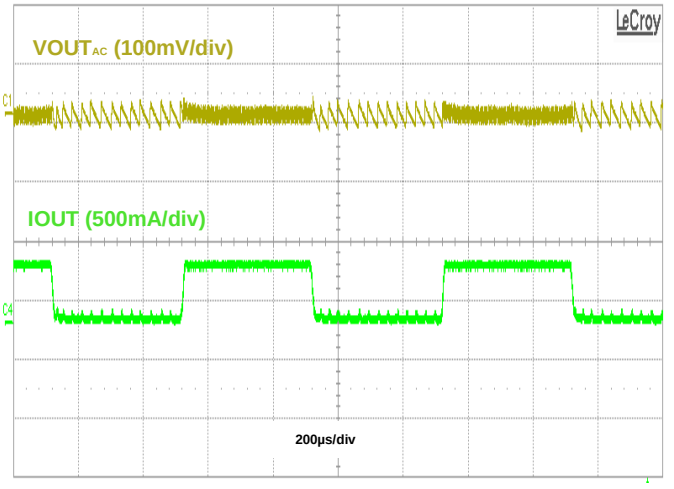


Figure 22. Load Transient, IOUT = 50mA to 500mA to 50mA, PFM

Typical Performance Characteristics (T_A = +25°C, VIN = 12V, VOUT = 5V, f_{SW} = 400kHz, BOM = Table 1, unless otherwise specified.) (continued)

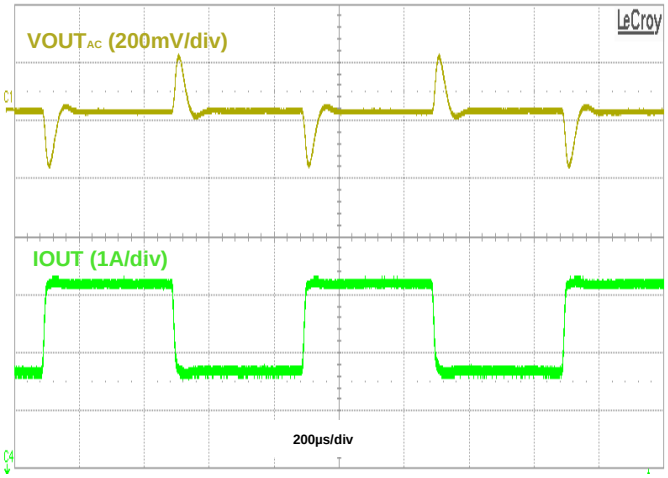


Figure 23. Load Transient, IOUT = 2A to 3.5A to 2A, PWM

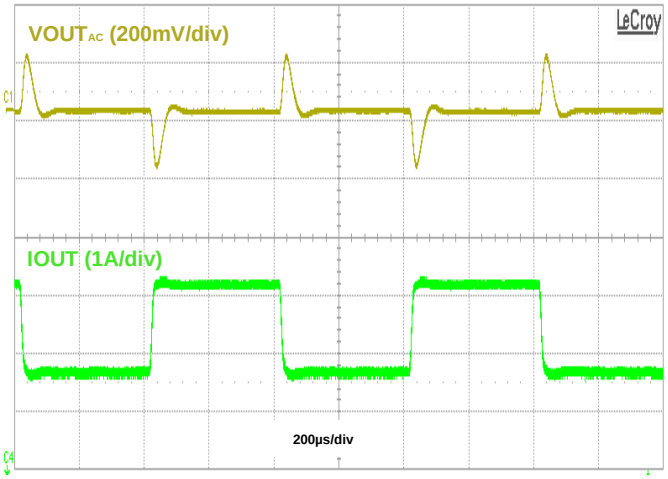


Figure 24. Load Transient, IOUT = 2A to 3.5A to 2A, PFM

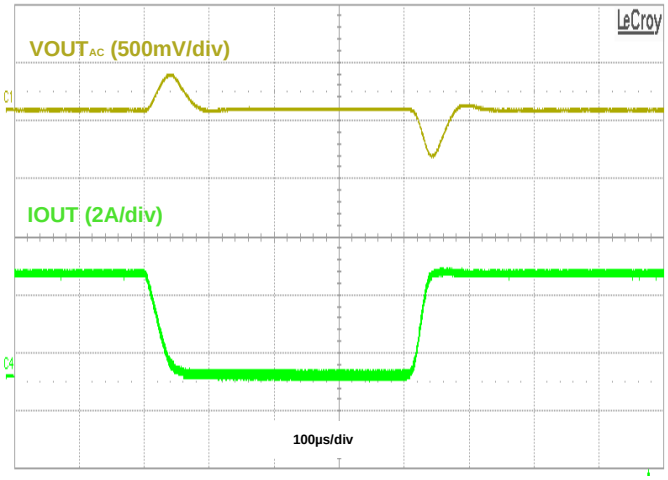


Figure 25. Load Transient, IOUT = 50mA to 3.5A to 50mA, PWM

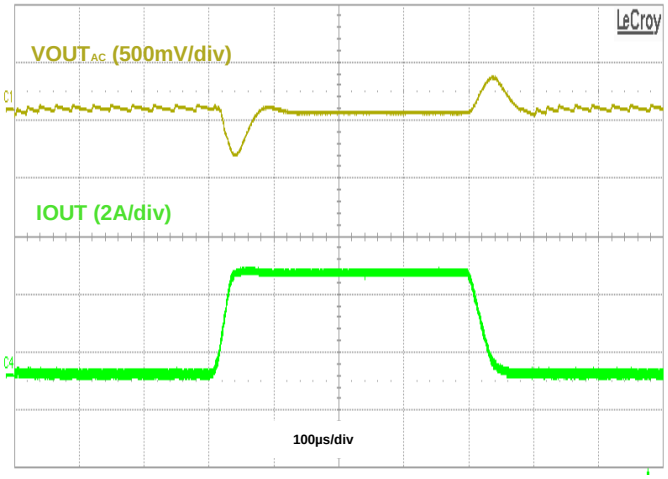


Figure 26. Load Transient, IOUT = 50mA to 3.5A to 50mA, PFM

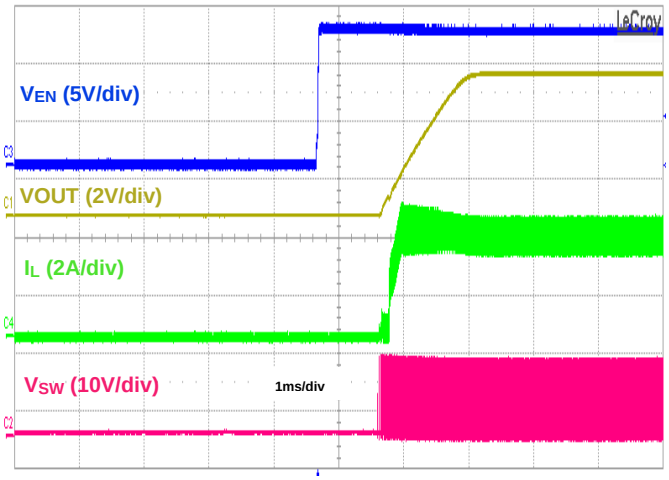


Figure 27. Startup Using EN, IOUT = 3.5A

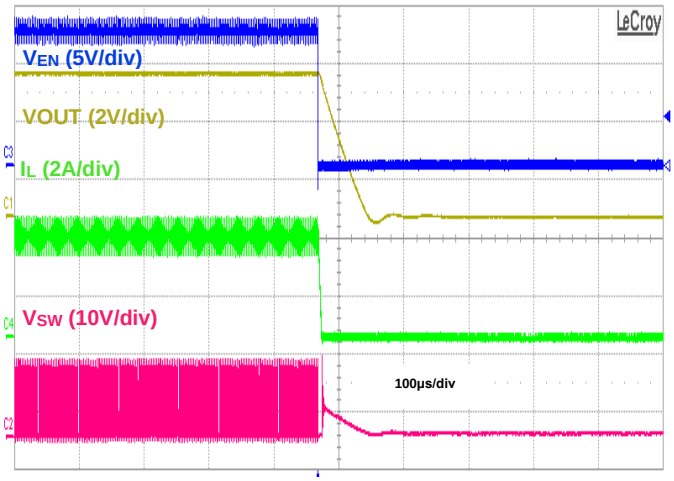


Figure 28. Shutdown Using EN, IOUT = 3.5A

Typical Performance Characteristics (T_A = +25°C, VIN = 12V, VOUT = 5V, f_{SW} = 400kHz, BOM = Table 1, unless otherwise specified.) (continued)

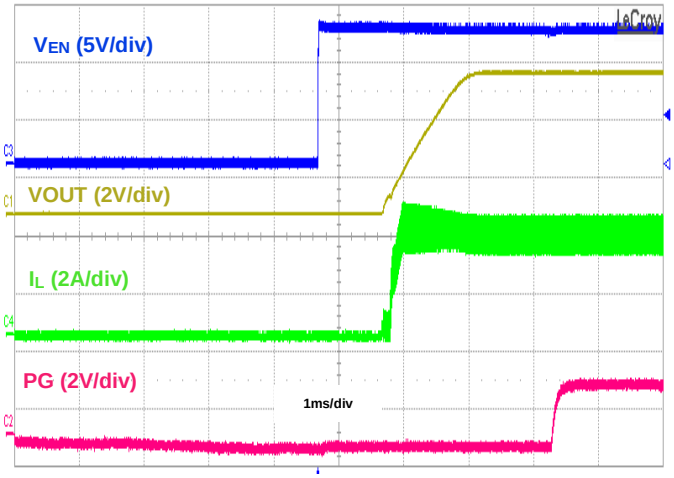


Figure 29. Startup Using EN with PG, IOUT = 3.5A

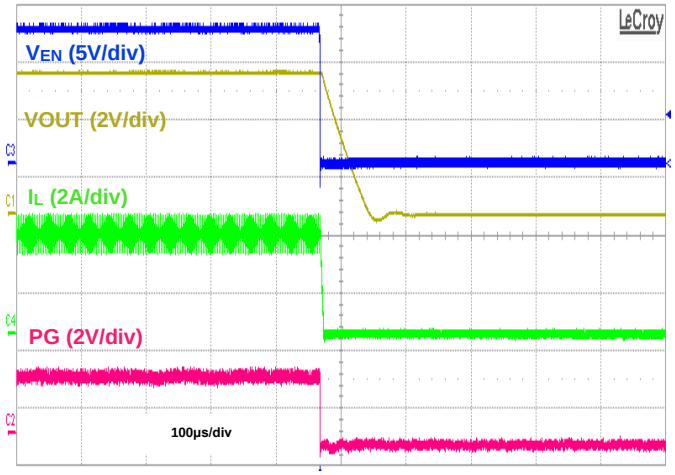


Figure 30. Shutdown Using EN with PG, IOUT = 3.5A

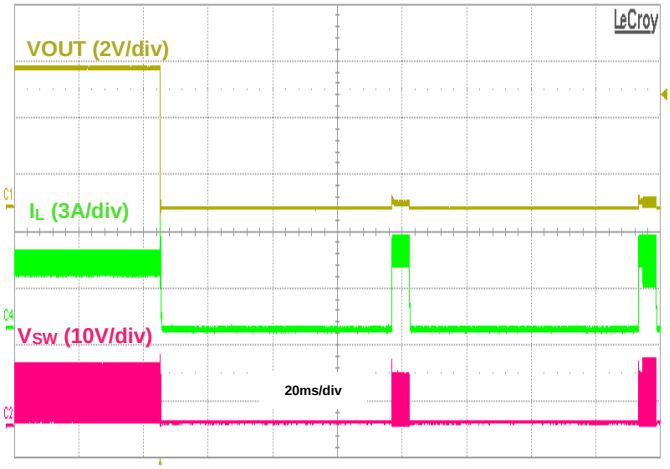


Figure 31. Output Short Protection, IOUT = 3.5A

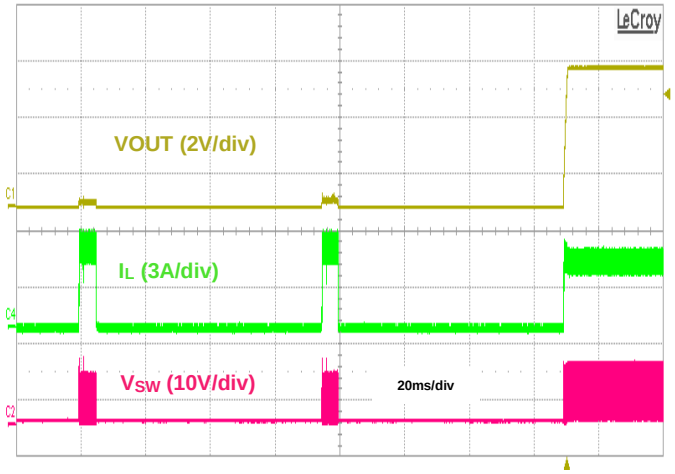


Figure 32. Output Short Recovery, IOUT = 3.5A

Typical Performance Characteristics (T_A = +25°C, VIN = 12V, VOUT = 5V, f_{SW} = 2.2MHz, BOM = Table 1, unless otherwise specified.)

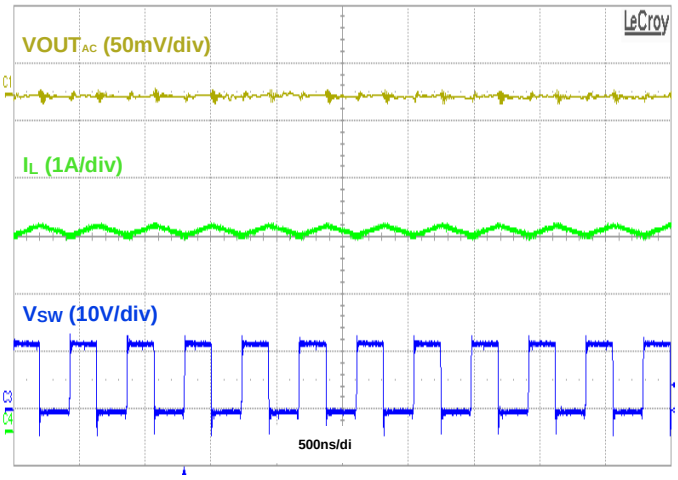


Figure 33. Output Ripple, VIN = 12V, VOUT = 5V @3.5A, PFM

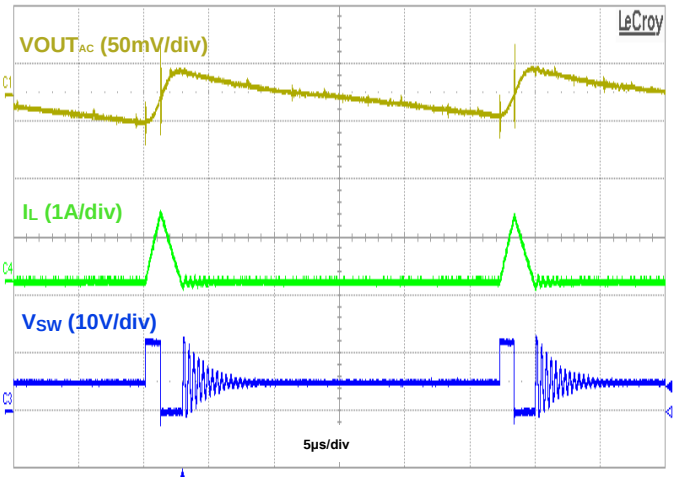


Figure 34. Output Ripple, VIN = 12V, VOUT = 5V @50mA, PFM

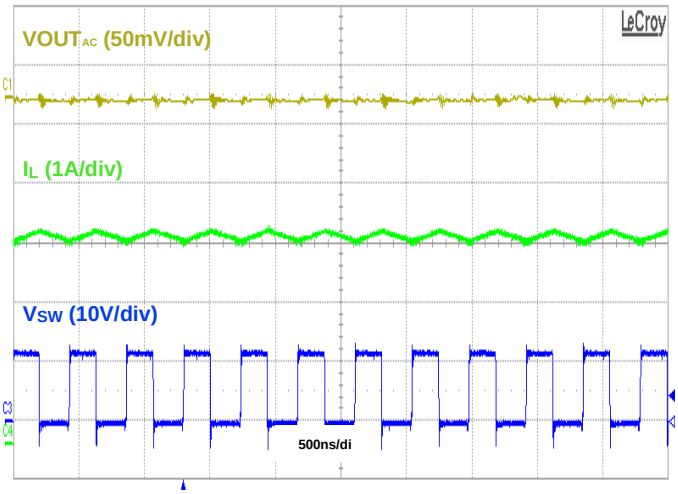


Figure 35. Output Ripple, VIN = 12V, VOUT = 5V @3.5A, PWM

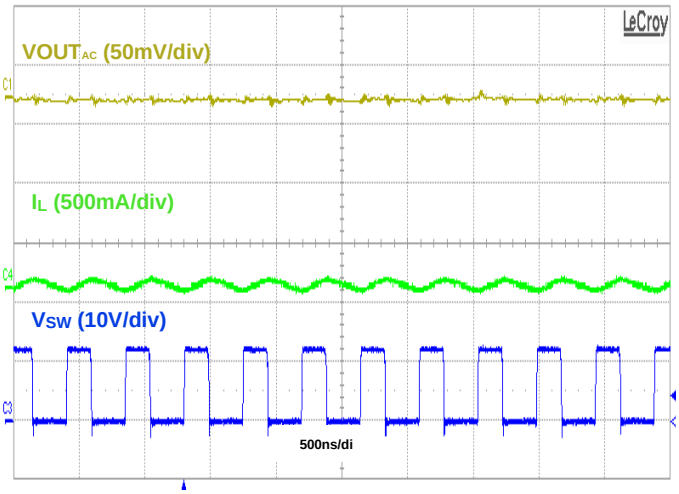


Figure 36. Output Ripple, VIN = 12V, VOUT = 5V @50mA, PWM

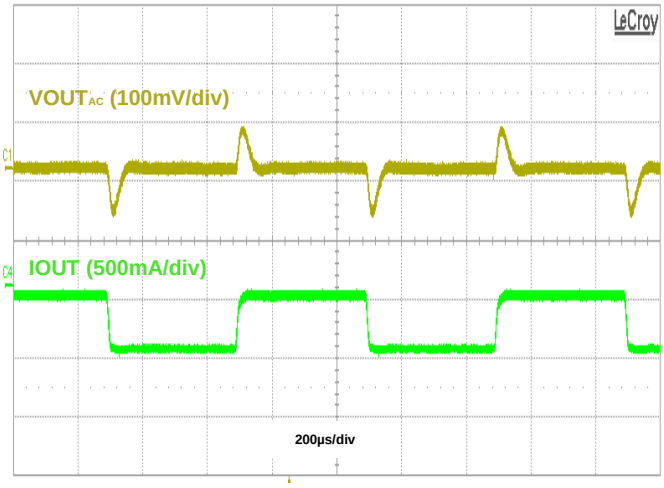


Figure 37. Load Transient, IOUT = 50mA to 500mA to 50mA, PWM

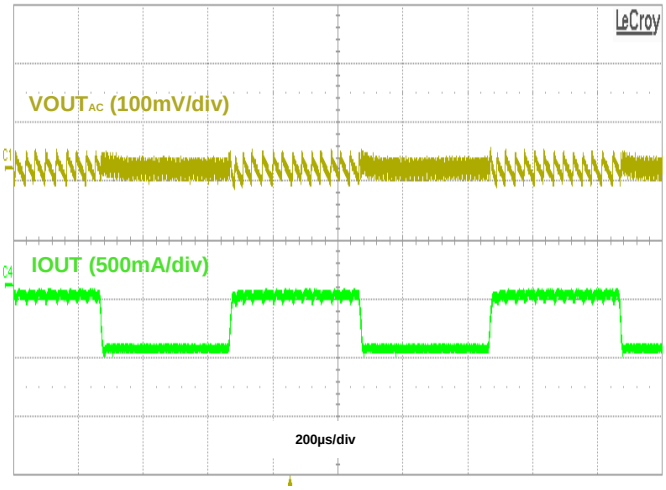


Figure 38. Load Transient, IOUT = 50mA to 500mA to 50mA, PFM

Typical Performance Characteristics (T_A = +25°C, VIN = 12V, VOUT = 5V, f_{SW} = 2.2MHz, BOM = Table 1, unless otherwise specified.) (continued)

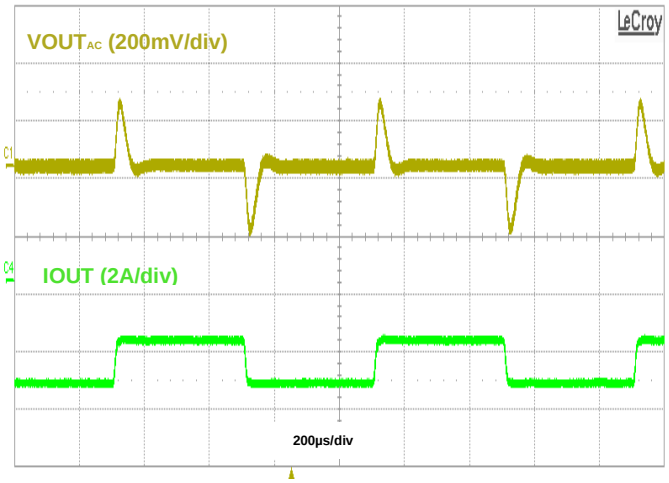


Figure 39. Load Transient, IOUT = 2A to 3.5A to 2A, PWM

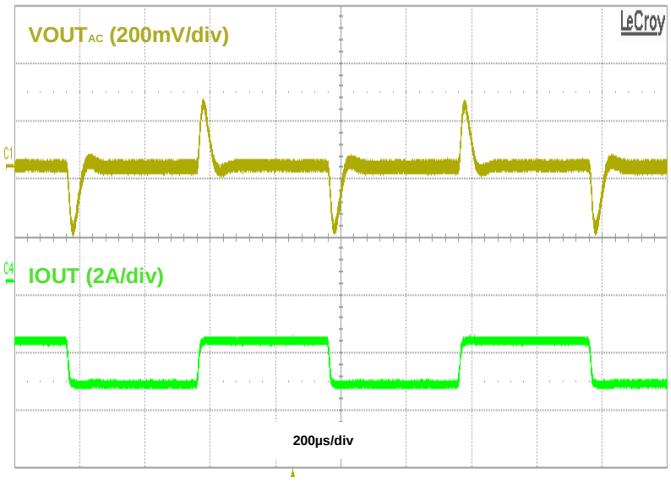


Figure 40. Load Transient, IOUT = 2A to 3.5A to 2A, PFM

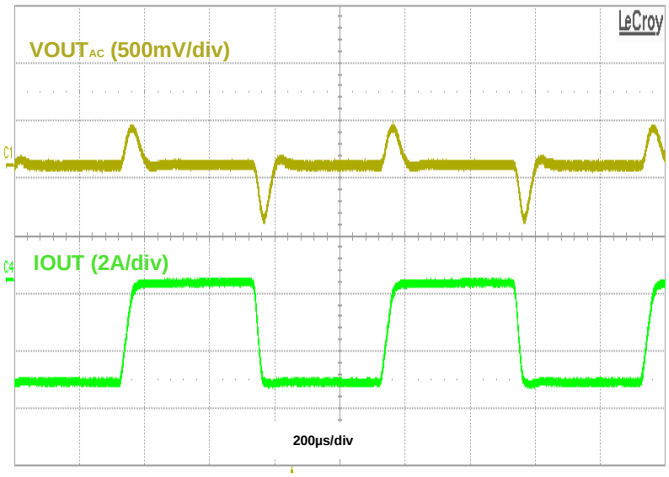


Figure 41. Load Transient, IOUT = 50mA to 3.5A to 50mA, PWM

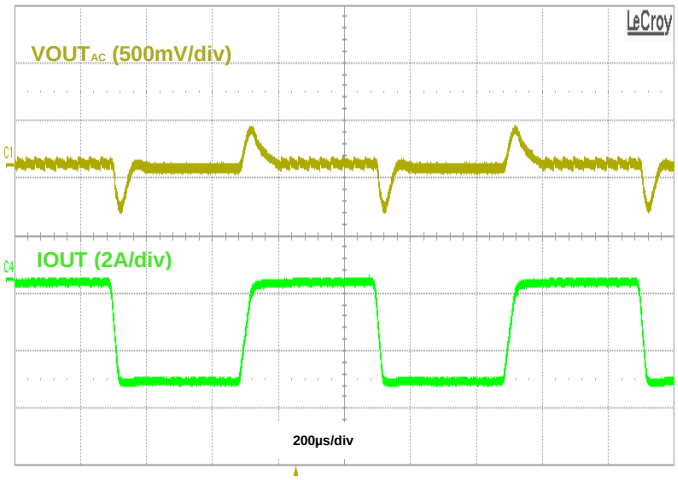


Figure 42. Load Transient, IOUT = 50mA to 3.5A to 50mA, PFM

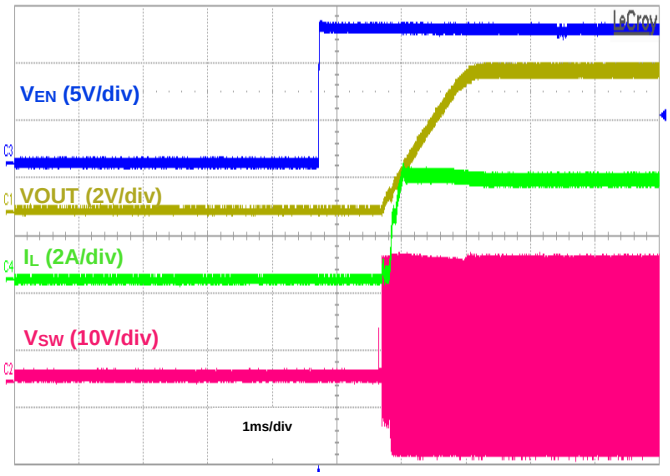


Figure 43. Startup Using EN, IOUT = 3.5A

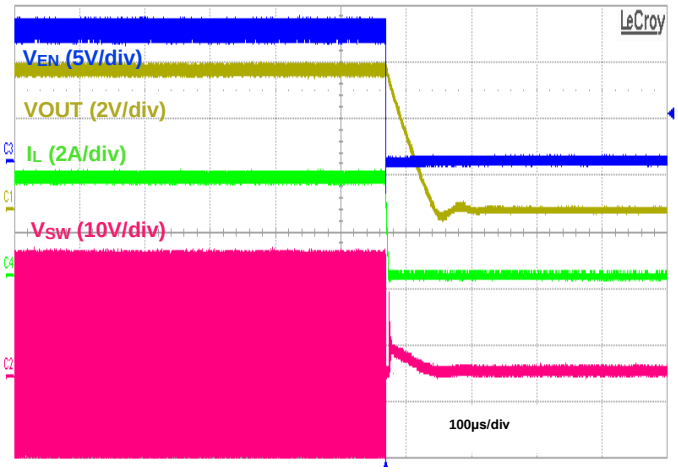


Figure 44. Shutdown Using EN, IOUT = 3.5A

Typical Performance Characteristics (T_A = +25°C, VIN = 12V, VOUT = 5V, f_{SW} = 2.2MHz, BOM = Table 1, unless otherwise specified.) (continued)

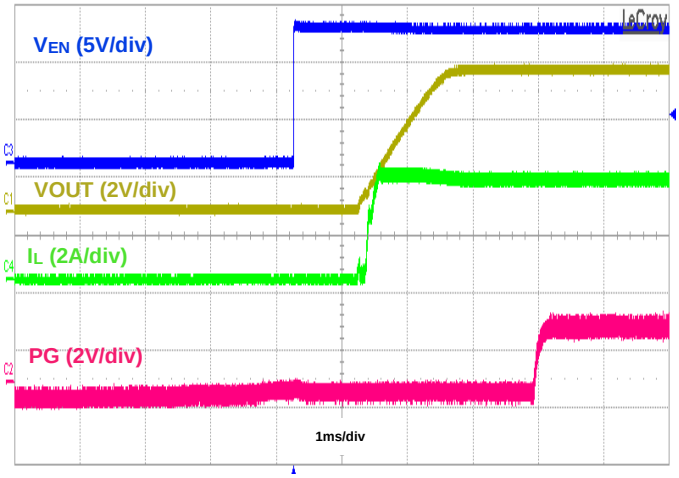


Figure 45. Startup Using EN with PG, IOUT = 3.5A

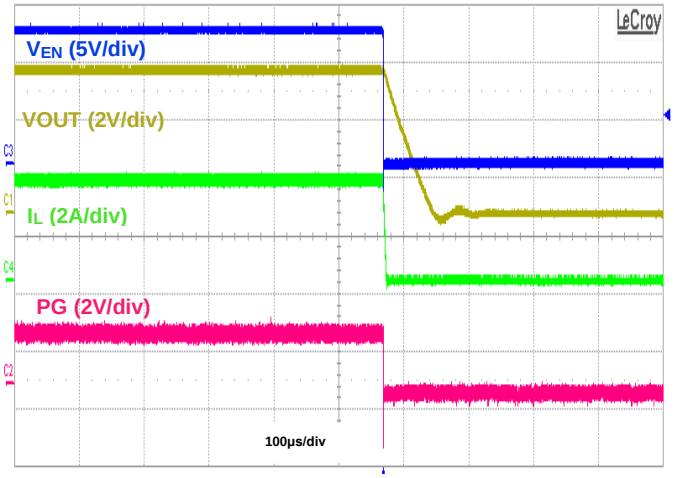


Figure 46. Shutdown Using EN with PG, IOUT = 3.5A

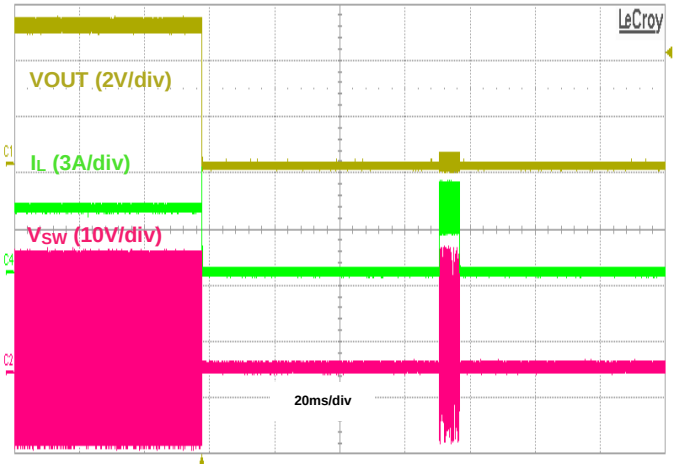


Figure 47. Output Short Protection, IOUT = 3.5A

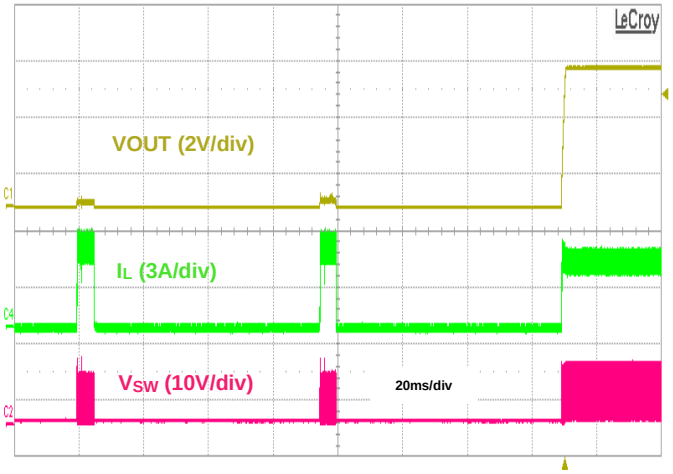


Figure 48. Output Short Recovery, IOUT = 3.5A

Functional Description

Setting the Output Voltage

The output voltage can be adjusted from 0.8V using an external resistor divider. Table 1 shows a list of resistor selection for common output voltages. An optional C4 of 10pF to 470pF can be used to boost the phase margin and improve stability as well as the transient performance. R2 in Figure 49 can be determined by the following equation:

$$R_2 = \frac{R_1 \cdot 0.8}{Vout - 0.8}$$

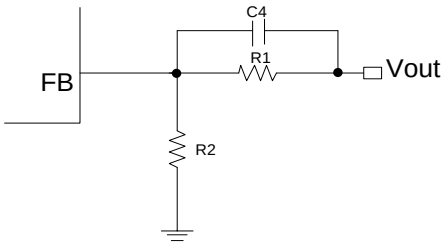


Figure 49. Feedback Divider Network

V_{OUT} (V)	R1 (kΩ)	R2 (kΩ)	C4 (pF)	L1 (μH)	C2 (μF)	f_{SW} (kHz)
1.2	100	200	47	3.3	2 x 22	500
2.5	100	47.06	47	3.3	2 x 22	500
3.3	100	31.60	47	5.5	2 x 22	500
5	100	19.10	47	6.5	2 x 22	500
12	100	7.14	47	15	2 x 22	500
24	100	3.45	47	20	2 x 22	500

Table 1. Recommended Component Selection

Operating Frequency

The AL8890/AL88902 operates at a default 500kHz switching frequency when FS is connected to VCC. Using a resistor from FS to GND programs the frequency from 300kHz to 2.5MHz. A minimum on-time of 115ns typical in conjunction with the input and output voltage should be considered when selecting the maximum operating frequency. Use the equation below to set the desired switching frequency:

$$R_{FS}[k\Omega] = \frac{267}{FS[MHz]} - 50$$

Alternatively, the frequency of operation can be synchronized from 300kHz to 2.5MHz with an external signal applied to the MSYNC pin. It is recommended to use a MSYNC pulse width of at least 250ns.

Theory of Operation

The AL8890/AL88902 is a 3.5A/2.5A current-mode control, synchronous buck regulator with integrated power MOSFETs. Current-mode control assures excellent line regulation, load regulation, and a wide loop bandwidth for fast response to load transients. Figure 1 and Figure 4 depicts the typical application schematic and functional block diagram of the AL8890/AL88902. The buck controller drives the internal nFETs. The buck regulator can operate from an unregulated DC source, such as a battery, with a voltage ranging from 3.8V to 60V. The converter output can be regulated as low as 0.8V to as high as 50V.

The feedback loop is compensated internally. See *Loop Compensation Design* for more details.

Internal VCC Regulator

An internal low dropout regulator produces the 4.8V supply from V_{IN} that powers the drivers and the internal bias circuity. The VCC can supply enough current for the AL8890/AL88902's circuitry and must be bypassed to PGND with a minimum of 1μF ceramic capacitor. Good bypassing is necessary to supply the high transient currents required by the power MOSFET gate drivers. To improve efficiency, the internal 5V regulator can also draw current from the BIAS pin when its voltage is at 4.5V or higher. If BIAS is connected to an external supply far away, be sure to bypass with a local ceramic capacitor. If the BIAS pin voltage is below 4.25V, the internal 5V regulator will source current from V_{IN}. Application with high input voltage or high switching frequency where the internal 4.8V regulator pulls current from V_{IN} will increase the die temperature.

Functional Description (continued)

Enable, Soft-Start, Tracking, Sequencing, and Disable

The enable (EN) input allows the user to control turning on or off the regulator. Once the voltage on the EN pin is above its threshold, the buck controller powers up and soft-start begins.

The regulator does not allow the regulator to sink current during the soft-start period. The default time is 1.7ms if SS/TR pin is tied to VCC. The soft-start time can be extended by connecting an external capacitor between SS/TR and GND. The capacitor along with an internal I_{SS} of 1µA, sets the soft-start interval of the converter, t_{SS}, according to equation below:

C_{SS} (nF) = 1.25*t_{SS} (ms)

Ratiometric tracking is achieved in Figure 50 by using the same value for the soft-start capacitor on each power rail.

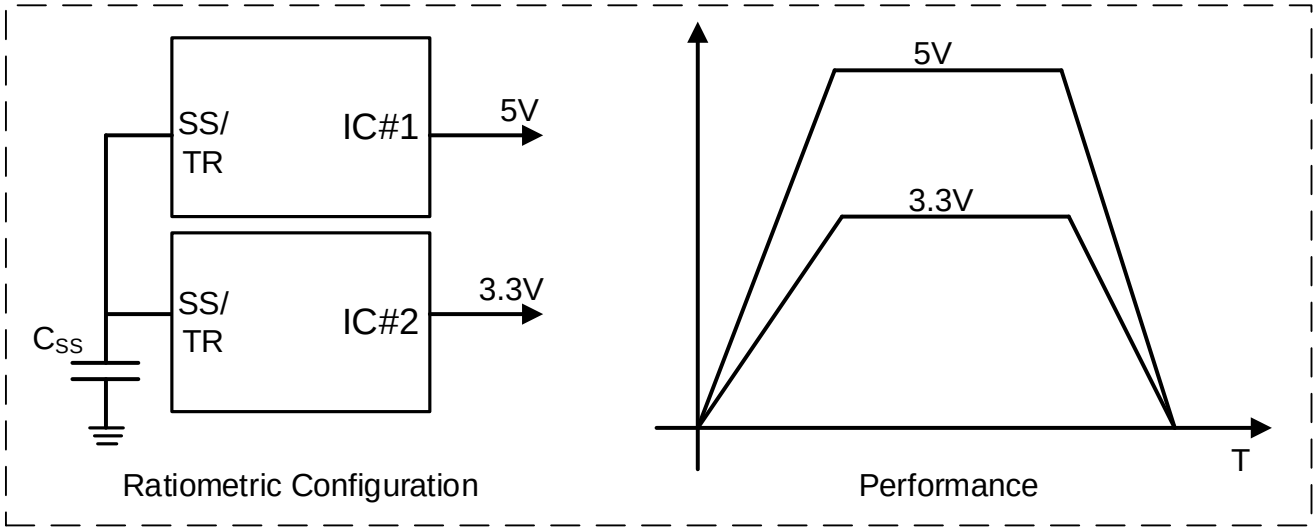


Figure 50. Ratiometic Configuration

Functional Description (continued)

By connecting a feedback network from the higher output voltage as shown in the Figure 51 below, coincidental track is implemented. The ratio of R3 and R4 should match with the ratio of feedback resistor divider of IC#2.

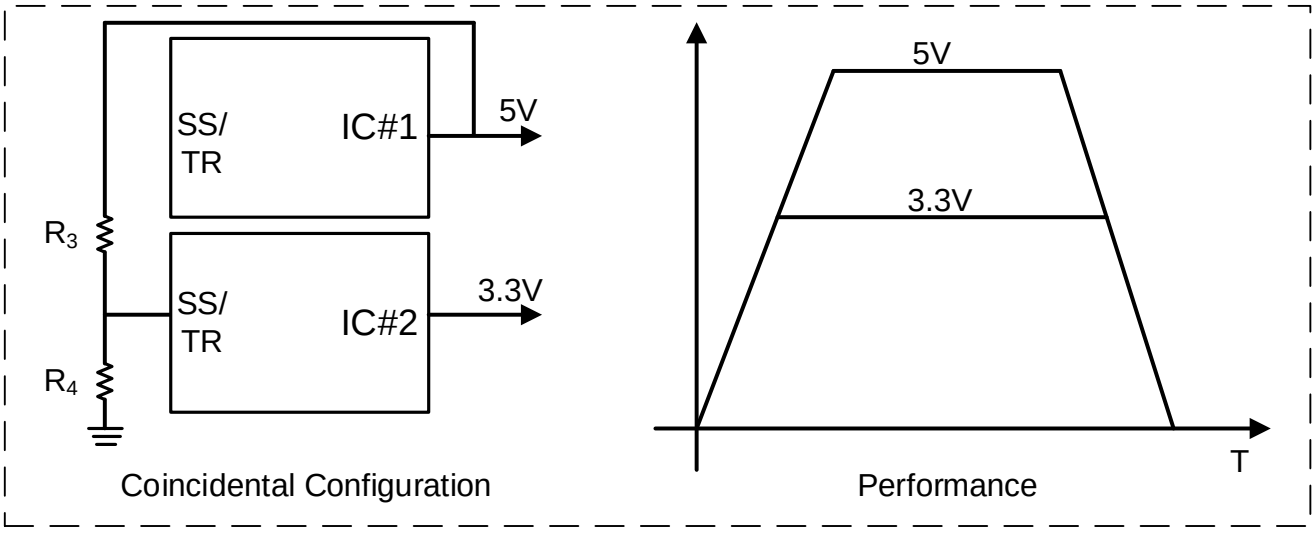


Figure 51. Coincidental Configuration

Figure 52 illustrates output sequencing.

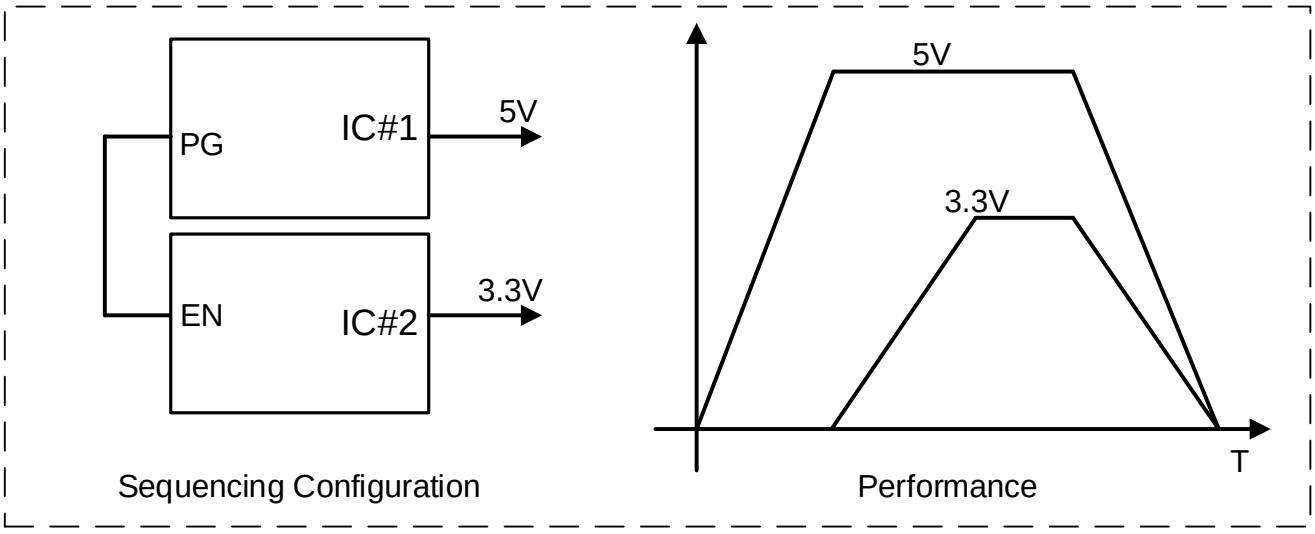


Figure 52. Sequencing Configuration

Functional Description (continued)

Output Active Discharge

The AL8890/AL88902 provides an internal 10kΩ resistor for output active discharge function. The internal resistor discharges the energy stored in the output capacitor to PGND whenever the regulator is disabled. When the regulator remains enabled, the internal resistor is disconnected from the output.

Current-Limit Protection

In order to reduce the total power dissipation and to protect the application, the AL8890/AL88902 has cycle-by-cycle current limiting implementation. The voltage drop across the internal high-side MOSFET is sensed and compared with the internally set current-limit threshold. This voltage drop is sensed at about 50ns after the HS turns on. When the peak inductor current exceeds the set current-limit threshold, current-limit protection is activated. When the current limit happens for 17 clock cycles within a 32-cycle time frame, the device enters Hiccup mode in which the controller periodically restarts the part. This protection mode greatly reduces the power dissipated on chip and reduces the thermal stress to help protect the device. The AL8890/AL88902 will exit Hiccup mode when the overcurrent situation is resolved.

Undervoltage Lockout (UVLO)

Undervoltage lockout is implemented to prevent the IC from insufficient input voltages. The AL8890/AL88902 has a UVLO comparator that monitors the VCC voltage and the internal bandgap reference. If the VCC voltage falls below 3.45V, the AL8890/AL88902 is disabled. Both HS and LS MOSFETs are off. Alternatively, the UVLO level can be adjusted by using EN pin with a resistive divider connected from VIN to GND. Connect the center node of the divider to EN. Choose R3 to be approximately 500kΩ, and the R4 is calculated using the equation below with a desired V_{UVLO} threshold.

$$R_4 = \frac{R_3 \cdot 1.45}{V_{UVLO} - 1.45}$$

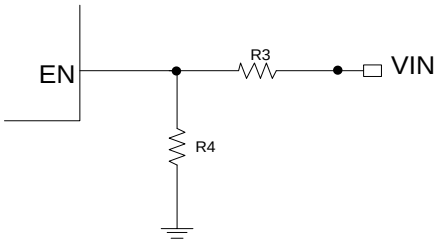


Figure 53. Setting the Input UVLO

Thermal Shutdown

If the junction temperature of the device reaches the thermal shutdown limit of +165°C, the AL8890/AL88902 shuts down both its high-side and low-side power MOSFETs. When the junction temperature reduces to the required level (+145°C typical), the device initiates a normal power-up cycle with soft-start.

Power Derating Characteristics

To prevent the regulator from exceeding the maximum recommended operating junction temperature, some thermal analysis is required. The regulator's temperature rise is given by:

$$\mathbf{T_{RISE} = PD \cdot (\theta_{JA})}$$

Where:

- PD is the power dissipated by the regulator
- θ_{JA} is the thermal resistance from the junction of the die to the ambient temperature

The junction temperature, T_J, is given by:

$$\mathbf{T_J = T_A + T_{RISE}}$$

Where:

- T_A is the ambient temperature of the environment

Functional Description (continued)

For the U-QFN4040-16/SWP (Type UXB) package, the θ_{JA} is 30°C/W. The actual junction temperature should not exceed the maximum recommended operating junction temperature of +150°C when considering the thermal design. Figure 54 shows a typical derating curve versus ambient temperature.

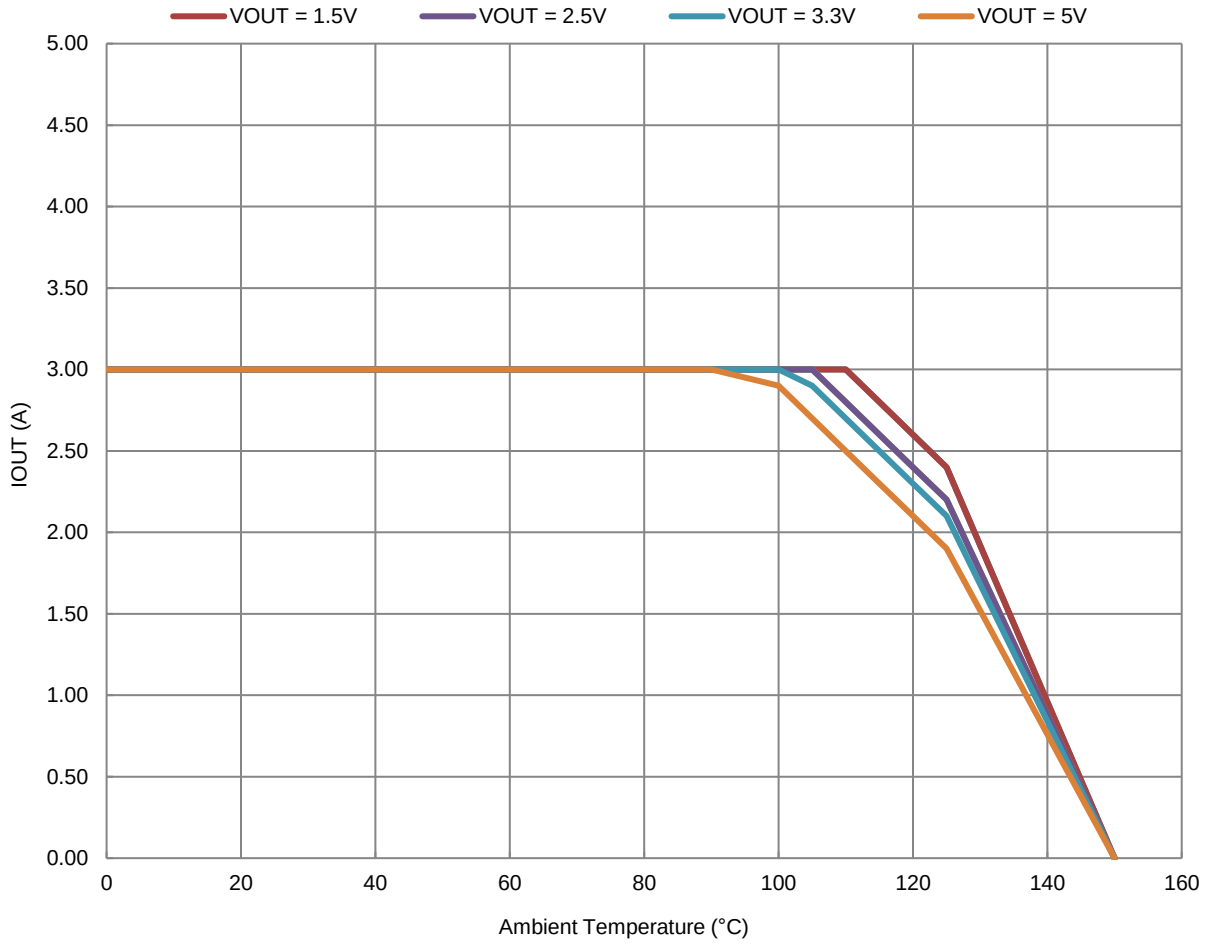


Figure 54. Output Current Derating Curve vs. Ambient Temperature, VIN = 12V

Power-Good

PG is the open-drain output of a window comparator that continuously monitors the buck regulator's output voltage via the FB pin. PG is actively held low when EN is low and during the soft-start period. After the soft-start period terminates, PG becomes high impedance as long as the output voltage is within ±5% of its regulation. Any fault condition forces PG low. There is an internal 5MΩ pullup resistor.

Startup with Pre-Biased Output

If V_{OUT} has been pre-biased to a certain voltage before power-up, V_{OUT} will remain at that pre-set voltage until the soft-start voltage catches up with V_{FB}. Therefore, the soft-start waveform is smooth without the excessive negative inductor current.

Functional Description (continued)

CCM Control Scheme

The regulator employs a current-mode pulse-width modulation control scheme for fast transient response and pulse-by-pulse current limiting. The current loop consists of the oscillator, the PWM comparator, current sensing circuit, and a slope compensation circuit. The gain of the current sensing circuit is typically 300mV/A and the slope compensation is 500mV/T. The reference for the current loop is provided by the output of an error amplifier (EA), which compares the feedback signal at the FB pin to the integrated 0.8V reference. Thus, the output voltage is regulated by using the error amplifier to control the reference for the current loop. The error amplifier is an operational amplifier that converts the voltage error signal to a voltage output. The voltage loop is internally compensated with the 50pF and 320kΩ RC network that can support most applications.

PWM operation is initialized by the clock from the oscillator. The HS MOSFET is turned on at the beginning of a cycle and the current in the MOSFET starts to ramp up. When the sum of the current amplifier, CSA, signal and the slope compensation, SE, reaches the control reference of the current loop, the PWM comparator sends a signal to the logic to turn off the HS MOSFET and turn on the LS MOSFET. The LS MOSFET stays on until the end of the cycle. Figure 55 shows the typical operating waveforms during continuous-conduction mode (CCM) operation. The dotted lines illustrate the sum of the compensation ramp and the current-sense amplifier's output.

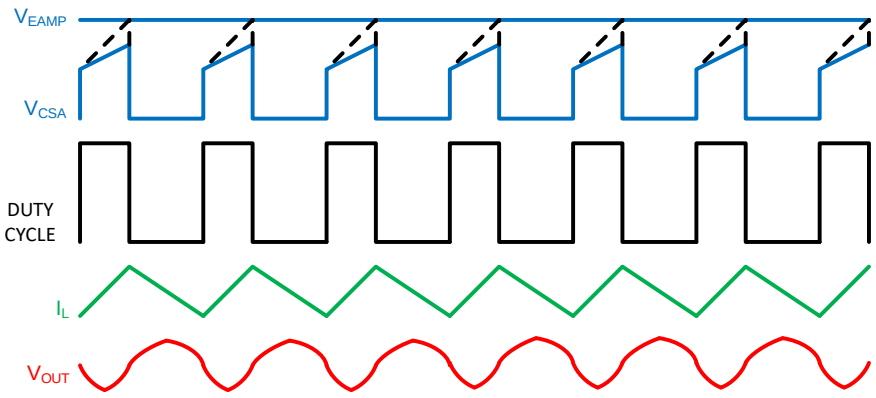


Figure 55. CCM Operation Waveforms

Functional Description (continued)

PFM Control Scheme

The AL8890/AL88902 enters a pulse-skipping mode at light load to minimize the switching loss by reducing the switching frequency. Figure 56 illustrates the PFM operation. A zero-cross sensing circuit shown in Figure 4 monitors the LS MOSFET current for zero crossing. When 8 consecutive cycles are detected, the regulator enters the PFM mode. The counter is reset to zero when the current in any cycle does not cross zero. Once the PFM mode is entered, the pulse modulation starts being controlled by the PFM comparator shown in Figure 4. The HS MOSFET is turned on at the clock's rising edge and turned off when its current reaches the peak PFM current-limit value. Then, the inductor current is discharged to 0A, stays at zero, and the output voltage reduces gradually due to the load current discharging the output capacitor. When the output voltage drops to the nominal voltage, the HS MOSFET is turned on again as it repeats the previous operations. The regulator resumes normal PWM mode operation when the output voltage drops 2.5% below the nominal voltage.

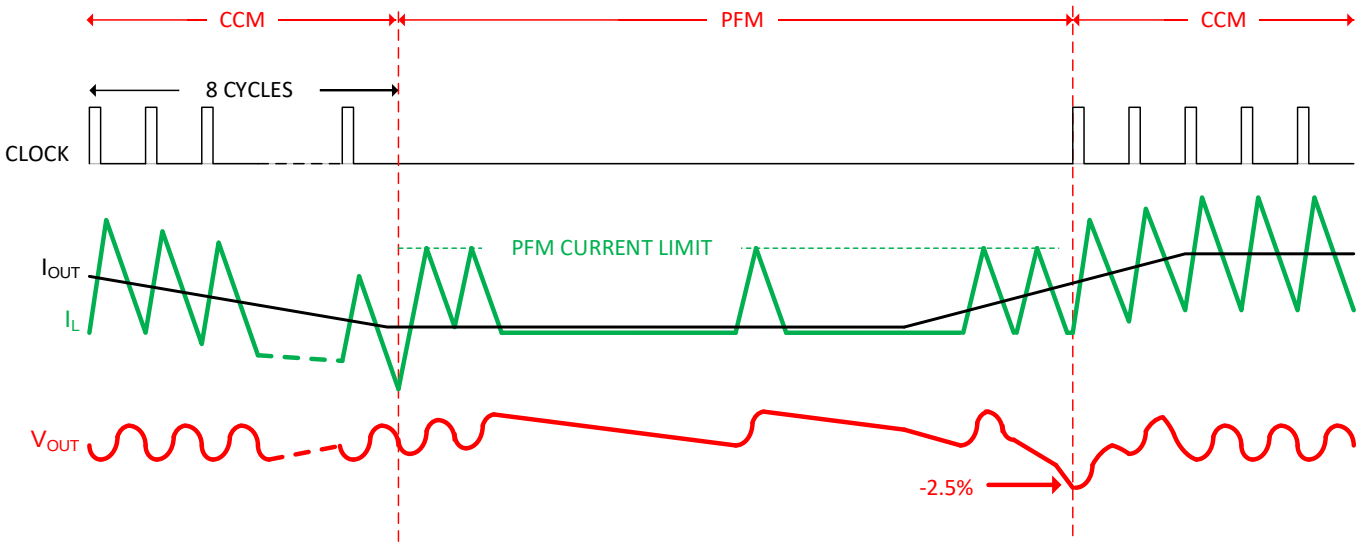


Figure 56. PFM Operation Waveforms

Application Information

Input Capacitor

The input capacitor reduces the surge current drawn from the input supply and the switching noise from the device. The input capacitor has to sustain the ripple current produced during the on-time on the upper MOSFET. It must hence have a low ESR to minimize the losses.

The RMS current rating of the input capacitor is a critical parameter that must be higher than the RMS input current. As a rule of thumb, select an input capacitor which has an RMS rating that is greater than half of the maximum load current.

Due to large di/dt through the input capacitors, electrolytic or ceramics should be used. If a tantalum must be used, it must be surge protected. Otherwise, capacitor failure could occur. For most applications, a 10µF ceramic capacitor is sufficient and 0.1µF parallel capacitor is also recommended for improving the stability.

Inductor

Calculating the inductor value is a critical factor in designing a buck converter. For most designs, the following equation can be used to calculate the inductor value:

$$L = \frac{V_{OUT} \cdot (V_{IN} - V_{OUT})}{V_{IN} \cdot \Delta I_L \cdot f_{SW}}$$

Where ΔI_L is the inductor ripple current and f_{SW} is the buck converter switching frequency.

Choose the inductor ripple current to be 30% to 40% of the maximum load current. The maximum inductor peak current is calculated from:

$$I_{L(MAX)} = I_{LOAD} + \frac{\Delta I_L}{2}$$

Peak current determines the required saturation current rating, which influences the size of the inductor. Saturating the inductor decreases the converter efficiency while increasing the temperatures of the inductor and the internal MOSFETs. Hence, choosing an inductor with appropriate saturation current rating is important.

An inductor with a DC current rating of at least 25% higher than the maximum load current is recommended for most applications. For highest efficiency, the inductor's DC resistance should be as low as possible. Use a larger inductance for improved efficiency under light load conditions.

Output Capacitor

The output capacitor keeps the output voltage ripple small, ensures feedback loop stability and reduces the overshoot of the output voltage. The output capacitor is a basic component for the fast response of the power supply. In fact, during load transient, for the first few microseconds it supplies the current to the load. The converter recognizes the load transient and sets the duty cycle to maximum, but the current slope is limited by the inductor value.

ESR of the output capacitor dominates the output voltage ripple. The amount of ripple is approximated using the equation below:

$$Vout_{capacitor} = \Delta I_{inductor} * (ESR + \frac{1}{8f_{SW}C_O})$$

An output capacitor with ample capacitance and low ESR is the best option. For most applications, a 22µF ceramic capacitor will be sufficient.

$$C_o = \frac{L(I_{out} + \frac{\Delta I_{inductor}}{2})^2}{(\Delta V + V_{out})^2 - V_{out}^2}$$

Where ΔV is the maximum output voltage overshoot.

Bootstrap

The internal driver of the HS FET is equipped with a BST undervoltage detection (UV) circuit. In the event that the voltage difference between BST and SW falls below 2V, the UV detection circuit allows the LS FET on for 400ns to recharge the bootstrap capacitor.

Self-Bias Mode

For highest possible efficiency operation, it is recommended to connect the BIAS pin directly to V_{OUT} or other external supply in the range of 4.5V to 15V. In this condition, the internal LDO will source from the BIAS voltage to minimize the power dissipation. Therefore, the overall efficiency is improved.

Application Information (continued)

External Soft-Start Discharge when the Accurate EN Feature is in Use

1) During power-down, when EN pin voltage is between 0.9V and 1.35V
   a) only the internal buck regulator was turned off, and V_{CC} (4.8V) is still active.
   b) C_{SS} is discharged by the internal 500kΩ resistor in series with a 210Ω MOSFET switch controlled by V_{CC}.
2) During power-down, when EN pin voltage drops below 0.9V
   c) V_{CC} (4.8V) will turned off and also the internal 210Ω MOSFET switch turns off
   d) resulting in high impedance on the SS pin and a very slow C_{SS} decay.
3) If the device is power-up before the entire power-down cycle and the V_{CSS} is still higher than 0.9V due to a very slow C_{SS} decay
   e) the device SS pin will set back to use the internal 1.7ms soft-start time, even though an external C_{SS} capacitor is connected to the SS pin.

Suggestion to Handling This Discharge Properly when Using External Soft-Start Setup:

1) Connect a 2MΩ resistor to GND in parallel with the C_{SS} capacitor to help the C_{SS} capacitor discharge quicker.

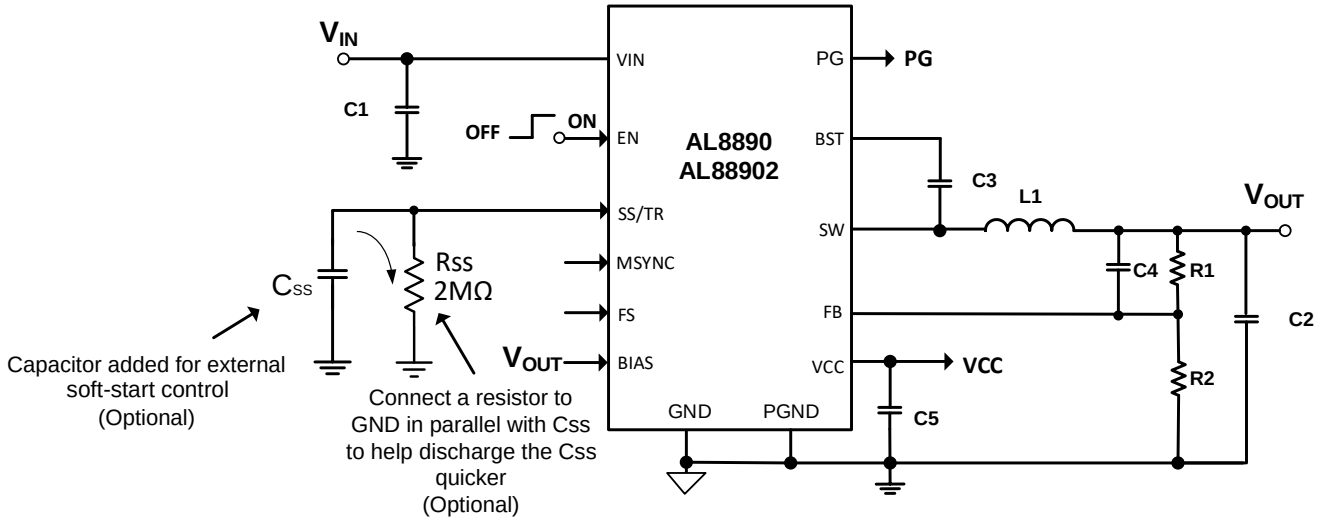


Figure 57. Resistor Added at SS Pin to Discharge C_{SS} Capacitor Quicker

Analog Dimming Operation in Contant Current Output Application

To save power loss on current-sense resistor through LED string in constant current output system, suggest setting max voltage on SS/TR pin not above 200mV. SS/TR pin also could be used as analog dimming signal input pin. Output current is regulated from 0 to 100% with 0 to 0.2V.

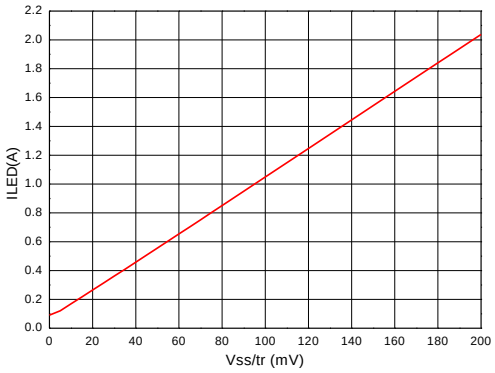


Figure 58. Analog Dimming Curve with 0 to 0.2V Dimming on SS/TR Pin

Application Information (continued)

Loop Compensation Design

The regulator uses constant frequency peak current-mode control architecture to achieve a fast loop transient response. An accurate current sensing pilot device in parallel with the upper MOSFET is used for peak current control signal and overcurrent protection. The inductor is not considered as a state variable since its peak current is constant, and the system becomes a single order system. It is much easier to design a Type 2 compensator to stabilize the loop than to implement voltage mode control. Peak current-mode control has an inherent input voltage feed-forward function to achieve good line regulation. Figure 59 shows the small signal model of the synchronous buck regulator and Figure 60 is the compensation network.

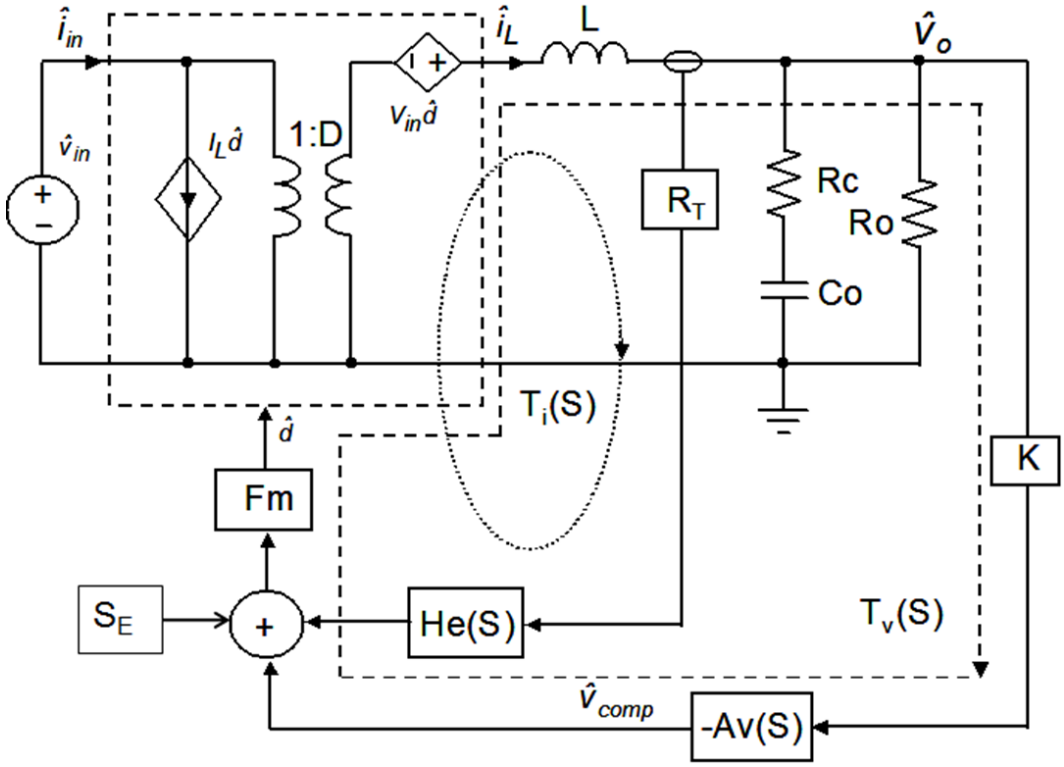


Figure 59. Linearized Small Signal Model

Figure 60 is the type 2 compensator.

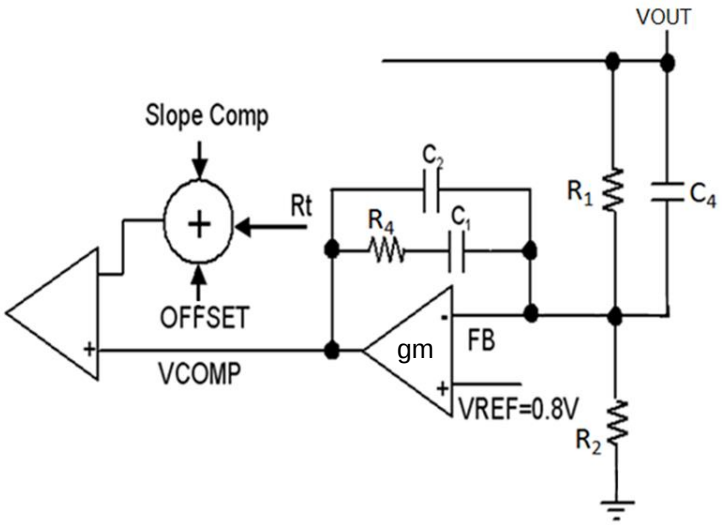


Figure 60. Type 2 Compensator

Application Information (continued)

Compensation design goals are the following:

1. Crossover frequency, f_C, of approximately 1/10th of the switching frequency.
2. Phase margin > 40°.
3. Gain margin > 10dB in magnitude.

The loop gain at the crossover frequency has a unity gain. Therefore, the value of the top feedback resistance is determined by:

$$R_1 = \frac{136k}{C_o f_C V_{OUT}}$$

Where, C_O is the total output capacitance seen by the regulator. This may include ceramic high frequency decoupling and bulk output capacitors. Ceramic will have a derating factor by approximately 40% depending on dielectric, voltage stress, and thermal.

An additional zero contribution due to R_1 and C_4 can boost the phase margin. Put the compensator zero between 1/2f_C to f_C frequency.

$$C_4 = \frac{1}{2\pi f c R_1}$$

Layout

PCB Layout

1. The AL8890/AL88902 is a high switching frequency converter. Hence, attention must be paid to the switching currents interference in the layout. Switching current from one power device to another can generate voltage transients across the impedances of the interconnecting bond wires and circuit traces. These interconnecting impedances should be minimized by using wide, short printed circuit traces. The AL8890/AL88902 works at 3.5A/2.5A load current so heat dissipation is a major concern in the layout of the PCB. 2oz copper for both the top and bottom layers is recommended. Four layers PCB is recommended to minimize ground noise.
2. Place the input capacitors as closely across VIN and GND as possible.
3. Place the inductor as close to SW as possible.
4. Place the output capacitors as close to GND as possible.
5. Place the feedback components as close to FB as possible.
6. If using four or more layers, use at least the 2nd and 3rd layers as GND to maximize thermal performance.
7. Add as many vias as possible around both the GND pin and under the GND plane for heat dissipation to all the GND layers.
8. Add as many vias as possible around both the VIN pin and under the VIN plane for heat dissipation to all the VIN layers.
9. See Figure 61 for more details.

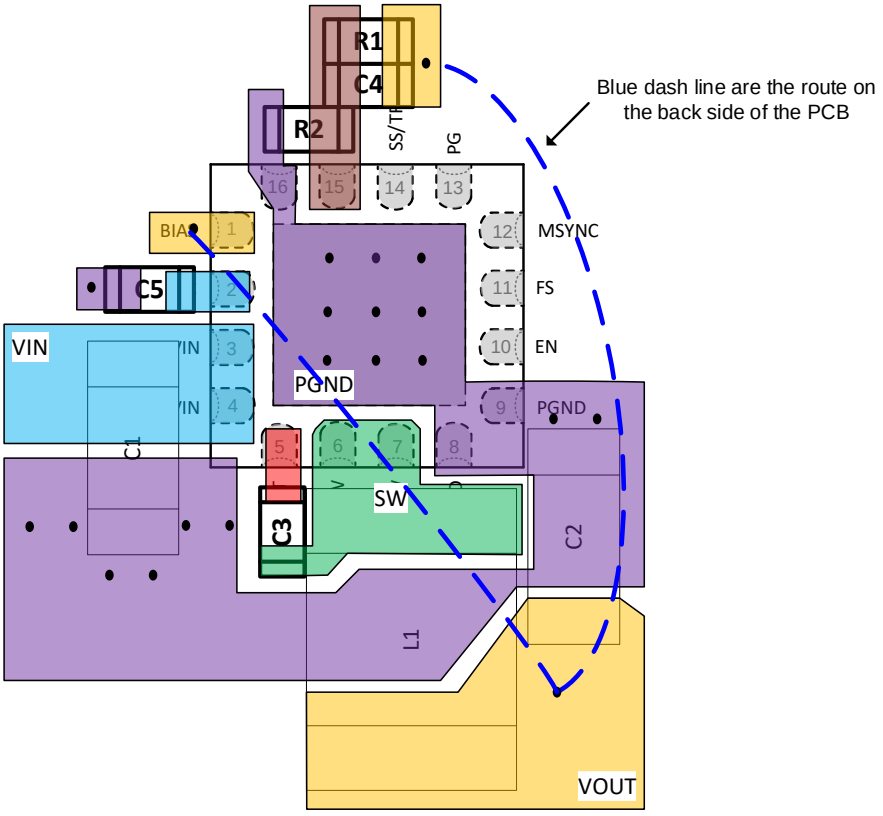
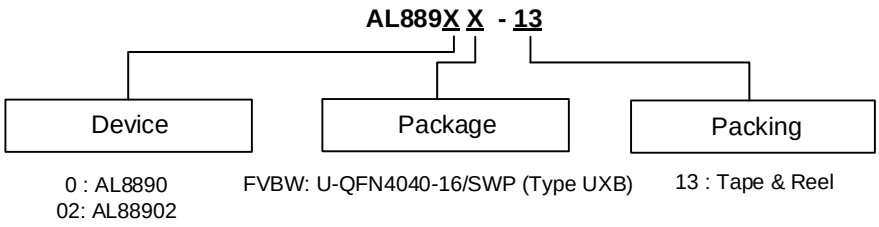


Figure 61. PC Board Layout with U-QFN4040-16/SWP (Type UXB) Package Device

Design Resources (https://www.diodes.com/design/tools/)

- AL8890 EV1 Evaluation Board User Guides
- AL88902 EV1 Evaluation Board User Guides
- AL8890/AL88902 Simplis Model
- AL8890/AL88902 Design Calculators

Ordering Information (Note 9)



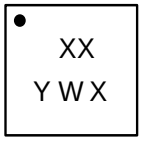
Orderable Part Number	Package Code	Package	Identification Code	Packing	
				Qty.	Carrier
AL8890FVBW-13	FVBW	U-QFN4040-16/SWP (Type UXB)	F5	3000	Tape and Reel
AL88902FVBW-13			F6		

Note: 9. For packaging details, go to our website at https://www.diodes.com/design/support/packaging/diodes-packaging/.

Marking Information

U-QFN4040-16/SWP (Type UXB)

(Top View – Not to Scale)



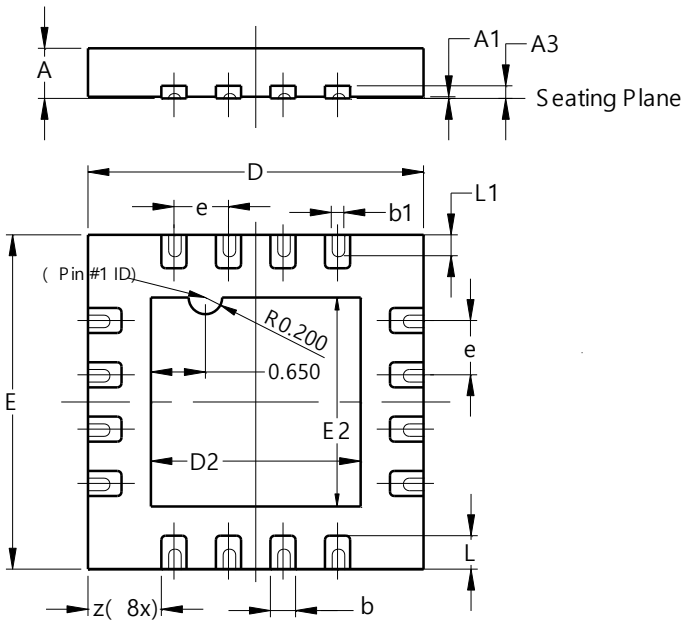
XX : Identification Code
Y : Year : 0 to 9 (ex: 4 = 2024)
W : Week : A to Z : week 1 to 26;
a to z : week 27 to 52; z represents week 52 and 53
X : Internal Code

Orderable Part Number	Package	Identification Code
AL8890FVBW-13	U-QFN4040-16/SWP (Type UXB)	F5
AL88902FVBW-13	U-QFN4040-16/SWP (Type UXB)	F6

Package Outline Dimensions

Please see http://www.diodes.com/package-outlines.html for the latest version.

U-QFN4040-16/SWP (Type UXB)

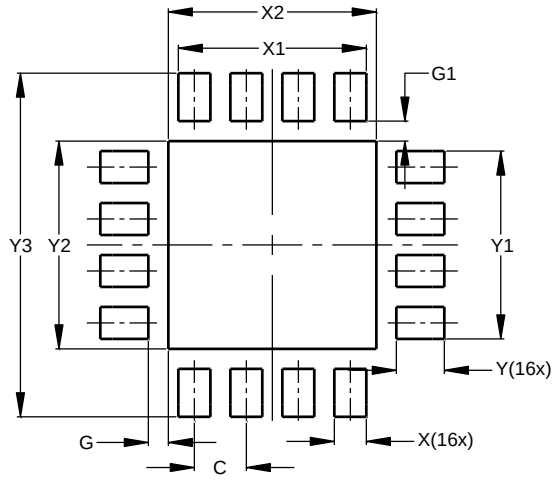


U-QFN4040-16/SWP (Type UXB)			
Dim	**Min**	**Max**	**Typ**
A	0.57	0.63	0.60
A1	0.00	0.05	0.02
A3	--	--	0.15
b	0.25	0.35	0.30
b1	--	--	0.15
D	3.95	4.05	4.00
D2	2.40	2.60	2.50
E	3.95	4.05	4.00
E2	2.40	2.60	2.50
e	--	--	0.65
L	0.35	0.45	0.40
L1	--	--	0.25
z	0.850	0.900	0.875
All Dimensions in mm			

Suggested Pad Layout

Please see http://www.diodes.com/package-outlines.html for the latest version.

U-QFN4040-16/SWP (Type UXB)



Dimensions	Value (in mm)
C	0.650
G	0.250
G1	0.250
X	0.400
X1	2.350
X2	2.600
Y	0.600
Y1	2.350
Y2	2.600
Y3	4.300

Mechanical Data

- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals: Finish – Matte Tin Plated Leads, Solderable per MIL-STD-202, Method 208 e3
- Weight: 0.035 grams (Approximate)

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