Description

The AL8891Q is an easy-to-use synchronous step-down DC-DC LED driver with high-side current sense capable of driving up to 2A of constant current from an input voltage ranging from 4.5V to 65V. The AL8891Q provides high switching frequency up to 2.5MHz to optimize high efficiency, allowing a smaller inductor size and compact form factor solution. Pin arrangement allows simple, optimum PCB layout. Constant on time control is employed to achieve simple control-loop compensation and cycle-by-cycle current limiting with fast dynamic response.

Features such as fault flag, PWM and analog dimming, internal soft-start, and shutdown provide a flexible and easy-to-use platform for a wide range of applications. Discontinuous conduction and automatic frequency reduction at light loads improve light-load efficiency.

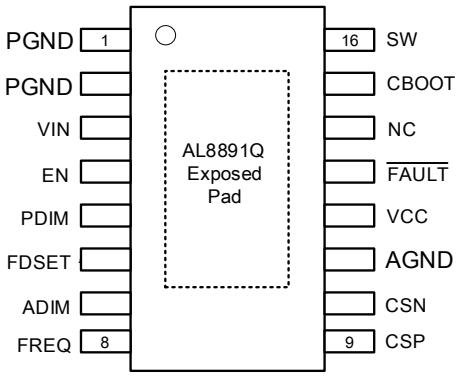
Protection features include thermal shutdown, VIN and VCC undervoltage lockout, cycle-by-cycle current limit, output open & short-circuit protection for LED, and external components open & short protection.

The AL8891Q device is available in the thermal enhanced TSSOP-16EP package.

Pin Assignments

(3D Step file available)

Top View – (Not to Scale)



TSSOP-16EP

Features

- AEC-Q100 Grade 1
- Input voltage 4.5V to 65V
- VOUT close to VIN rail (up to 99% duty cycle)
- Integrated MOSFETs high-side 200mΩ and low-side 130mΩ
- 2A constant output current
- High-side current sense
- Support both PWM and analog dimming
- Internal compensation without external capacitor
- Cycle-by-cycle current protection
- Diagnosis and fault flag indicator
- LED open and short protection
- Overtemperature thermal protection and auto-restart
- Ambient temperature -40°C to +125°C
- Thermally enhanced TSSOP-16EP package
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**
- **The AL8891Q is suitable for automotive applications requiring specific change control; this part is AEC-Q100 qualified, PPAP capable, and manufactured in IATF16949 certified facilities.**
  https://www.diodes.com/quality/product-definitions/

Applications

- Automotive head lights
- Daytime running lights (DRL)
- Front and rear fog lights
- Turn/stop lights
- Map lights
- Dimmable interior/exterior lights

Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

Typical Applications Circuit

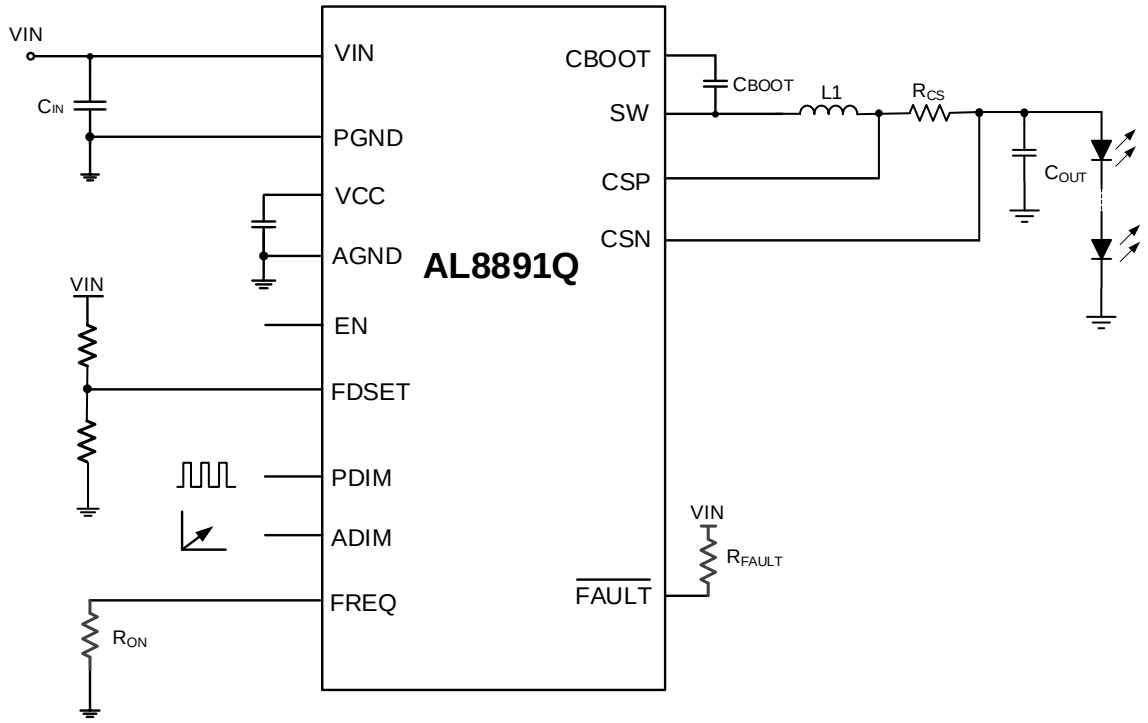


Figure 1. Typical Application

Functional Block Diagram

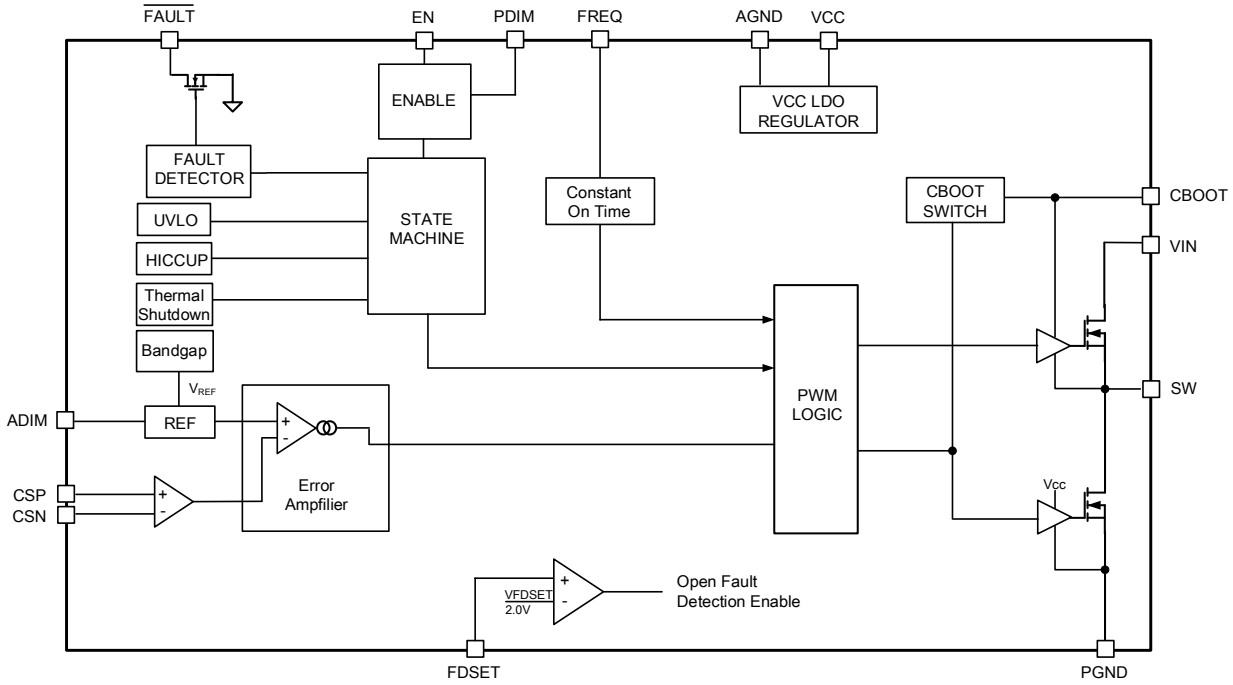


Figure 2. Functional Block Diagram

Pin Descriptions

Pin Name	Pin Number (TSSOP-16EP)	Function
PGND	1, 2	Power ground. Connect the pins to ground plane.
VIN	3	Power supply input pin to high-side power MOSFET and VIN LDO regulator. Decouple this pin to GND with ceramic capacitors.
EN	4	Enable pin for VCC LDO regulator and input voltage for VIN UVLO. Connect to VIN directly through a resistor divider, or to an external voltage source. This pin can also achieve PWM dimming by connecting to an external pulse signal.
PDIM	5	PWM dimming input pin. Apply PWM signal for PWM dimming. Connect to high-level voltage when not in use. Do not leave it floating.
FDSET	6	Set VIN rising threshold to mask LED open fault. Connect to an external divider to detect VIN rising condition.
ADIM	7	Apply an analog voltage for analog dimming. Do not leave it floating.
FREQ	8	Switching frequency control pin. Place a resistor between this pin and AGND to set the switching frequency between 200kHz and 2.5MHz.
CSP	9	Current sense positive input across RCS
CSN	10	Current sense negative input across RCS
AGND	11	Analog ground for regulator and system. All electrical parameters are measured with respect to this pin. Connect to EP and PGND on PCB.
VCC	12	Internal VCC regulator that powers the control circuits. Must be decoupled to PGND with 1µF to 4.7µF ceramic capacitor.
$\overline{\text{FAULT}}$	13	FAULT Indication. Asserted Low to report faulty conditions. Needs an external pullup resistor.
NC	14	Not Connected, leave it floating.
CBOOT	15	Bootstrap supply input for high-side gate driver. Connect a 100nF ceramic capacitor from this pin to SW pin.
SW	16	Regulator switch node. Connect to power inductor.
Exposed Thermal Pad	—	Connect to ground plane for adequate heat sinking and noise reduction.

Absolute Maximum Ratings (Note 4)

Symbol	Parameter	Rating	Unit
V_{IN}	Input voltages, VIN to PGND	-0.3 to +72	V
V_{EN}, V_{FAULT}	Input voltages, EN, $\overline{FAULT}$ to AGND		V
V_{AGND}	Input voltages, AGND to PGND	-0.3 to +0.3	V
V_{PDIM}, V_{ADIM}, V_{FREQ}, V_{FDSET}	Input voltages, PWM, ADIM to AGND	-0.3 to +5.5	V
V_{SW}	Output voltages, SW to PGND	-0.3 to V_{IN}+0.3	V
V_{SW_PK}	Output voltages, SW to PGND less than 10ns transients	-3.5 to +72	V
V_{CSP}, V_{CSN}	Input voltages, CSP, CSN to AGND	-0.3 to +72	V
V_{CBOOT_SW}	Output voltages, CBOOT to SW	-0.3 to +5.5	V
V_{CC}	Output voltages, VCC to AGND	-0.3V to +5.5	V
T_J	Operating junction temperature	-40 to +150	°C
T_{ST}	Storage temperature	-55 to +150	°C
V_{ESD}	Human body model (HBM)	±2000	V
	Charged-device model (CDM)	±1000	

Note: 4. Stresses greater than those listed under *Absolute Maximum Ratings* can cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to *Absolute Maximum Ratings* for extended periods can affect device reliability.

Thermal Information (Note 5)

Package	θ_{JC} Thermal Resistance Junction-to-Case	θ_{JA} (Note 5) Thermal Resistance Junction-to-Ambient	P_{DIS} T_A = +25°C
TSSOP-16EP	23°C/W	50°C/W	2.5W

Note: 5. The device is mounted on JEDEC standard 4 layers (2s2p) PCB test board.

Recommended Operating Conditions (Over operating free-air temperature range, unless otherwise specified.) (Note 6)

Parameter		Min	Typ	Max	Unit
Input voltages	V_{IN} to PGND	4.5	—	65	V
	EN	0	—	V_{IN}	
	PDIM, ADIM, FDSET	0	—	5.5	
	AGND to PGND	-0.1	—	0.1	
Output voltage, CBOOT		1	—	65	V
Output voltage, VOUT		1	—	65	V
Output current, IOUT		0	—	2	A
Operating junction temperature range, T_J		-40	—	+150	°C
Operating ambient temperature range, T_A		-40	—	+125	°C

Note: 6. Operating ratings indicate conditions for which the device is intended to be functional, but do not ensure specific performance limits. For verified specifications, see *Electrical Characteristics*.

Electrical Characteristics

Limits apply to the recommended operating junction temperature (T_J) range of -40°C to +150°C, unless otherwise stated. Minimum and Maximum limits are specified through test, design or statistical correlation. Unless otherwise stated, the following conditions apply: V_{IN} = 24V, f_S = 400kHz.

Symbol	Parameter	Condition	Min	Typ	Max	Unit
Supply Voltage (VIN Pin)						
V_{IN_MIN}	Minimum input voltage for startup	—	—	—	4.5	V
I_{SHDN}	Shutdown quiescent current	V_{IN} = 24 V, V_{EN} = 0V	—	0.1	10	μA
I_{Q_SW}	Operating quiescent current (switching)	V_{EN} = V_{IN} = 24V, I_{OUT} = 0A f_S = 400kHz	—	1.0	—	mA
Enable V_{IN} UVLO (EN Pin)						
EN_{VCC-ON}	V_{EN} high-level threshold	V_{EN} rising	2.2	—	—	V
$EN_{VCC-OFF}$	V_{EN} low-level threshold	V_{EN} falling	—	—	0.7	V
$V_{IN\_UVLO\_R}$	V_{IN} UVLO rising threshold	V_{IN} rising	4.0	4.2	4.45	V
$V_{IN\_UVLO\_F}$	V_{IN} UVLO falling threshold	V_{IN} falling	—	3.9	—	V
I_{Q-EN}	EN pin current	V_{EN} = 3.3V	—	1	—	μA
$t_{EN\_OFF\_DELAY}$	EN turned off delay	—	6	23	40	ms
Internal LDO (VCC Pin)						
V_{CC}	Internal LDO output voltage V_{CC}	V_{IN} ≥ 6V, I_{VCC} > 15mA	4.4	5.0	5.7	V
I_{VCC_LIMIT}	V_{CC} current limit	V_{IN} > 6V, V_{CC} = 4.5V	30	—	—	mA
V_{CC_UVLO}	Undervoltage lockout (UVLO) thresholds for V_{CC}	V_{CC} rising threshold	3.4	3.6	3.8	V
		V_{CC} thresholds hysteresis	—	0.15	—	mV
Current Control (CSP, CSN, ADIM Pins)						
$V_{CSP-CSN}$	CSP-CSN voltage	V_{ADIM} = 2V	192	200	208	mV
		V_{ADIM} = 1V	—	100	—	
		V_{ADIM} = 0.4V	—	40	—	
$V_{CSPN-LOW\ CLAMP}$	Analog dimming low clamp	V_{ADIM} ≤ 0.15V	—	20	—	mV
I_{CSN}	CSN sink current	V_{CSP} - V_{CSN} = 200mV, V_{CSN} > 5V	30	60	90	μA
Overcurrent Limit						
$I_{HS-LIMIT}$	Peak inductor current positive limit	V_{IN} = 24V	—	3.6	—	A
$I_{LS-LIMIT}$	Valley inductor current negative limit	V_{IN} = 24V	—	-1.6	—	A

Electrical Characteristics (continued)

Limits apply to the recommended operating junction temperature (T_J) range of -40°C to +150°C, unless otherwise stated. Minimum and Maximum limits are specified through test, design or statistical correlation. Unless otherwise stated, the following conditions apply: V_{IN} = 24V, f_S = 400kHz.

Symbol	Parameter	Condition	Min	Typ	Max	Unit
Power MOSFETs (Note 7)						
R_{DSON_HS}	High-side MOSFET ON-resistance (Note 8)	I_{OUT} = 0.5A, V_{CBOOT} - V_{SW} = 5V	—	200	360	mΩ
R_{DSON_LS}	Low-side MOSFET ON-resistance (Note 8)	I_{OUT} = 0.5A, V_{CC} = 5V	—	130	240	mΩ
t_{ON} (SW, FREQ Pins)						
$t_{ON\_MIN\_HS}$	Minimum high-side MOSFET ON-time	T_A = +25°C, V_{IN} = 24V, V_{OUT} = 12V R_{ON} = 237kΩ, I_{LOAD} = 0A	—	65	90	ns
t_{ON}	Typical t_{ON} @400kHz	T_A = +25°C, V_{IN} = 24V, V_{OUT} = 12V R_{ON} = 237kΩ, I_{LOAD} = 0A	—	1250	—	ns
f	Typical 400kHz frequency	T_A = +25°C, V_{IN} = 24V, V_{OUT} = 12V R_{ON} = 237kΩ, I_{LOAD} = 0A	—	400k	—	Hz
%F	Frequency over 400kHz target	V_{IN} = 4.5V to 65V V_{OUT} = 3V to V_{IN} x 95%, R_{ON} = 237kΩ I_{LOAD} = 0A, full temperature range	80	—	120	%
$t_{ON\_2.1M}$	Typical t_{ON} @2.1MHz	T_A = +25°C, V_{IN} = 24V, V_{OUT} = 12V R_{ON} = 43kΩ, I_{LOAD} = 0A	—	238	—	ns
$f_{2.1M}$	Typical 2.1MHz frequency	T_A = +25°C, V_{IN} = 24V, V_{OUT} = 12V R_{ON} = 43kΩ, I_{LOAD} = 0A	—	2.1M	—	Hz
$\%F_{2.1M}$	Frequency over 2.1MHz target	V_{IN} = 4.5V to 65V V_{OUT} = 3.5V to V_{IN} x 85%, R_{ON} = 43kΩ I_{LOAD} = 0A, full temperature range	80	—	120	%
$t_{OFF\_MIN\_HS}$	Minimum high-side MOSFET OFF-time (Note 7)	—	—	100	—	ns
Dimming (PDIM Pin)						
V_{PDIM}	PDIM input threshold	Rising	1.5	—	—	V
		Falling	—	—	0.7	V
$t_{ON\_PDIM\_MIN}$	Minimum PWM on time with FAULT recovery	—	—	360	—	µs
Spread Spectrum (Measured at SW Pin)						
t_{ON_SS}	t_{ON} spread spectrum amplitude	T_A = +25°C, V_{IN} = 24V, V_{OUT} = 12V R_{ON} = 238.5kΩ, I_{LOAD} = 0A	—	±10	—	%
f_{SS}	t_{ON} spread spectrum frequency	T_A = +25°C, V_{IN} = 24V, V_{OUT} = 12V R_{ON} = 238.5kΩ, I_{LOAD} = 0A	—	20	—	kHz

Notes: 7. Guaranteed by design.
8. Measured at package pins.

Electrical Characteristics (continued)

Limits apply to the recommended operating junction temperature (T_J) range of -40°C to +150°C, unless otherwise stated. Minimum and Maximum limits are specified through test, design or statistical correlation. Unless otherwise stated, the following conditions apply: V_{IN} = 24V, f_S = 400kHz.

Symbol	Parameter	Condition	Min	Typ	Max	Unit
Fault Detection						
$V_{FT\_SHORT\_FALL}$	LED short threshold detected on CSN falling	V_{IN} = 24V	1.0	1.6	—	V
$V_{FT\_SHORT\_RISE}$	LED short threshold detected on CSN rising	V_{IN} = 24V	—	1.8	2.5	V
V_{PD_FAULT}	$\overline{\text{Fault}}$ pin pulldown strength	I_{FT} = 1mA	—	40	100	mV
t_{FDT}	$\overline{\text{Fault}}$ deglitch timer	—	—	80	—	µs
$t_{MASK-DET}$	$\overline{\text{Fault}}$ detect mask timer	—	—	160	—	µs
$t_{MASK-REL}$	$\overline{\text{Fault}}$ mask release timer	—	—	320	—	µs
I_{LEAK_FT}	$\overline{\text{Fault}}$ leakage current	V_{FT} = 5V	—	10	100	nA
V_{FDSET}	LED open-fault enable reference	Reference to AGND	1.8	2.0	2.2	V
R_{OPEN}	FREQ pin to GND open detect threshold	V_{CC} = 5V	2	—	—	MΩ
R_{SHORT}	FREQ pin to GND short detect threshold	V_{CC} = 5V	—	—	150	Ω
t_{RETRY}	Time for fault retry	—	—	1	—	ms
Thermal Shutdown						
T_{SD}	Thermal shutdown threshold	—	—	+170	—	°C
$T_{SD(HYS)}$	Thermal shutdown hysteresis	—	—	+20	—	°C

Typical Performance Characteristics (VIN = 24V, IOUT = 2A, COUT = 0.47µF, f_{SW} = 400kHz, unless otherwise specified.)

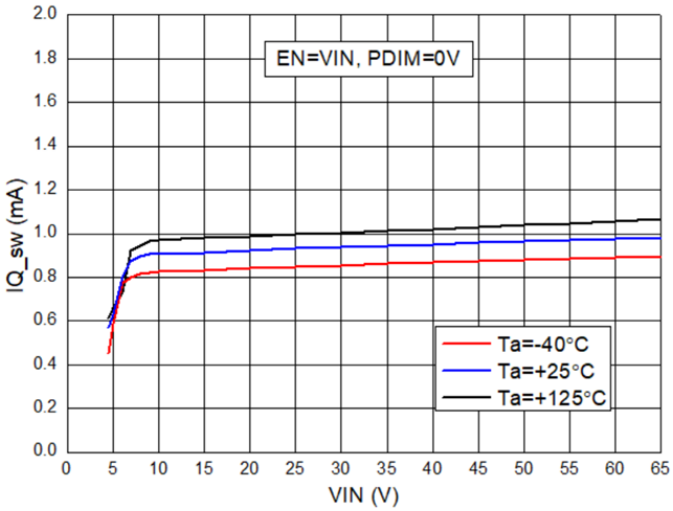


Figure 3. IQ_SW vs. VIN

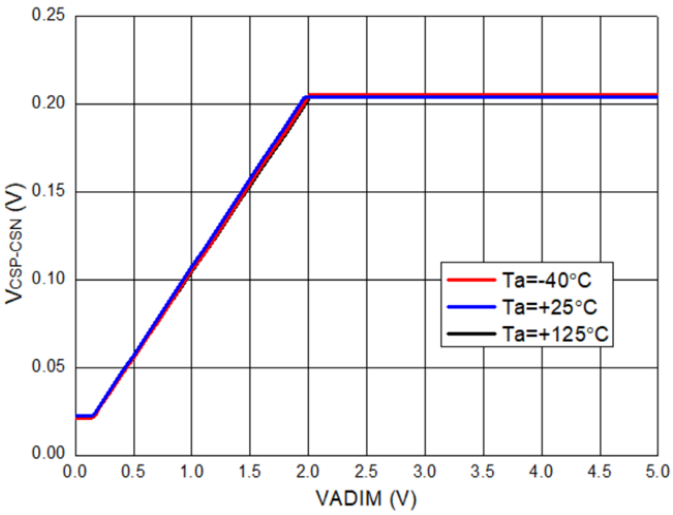


Figure 4. Analog Dimming Curve

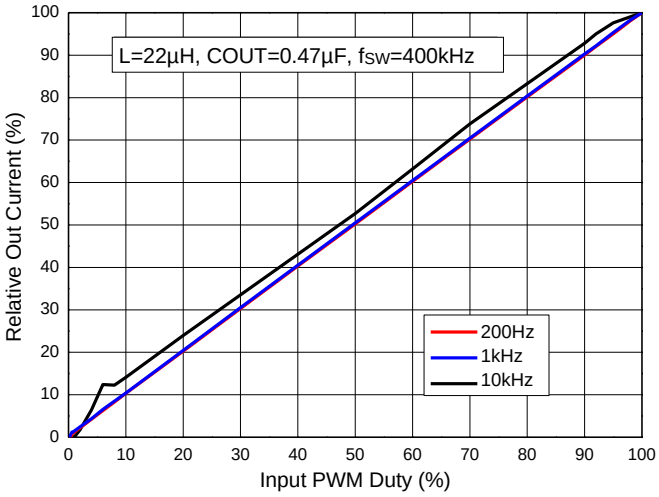


Figure 5. PWM Dimming Curve

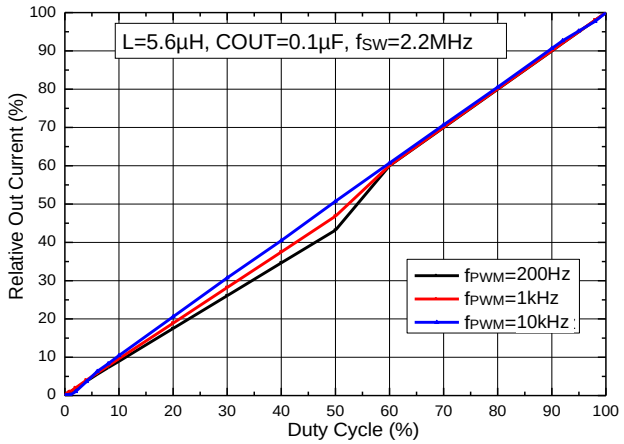


Figure 6. PWM Dimming Curve

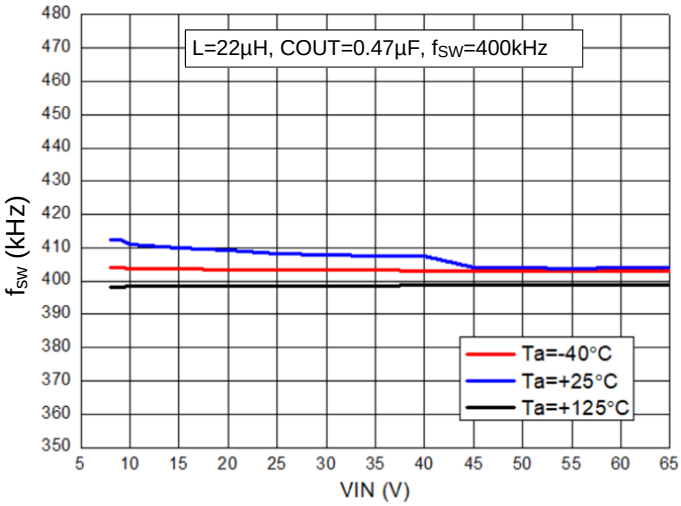


Figure 7. fsw vs. VIN

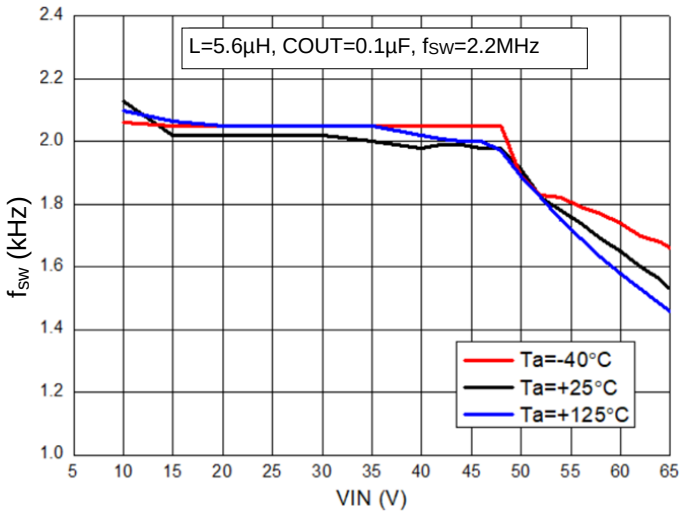


Figure 8. fsw vs. VIN

Typical Performance Characteristics (continued)

(VIN = 24V, IOUT = 2A, COUT = 0.47µF, f_{SW} = 400kHz, unless otherwise specified.)

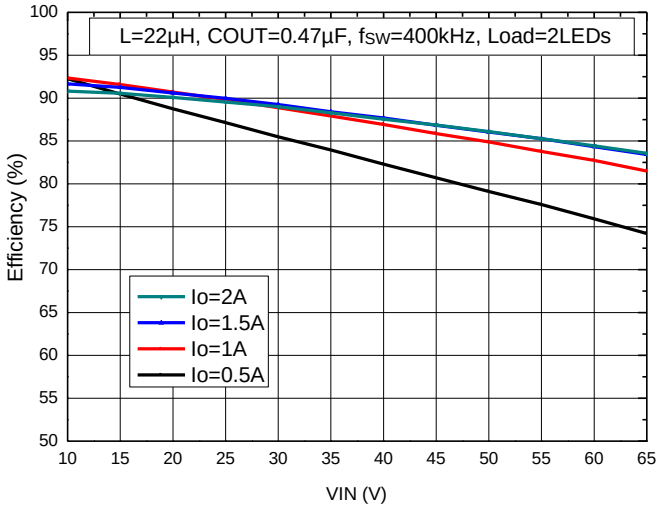


Figure 9. Efficiency vs. VIN

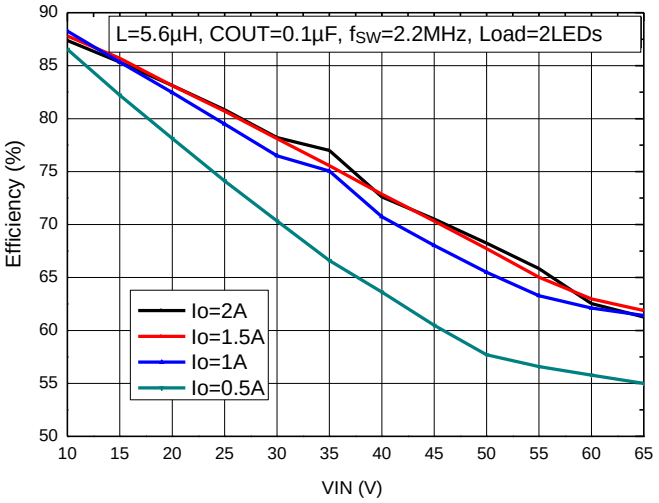


Figure 10. Efficiency vs. VIN

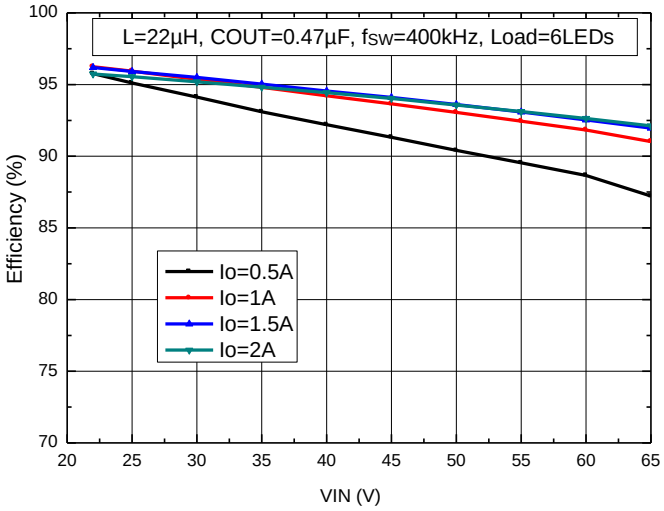


Figure 11. Efficiency vs. VIN

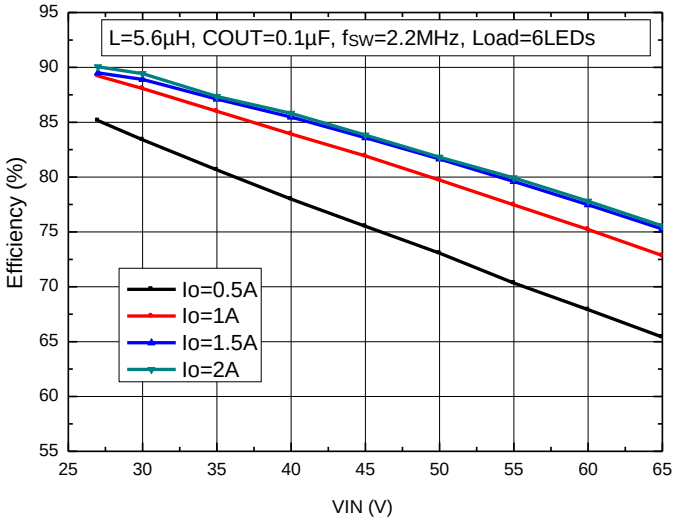


Figure 12. Efficiency vs. VIN

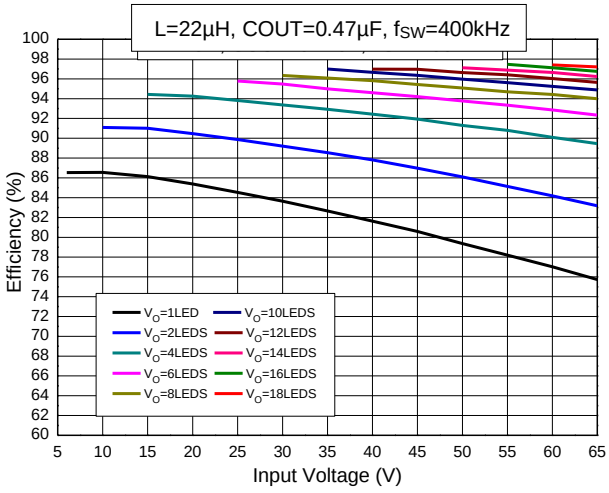


Figure 13. Efficiency vs. Input Voltage

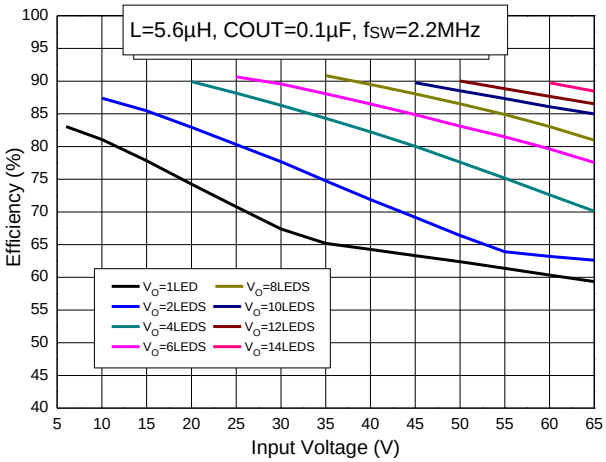


Figure 14. Efficiency vs. Input Voltage

Typical Performance Characteristics (continued)

(VIN = 24V, IOUT = 2A, COUT = 0.47µF, f_{SW} = 400kHz, unless otherwise specified.)

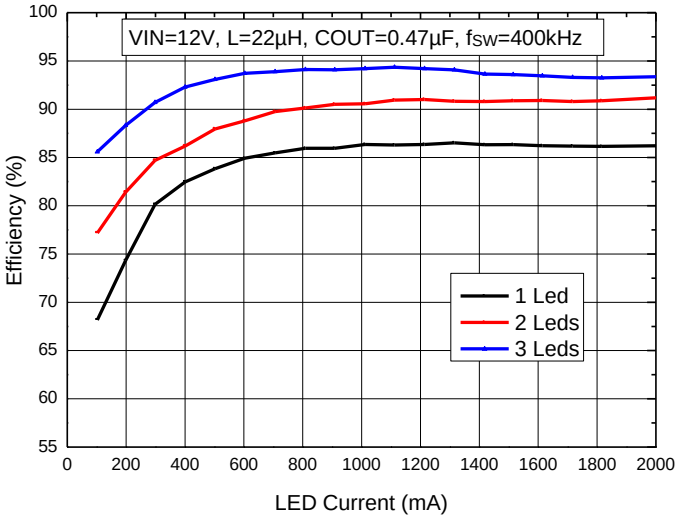


Figure 15. Efficiency vs. LED Current

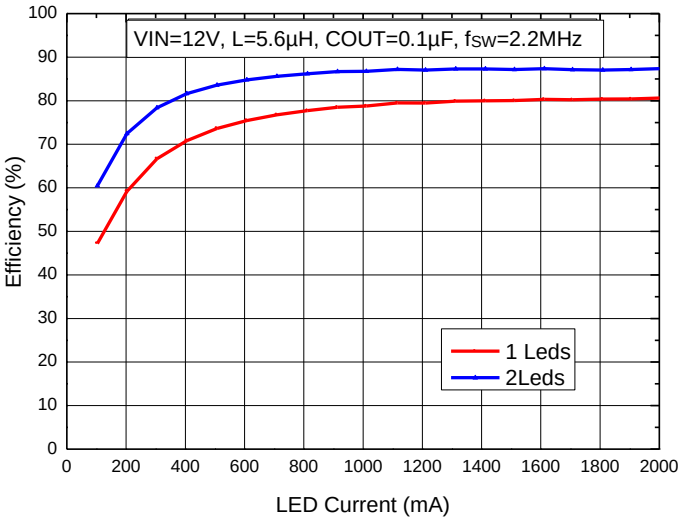


Figure 16. Efficiency vs. LED Current

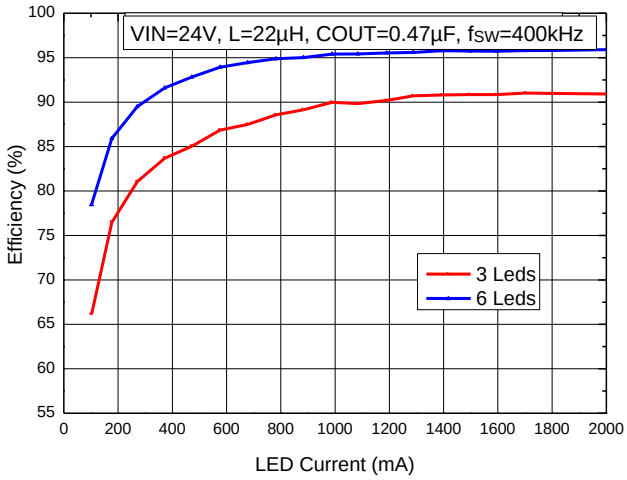


Figure 17. Efficiency vs. LED Current

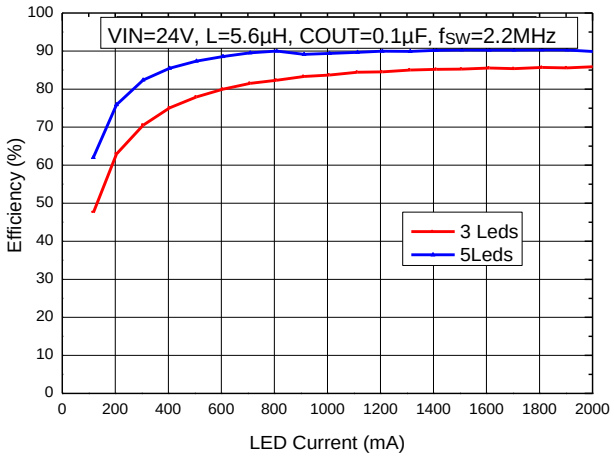


Figure 18. Efficiency vs. LED Current

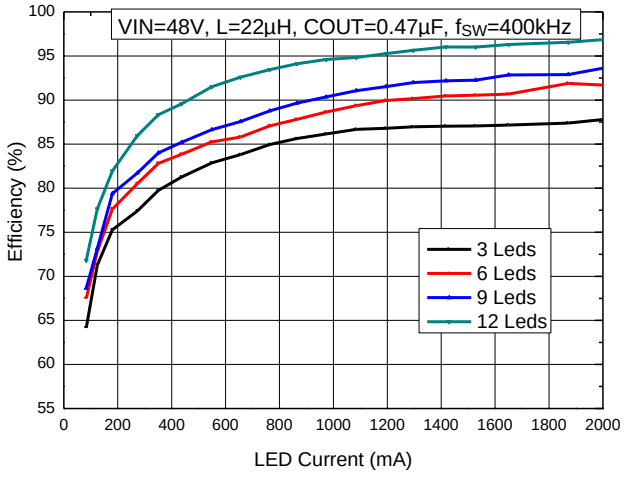


Figure 19. Efficiency vs. LED Current

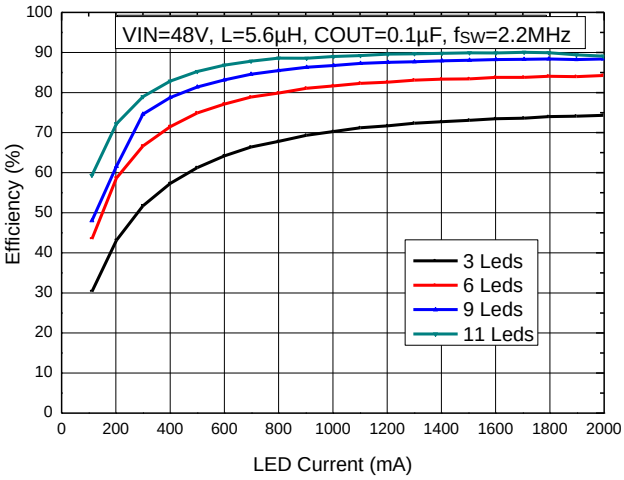


Figure 20. Efficiency vs. LED Current

Typical Performance Characteristics (continued)

(VIN = 24V, IOUT = 2A, COUT = 0.47µF, f_{SW} = 400kHz, unless otherwise specified.)

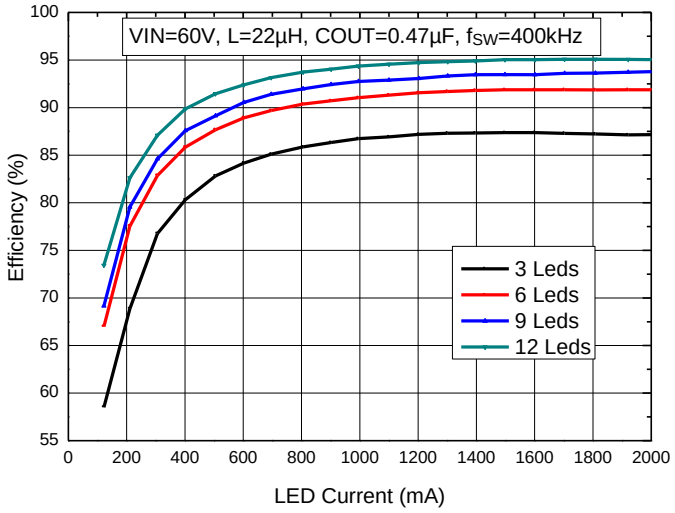


Figure 21. Efficiency vs. LED Current

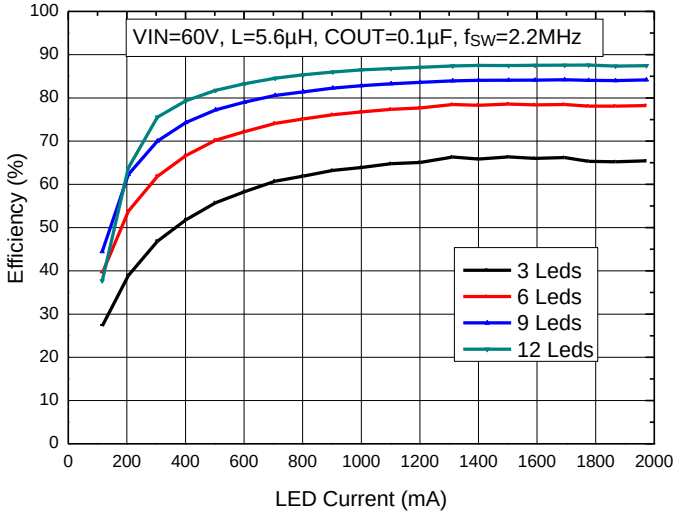


Figure 22. Efficiency vs. LED Current

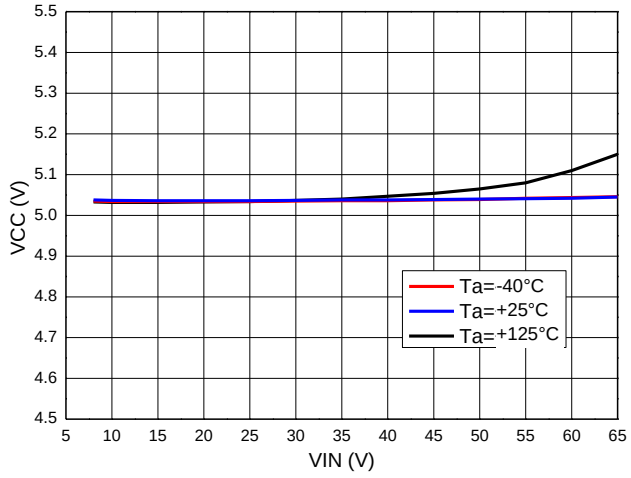


Figure 23. VCC vs. VIN

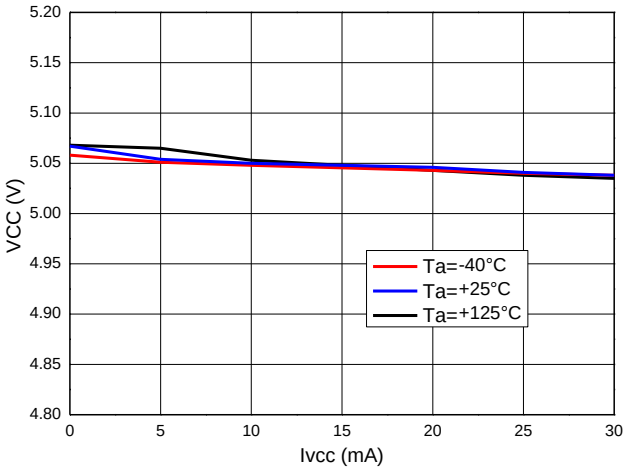


Figure 24. VCC vs. Ivcc

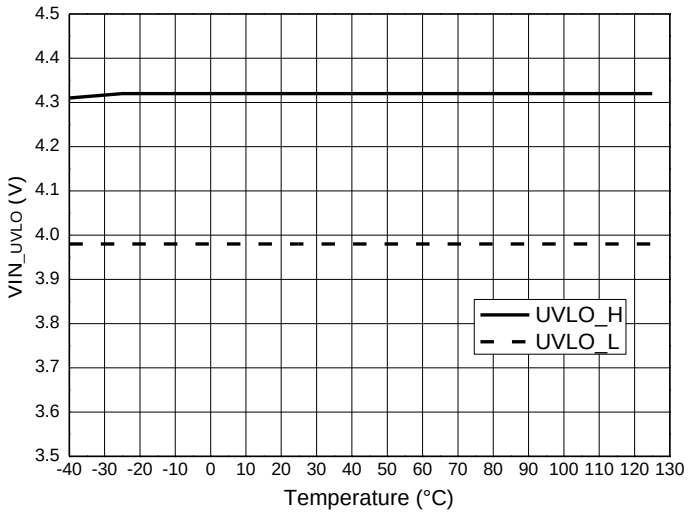


Figure 25. VIN UVLO vs. Temperature

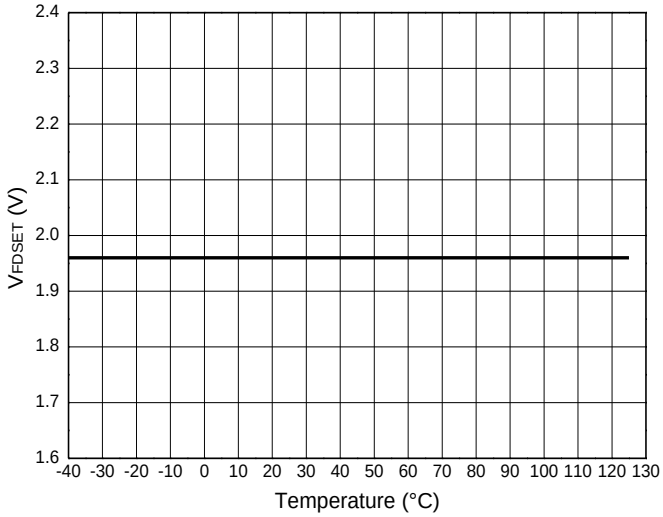


Figure 26. V_{FDSET} vs. Temperature

Typical Performance Characteristics (continued)

(VIN = 24V, IOUT = 2A, COUT = 0.47μF, f_{SW} = 400kHz, unless otherwise specified.)

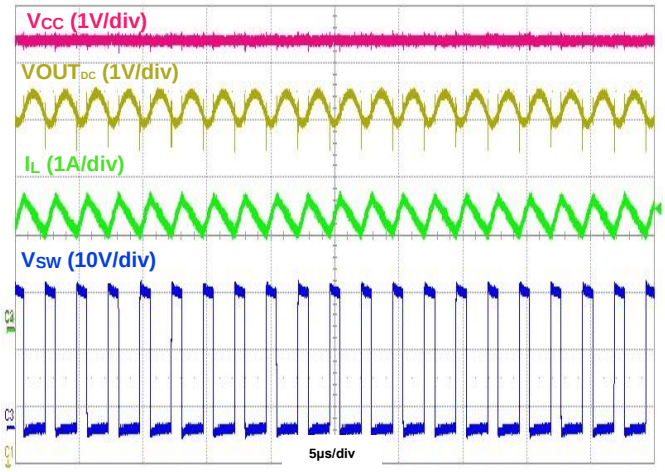


Figure 27. Steady State, Iout = 2A

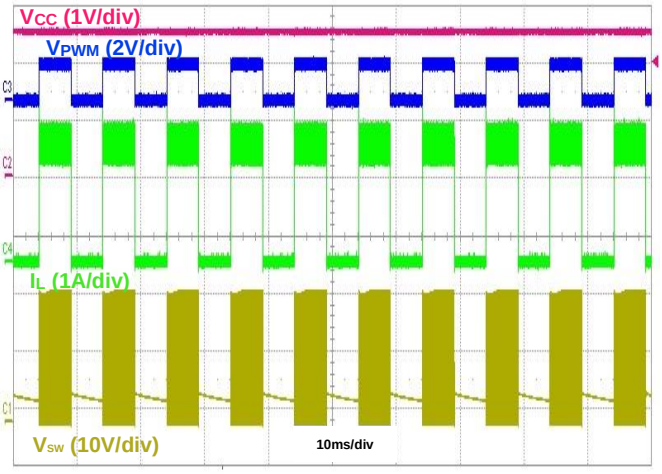


Figure 28. PWM Dimming, 100Hz, 50% Duty Cycle

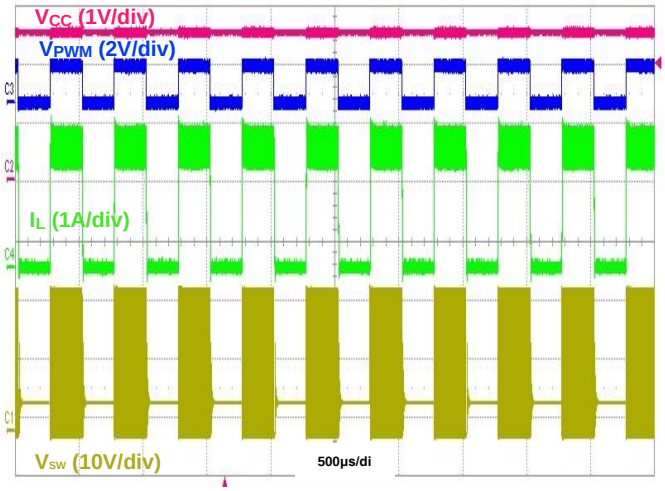


Figure 29. PWM Dimming, 2kHz, 50% Duty Cycle

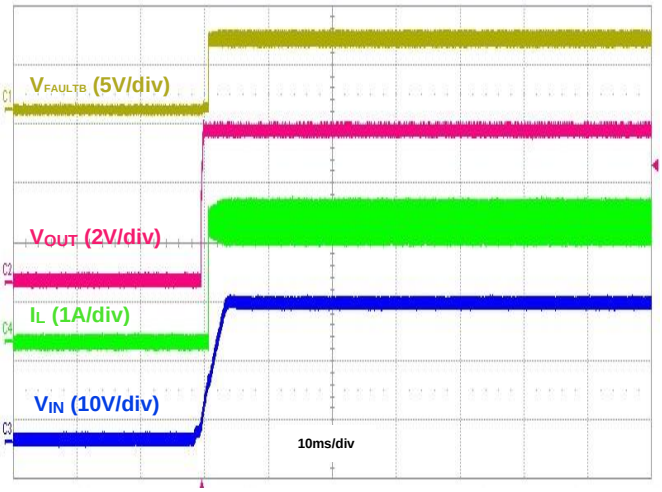


Figure 30. Startup through VIN

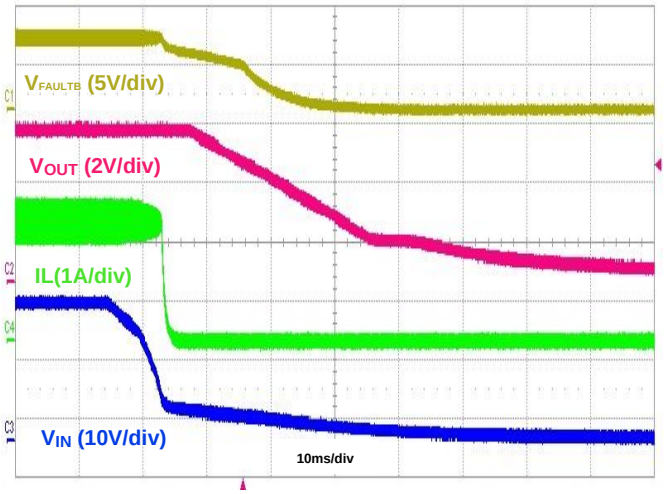


Figure 31. Shutdown through VIN, V_{FDSET} = 0V

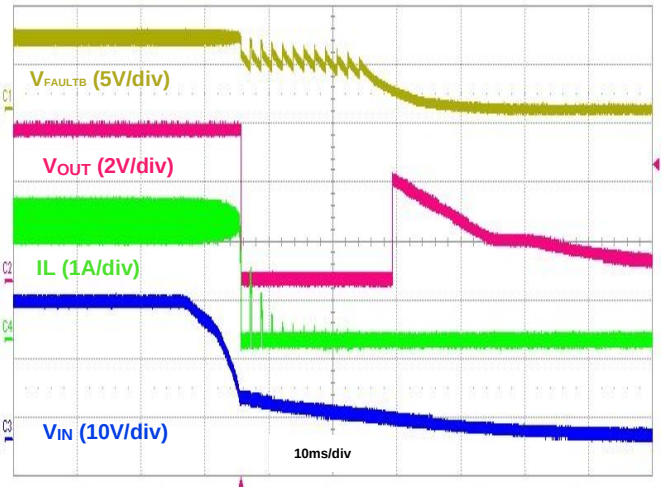


Figure 32. Shutdown through VIN, V_{FDSET} = 5V

Typical Performance Characteristics (Test at T_A = +25°C, VIN = 24V, LOAD = 2LEDs in series, IOUT = 2A, COUT = 0.47µF, f_{SW} = 400kHz, unless otherwise specified.)

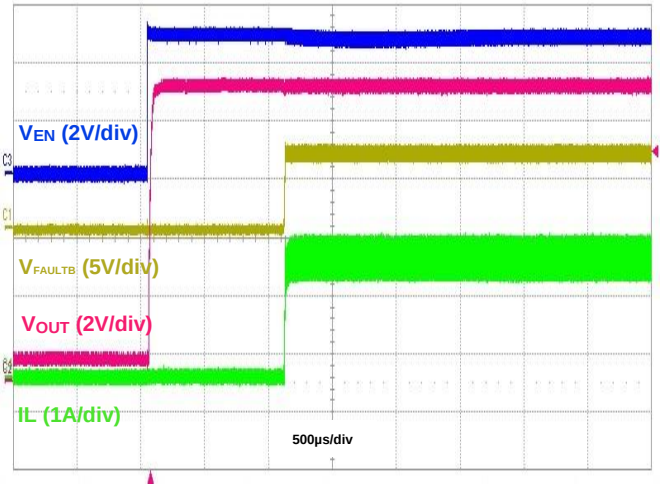


Figure 33. Start through EN

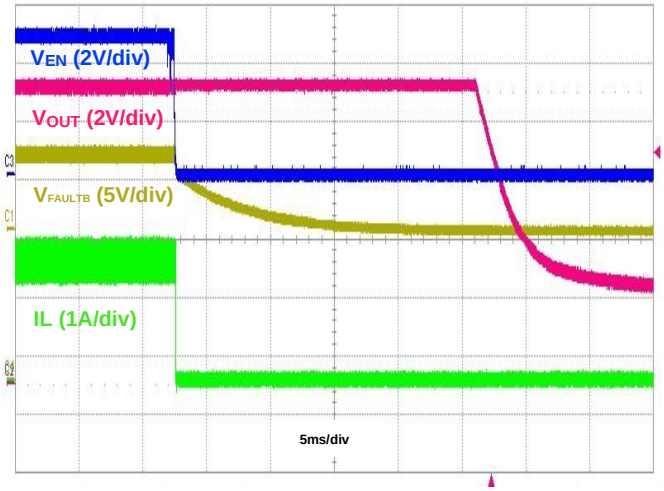


Figure 34. Shutdown through EN

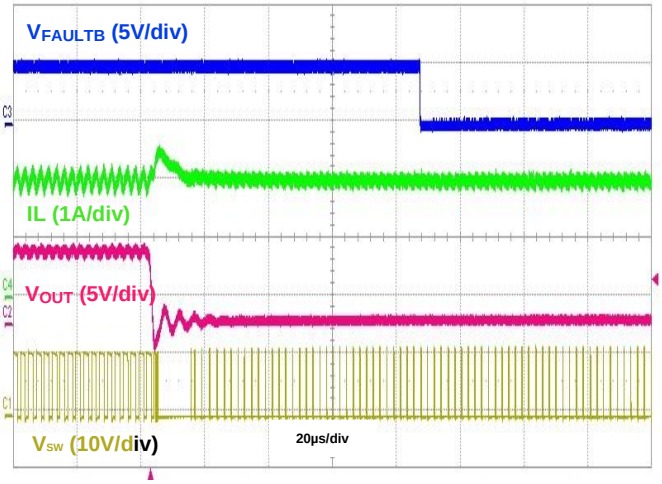


Figure 35. LED+ Short to LED- Entry, VIN = 12V

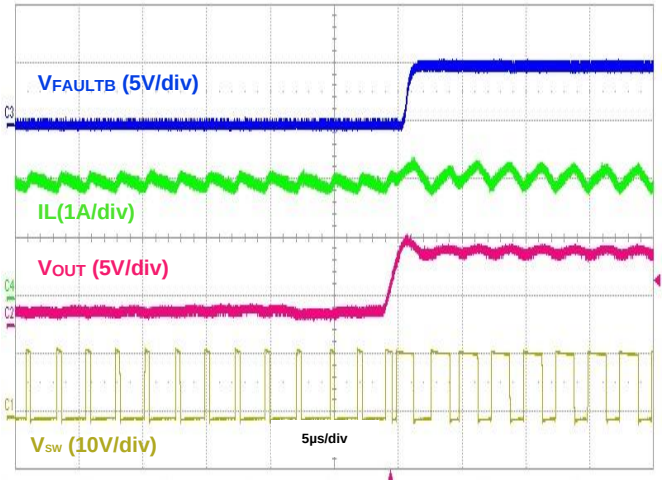


Figure 36. LED+ Short to LED- Recovery, VIN = 12V

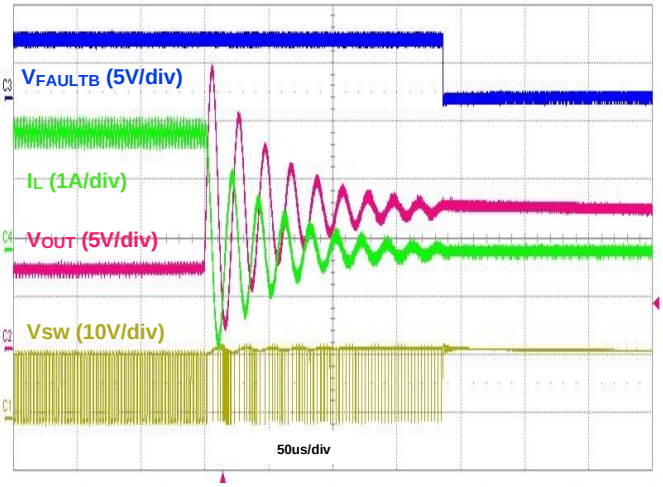


Figure 37. LED Open Entry, VIN = 12V

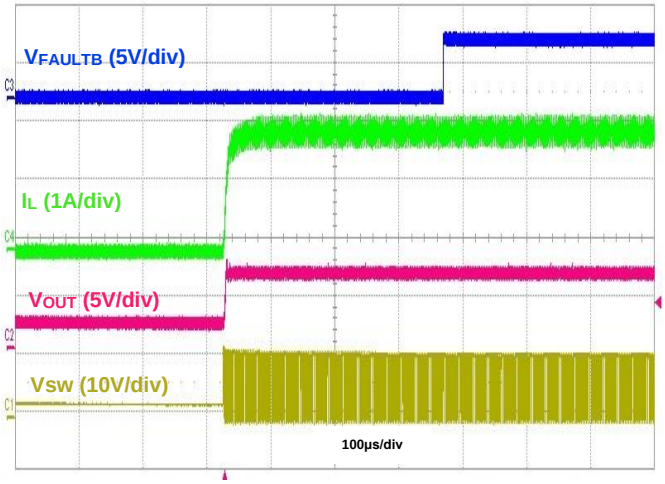


Figure 38. LED Open Recovery, VIN = 12V

Functional Description

Overview

The AL8891Q regulator is an easy-to-use, high-efficiency, compact, synchronous step-down LED driver capable of driving up to 2A of load current from an input voltage ranging from 4.5V to 65V. The switching frequency is adjustable from 200kHz to 2.5MHz by an external resistor.

Constant on time control is employed to achieve simple control-loop compensation and cycle-by-cycle current limiting. Internal compensation makes the AL8891Q require few external components.

Optional features such as programmable switching frequency, Power Good flag, internal soft-start, and multiple dimming methods provide a flexible and easy-to-use platform for a wide range of applications. Protection features include thermal shutdown, VIN and VCC undervoltage lockout, cycle-by-cycle current limit, output short-circuit protection, LED open and short detection, and external components open and short protection.

Switching Frequency

An adaptive on-time average current mode control is implemented to provide near constant switching frequency which can be set between 200kHz and 2.5MHz. The frequency is programmed using an external resistor R_{ON} connected between the FREQ pin and ground, thus the switching frequency is adjusted. t_{ON} is given by the following equation:

$$t_{ON} = k \times (R_{ON} + R_{INT}) \times (V_{OUT}/V_{IN}) \quad \text{Equation 1}$$

$$f_{SW} = 1 / [k \times (R_{ON} + R_{INT})] \quad \text{Equation } 2$$

Where k = 0.0103, with f_{SW} in MHz, t_{ON} in μs, R_{ON} and R_{INT} in kΩ. R_{INT} is an internal resistor 3kΩ

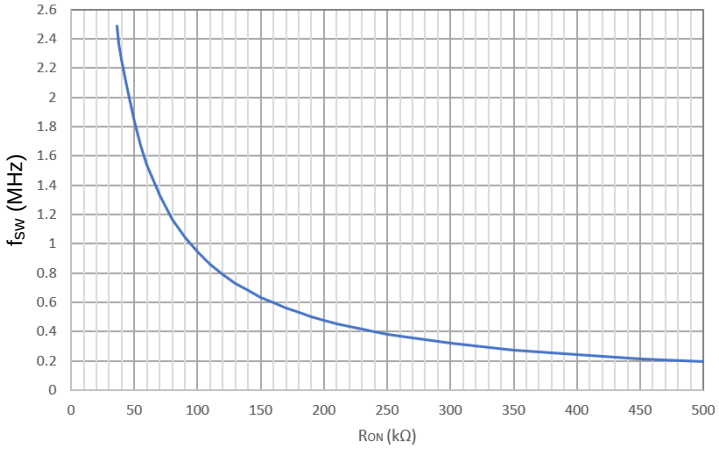


Figure 39. f_{SW} vs. R_{ON}

Enable (EN)

Enable (EN) is a digital control pin that turns the converter on and off. The AL8891Q is activated when a logic high signal is applied to the EN pin and VIN is above UVLO threshold. The device delivers desired LED current set by RCS when PDIM is high. EN pin should not be open circuit or floating.

PWM Dimming (PDIM) Control

PWM dimming can be achieved by PDIM pin or EN pin. By sending a PWM signal to PDIM pin or EN pin, the average LED current is proportional to the duty cycle of the applied PWM signal. The dimming frequency between 100Hz and 2kHz is recommended. By selecting a PWM frequency 100Hz, a dimming ratio of 0.1% can be achieved. The average LED current during dimming can be calculated as the following equation:

$$ILED\_AVG = PWM\ duty\ cycle \times ILED\_setting \quad \text{Equation 3}$$

Note that when EN dimming is applied, a pulse width greater than 200μs is necessary to activate the device during startup.

When the EN pin is toggled from high to low, the output is turned off immediately, but VCC will keep on for time $t_{EN\_OFF\_DELAY}$ and the device will stay in standby mode during this period. After that VCC will turn off, and the device will shut down completely.

Functional Description (continued)

Analog Dimming (ADIM) Control

The AL8891Q can also achieve analog dimming by applying an analog voltage on ADIM pin. When V_{ADIM} is higher than 2.0V, the LED current is at 100% level which is defined by sense resistor R_{CS}. When V_{ADIM} is between 2V and 0.15V, the LED current decreases linearly down from 100% to 7.5% level. The LED current is internally clamped to 7.5% level when V_{ADIM} is lower than 0.15V. The analog dimming feature is shown as below.

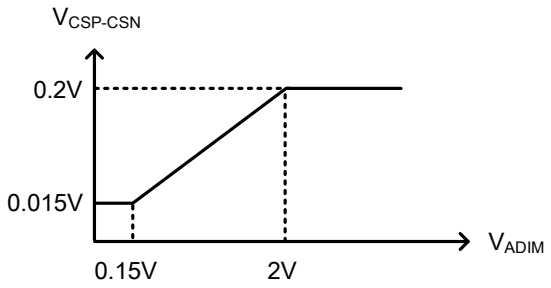


Figure 40. $V_{CSP-CSN}$ vs. V_{ADIM}

Then the LED current can be calculated as the following equation, the LED current can be programmed by sense resistor R_{CS}.

$$I_{LED\_AVG} = V_{CSP\text{-}CSN}/R_{CS} \qquad \text{Equation 4}$$

VCC, and UVLO

The AL8891Q integrates an internal LDO to generate V_{CC} for control circuitry and MOSFET drivers. The nominal voltage for V_{CC} is 5V (typical). The VCC pin is the output of the LDO. A high-quality ceramic capacitor is recommended to be placed as close as possible to VCC pin. The VCC output pin must not be loaded during operation.

Undervoltage lockout (UVLO) protects the chip from operating at an insufficient supply voltage. It monitors the VCC voltage. When the voltage is lower than UVLO threshold voltage, the device is shut down. The UVLO rising threshold is about 3.6V (typical), while its falling threshold is 3.45V (typical).

Bootstrap Voltage (CBOOT)

A voltage higher than VIN is required to drive the HS power MOSFET. The capacitor connected between CBOOT and SW pins works as a charge pump to boost voltage on the CBOOT pin to (V_{SW} + V_{CC}) through internally integrated diode. A ceramic capacitor of 0.47μF/6.3V or higher value for CBOOT is recommended.

Functional Information – Fault and Protections

The AL8891Q provides full protection functions, including cycle-by-cycle peak and valley current clamp, LED short and open protection, inductor short and open protection, RCS short protection (overcurrent), LED+ short to battery protection, FREQ pin short and open protection, and thermal shutdown. The following table summarizes all fault functions.

Fault	Detection	Fault Flag	Fault Delay	Fault Mode	Output
LED+ short to LED-	CSN-PGND < 1.6V	Yes	t_{FDG}	No action to driver	Running
LED open	FDSET > threshold & low LED current, no-fault- reporting if ADIM < 0.4V.	Yes	t_{MASK_DET}	Hiccup mode	Stop
LED+ short to battery	Same as LED open	Yes	t_{MASK_DET}	Hiccup mode	Stop
Inductor open	Same as LED open	Yes	t_{MASK_DET}	Hiccup mode	Stop
Inductor short	Trigger peak current limit for 9 cycles then latch. Toggle EN can exit latch after fault removal.	Yes	0µs	Latchoff	Stop
R_{CS} short	FDSET > threshold & overcurrent, no-fault- reporting if ADIM < 0.4V.	Yes	t_{MASK_DET}	Hiccup mode	Stop
Overcurrent	Trigger peak current limit for 9 cycles then latch.	Yes	0µs	Latchoff	Stop
FREQ pin open	External resistor open circuit detected for TON pin after VCC power-up	Yes	0µs	Latchoff	Stop
FREQ pin short	External resistor short circuit detected for TON pin after VCC power-up.	Yes	0µs	Latchoff	Stop
Overtemperature	T_J > Thermal shutdown threshold	Yes	0µs	Shutdown and auto recovery	Stop

LED+ Short to LED-

When output short fault occurred and CSN-PGND < 1.6V, including LED+ short to LED- or output capacitor short or any other event resulting in output short, the fault is detected, and FAULT pin is set to low level after deglitch time t_{FDT}. But the converter will work continuously and output nominal current. When the output short fault is removed and CSN-PGND > 1.8V, FAULT is set to high level immediately and the converter returns to normal work.

LED Open

The LED open fault is masked when FDSET pin voltage is lower than V_{FDSET}, that is to avoid misreporting LED open faults during VIN startup. To achieve the mask function, connect a voltage divider between VIN and GND, and connect the center of the divider to FDSET pin.

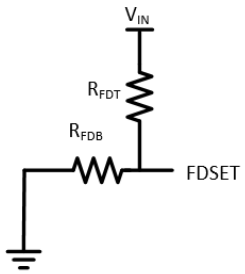


Figure 41. Set VIN Threshold to Mask LED Open Fault

Functional Information – Fault and Protections (continued)

The VIN rising threshold that enables LED open fault detection can be determined by:

$$V_{IN-RISING} = (1+R_{FDT} / R_{FDB}) \times V_{FDSET} \quad \text{Equation 5}$$

In addition, no LED open fault reporting if ADIM < 0.4V. So, only FDSET > threshold and ADIM > 0.4V are met, the LED open fault is reported, and the converter enter hiccup mode after mask time $t_{MASK-DET}$. When LED open is removed, the converter returns to normal operation when a hiccup period ended. $\overline{FAULT}$ pin is set to high level after mask time $t_{MASK-REL}$. The cool down time of hiccup mode is t_{RETRY}.

Note that FDSET is a high-impedance input pin and should not be left floating. If LED open detection is not required, tie the FDSET pin to GND. Or tie the FDSET pin to VCC then LED Open fault is never masked.

For inductor open and LED+ short to Battery fault, the detection and recovery is same as LED open fault.

RCS Short

When RCS short occurs and the peak current does not reach peak current limit $I_{PEAK-LIMIT}$, the converter will enter hiccup mode after mask time $t_{MASK-DET}$ and $\overline{FAULT}$ is set to low level. When RCS short is removed, the converter returns to normal operation: 1) when a hiccup period ended, and $\overline{FAULT}$ pin is set to high level after mask time $t_{MASK-REL}$; 2) FDSET > threshold and ADIM > 0.4V.

Inductor Short and Overcurrent Protection

When inductor short occurs, the current of internal power MOSFET will ramp up until it hits peak current limit $I_{PEAK-LIMIT}$. After triggering peak current limit for 9 cycles the converter latches off immediately and FAULT is set to low level. Toggling EN can exit latch after inductor short fault is removed.

Besides inductor short, if there is any other reason that results in the current of internal power MOSFET triggering peak current limit for 9 cycles, the converter will latch off.

FREQ Pin Fault

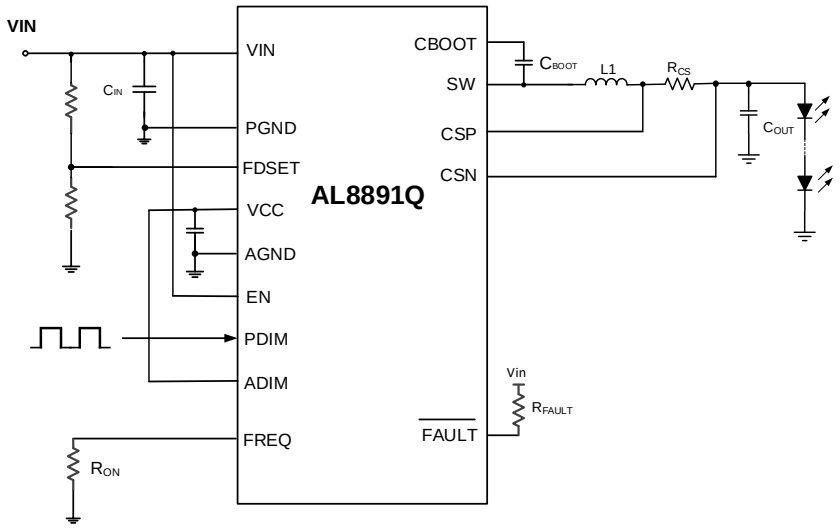
There is FREQ pin short and open detection after each VCC power-up. Make sure the FREQ pin is properly connected to a resistor to avoid triggering pin short or open fault. After fault is detected, the converter latches off immediately and FAULT pin is set to low level. The fault is latched until next VCC power-up.

Overtemperature Protection

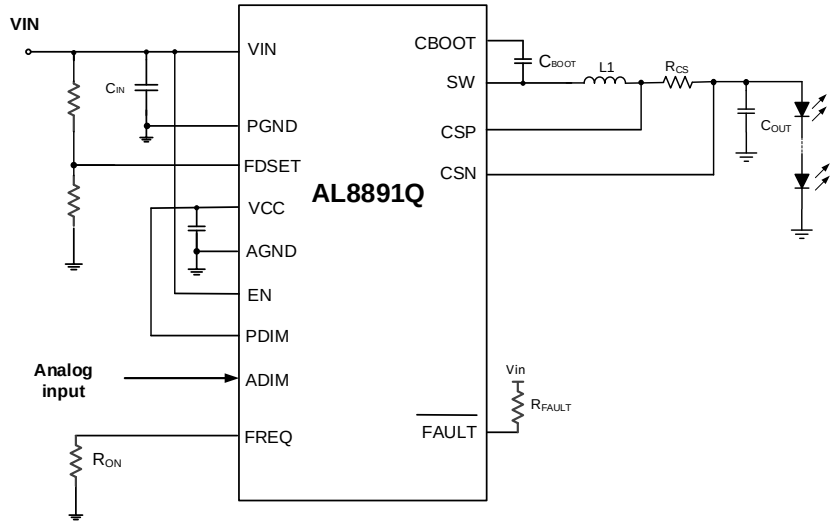
When the junction temperature exceeds T_{SD}, the AL8891Q shuts down the switching regulator to reduce thermal dissipation. It automatically restarts the switching regulator after junction temperature drops back below T_{SD}-$T_{SD(HYS)}$. The VCC LDO regulators remain operational during overtemperature event.

Typical Application Information

1) PWM Dimming Application Diagram

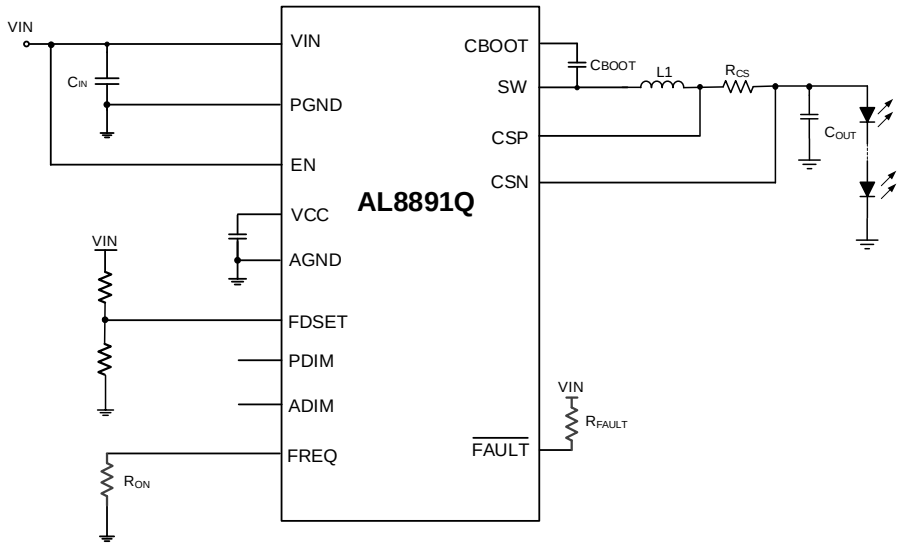


2) Analog Dimming Application Diagram

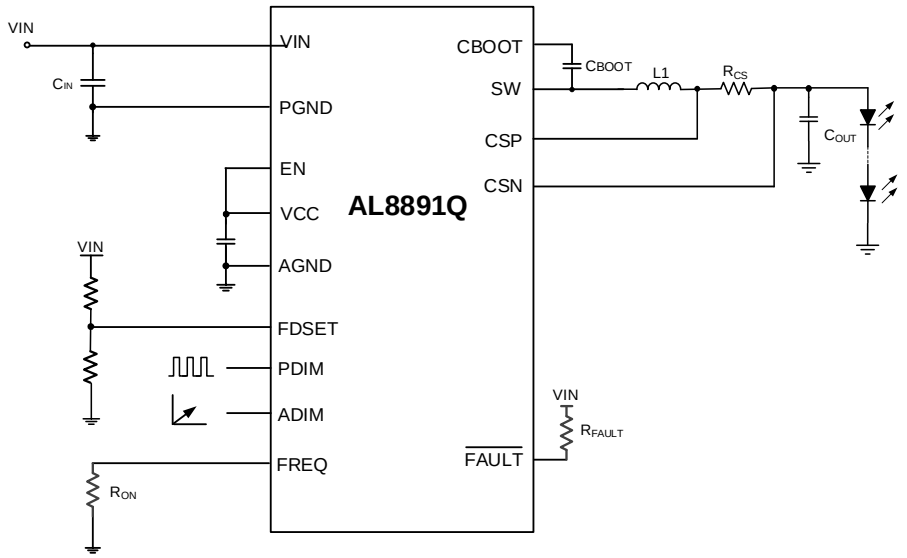


Typical Application Information (continued)

3) EN Pin to VIN Dimming Application Diagram



4) PDIM and ADIM Both Pins Dimming Application Diagram



Typical Application Information (continued)

5) Output Capacitor Calculation

The output capacitor value depends on the total series resistance of the LED string, r_LED, and the switching frequency, f_sw. The capacitance required for the target LED ripple current, Δi_LED, is calculated using Equation below.

$$C_{OUT} = \frac{\Delta i_{L\_max}}{8 \times f_{sw} \times r_{LED} \times \Delta i_{LED}}$$

Where

$\Delta i\_(L\_max)$ maximum ripple current of power inductor in worst case
f_sw switching frequency
r_LED equivalent resistance of total LED string
Δi_LED target ripple current of LED string

When choosing the output capacitors, consider the ESR and ESL characteristics because they directly impact the LED current ripple. Ceramic capacitors are the best choice due to the following:

- Low ESR
- High ripple current rating
- Long lifetime
- Good temperature performance

With ceramic capacitor technology, consider the derating factors associated with higher temperature and DC bias operating conditions. It is recommend to use an X7R dielectric with a voltage rating greater than the maximum LED stack voltage.

6) Input Capacitor Calculation

The input capacitor buffers the input voltage for transient events and decouples the converter from the supply. It is recommended to use a 10µF input capacitor across the VIN pin and PGND placed close to the device and connected using wide traces. X7R-rated ceramic capacitors are the best choice due to the low ESR, high ripple current rating, and good temperature performance.

In addition, a small case size 100nF ceramic capacitor must be used across VIN to PGND, immediately adjacent to the device. This usage provides a high-frequency bypass for the control circuits internal to the device. These capacitors also suppress SW node ringing, which reduces the maximum voltage present on the SW node and EMI.

The capacitance can be increased to further limit the input voltage deviation during PWM dimming operation.

Typical Application Information (continued)

7) Layout

The performance of any switching converter depends as much upon the layout of the PCB as the component selection. The AL8891Q is designed to meet the optimization requirements of PCB layout in the pin assignment. For example, VIN and GND pins are adjacent to each other, which is convenient for placing VIN bypass capacitors.

Radiated EMI is generated by the high di/dt components in pulsing currents in switching converters. The larger area covered by the path of a pulsing current, the more electromagnetic emission is generated. The key to minimize radiated EMI is to minimize the area of the pulsing current path, thus, placing high frequency ceramic bypass capacitor(s) as close as possible to the VIN and GND pins is necessary.

In addition, high dv/dt occurs on SW node during switching, so the trace between SW pin and inductor should be as short as possible, and just wide enough to carry the load current without excessive heating. Short and thick traces are highly recommended to minimize parasitic resistance. Besides, sensitive signal lines should be kept away from SW traces.

The following guidelines are provided to help users design a PCB with the best power conversion performance, thermal performance, and minimized generation of unwanted EMI.

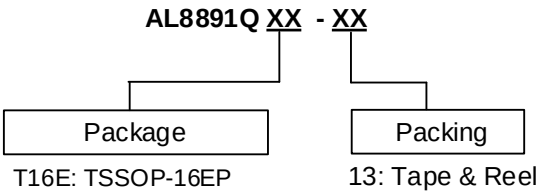
1. Place high-frequency ceramic bypass CIN as close as possible to VIN and GND pins; a ceramic capacitor in small package (such as 0603) is still needed even if multiple input capacitors are implemented.
2. The high-current loop consisting of VIN, VOUT and PGND should be as compact as possible.
3. The bypass capacitors of VCC should be arranged close to the VCC pin and return to the PGND pin with the shortest connection.
4. It is recommended to use a four-layer board with 2oz top and bottom layers, and a dedicate ground plane on middle layer. Use a minimum 3 by 4 arrays of 10 mil thermal VIAs to connect the thermal pad to the system ground plane for heat dissipation purpose.
5. The SW and CBOOT nodes contain a lot of high-frequency noise, so the connection of these pins should be as short as possible, meanwhile, there should be sufficient width to conduct the current.
6. Sensitive analog signals, such as CSP and CSN need to be far away from the noisy nodes, and ground plane can be used as a shielding layer while routing these sensitive signals.
7. The resistor for FREQ pin R_{ON} must be located as close to the pin as possible.

Design Tools (Note 9)

- AL8891Q Demo Board
- Demo Board Gerber File for PCB Layout Reference

Note: 9. Diodes Incorporated's design tools can be found on our website at https://www.diodes.com/design/tools/.

Ordering Information (Note 10)



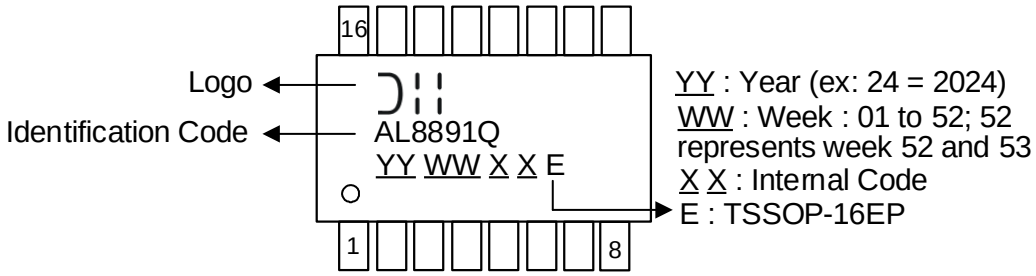
Orderable Part Number	Package Code	Package	Packing	
			Qty.	Carrier
AL8891QT16E-13	T16E	TSSOP-16EP	2500	Tape & Reel

Note: 10. For packaging details, go to our website at https://www.diodes.com/design/support/packaging/diodes-packaging/.

Marking Information

TSSOP-16EP

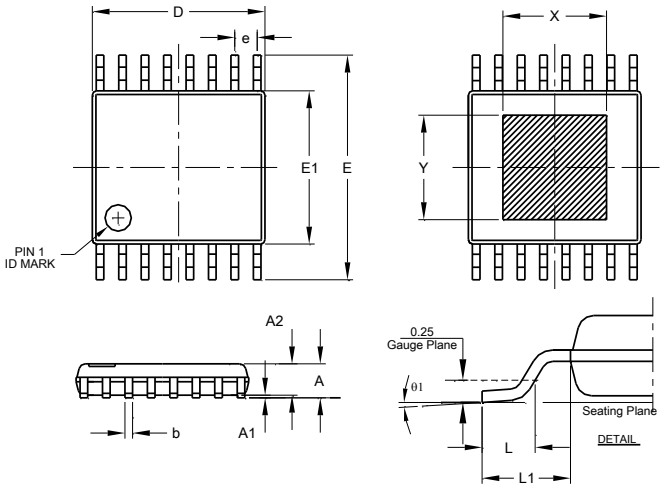
(Top View – Not to Scale)



Package Outline Dimensions

Please see http://www.diodes.com/package-outlines.html for the latest version.

TSSOP-16EP

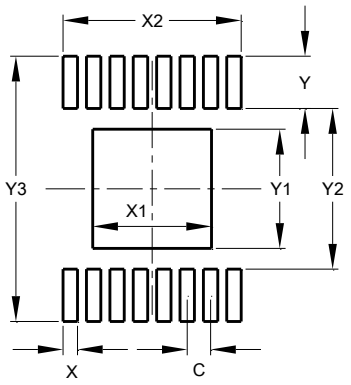


TSSOP-16EP			
Dim	**Min**	**Max**	**Typ**
A	-	1.20	-
A1	0.025	0.100	-
A2	0.80	1.05	0.90
b	0.19	0.30	-
c	0.09	0.20	-
D	4.90	5.10	5.00
E	6.20	6.60	6.40
E1	4.30	4.50	4.40
e	0.65 BSC		
L	0.45	0.75	0.60
L1	1.0 REF		
L2	0.65 BSC		
X	-	-	2.997
Y	-	-	2.997
θ1	0°	8°	-
All Dimensions in mm			

Suggested Pad Layout

Please see http://www.diodes.com/package-outlines.html for the latest version.

TSSOP-16EP



Dimensions	Value (in mm)
C	0.650
X	0.450
X1	3.290
X2	5.000
Y	1.450
Y1	3.290
Y2	4.450
Y3	7.350

Mechanical Data

- Moisture Sensitivity: Level 1 per JESD22-A113
- Terminals: Finish – Matte Tin Plated Leads, Solderable per M2003 JESD22-B102 e3
- Weight: 0.055 grams (Approximate)

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