USB TYPE-C DFP CONTROLLER AND POWER SWITCH WITH LOAD DETECTION

Description

The AP25810LQ device is a USB Type-C® downstream-facing port (DFP) controller with an integrated 3A rated USB power switch. The AP25810LQ device monitors the USB Type-C configuration channel (CC) lines to determine when a USB device is attached. If an upstream-facing port (UFP) device is attached, the AP25810LQ applies power to the V_{BUS} and communicates the selectable V_{BUS} current-sourcing capability to the UFP via the pass-through CC line. If the UFP is attached using an electronically marked cable, the AP25810LQ also applies V_{CONN} power to the cable CC pin. The device also identifies when USB Type-C audio or debug accessories are attached.

The AP25810LQ draws less than 0.7µA (typ) when no device is attached. Additional system power saving is achievable in the S4 and S5 system power states by using the $\overline{UFP}$ output to disable the high-power 5V supply when no UFP is attached. In this mode, the device is capable of running from an auxiliary supply (AUX), which can be a lower-voltage supply (3.3V), typically powering the system µC in low-power states (S4 and S5).

The AP25810LQ 30mΩ power switch has two selectable fixed-current limits that align with the Type-C current levels. The $\overline{FAULT}$ output signals when the switch is in an overcurrent or overtemperature condition. The $\overline{LD\_DET}$ output controls power management to multiple high-current Type-C ports in an environment where all ports cannot simultaneously provide high current (3A).

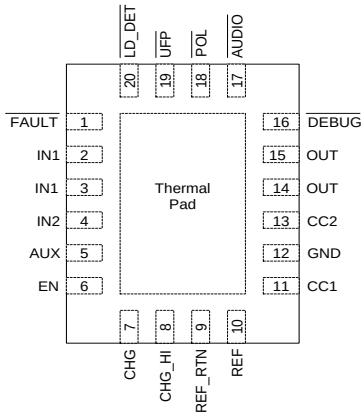
The AP25810LQ is available in a standard Green W-QFN3040-20 (Type A1) package with exposed pad for improved thermal performance and is RoHS-compliant.

Applications

- USB Type-C host ports in notebook computers for sleep charging
- LCD monitor/docking stations and charging cradles
- USB Type-C wall chargers

Pin Assignments

(Top View)



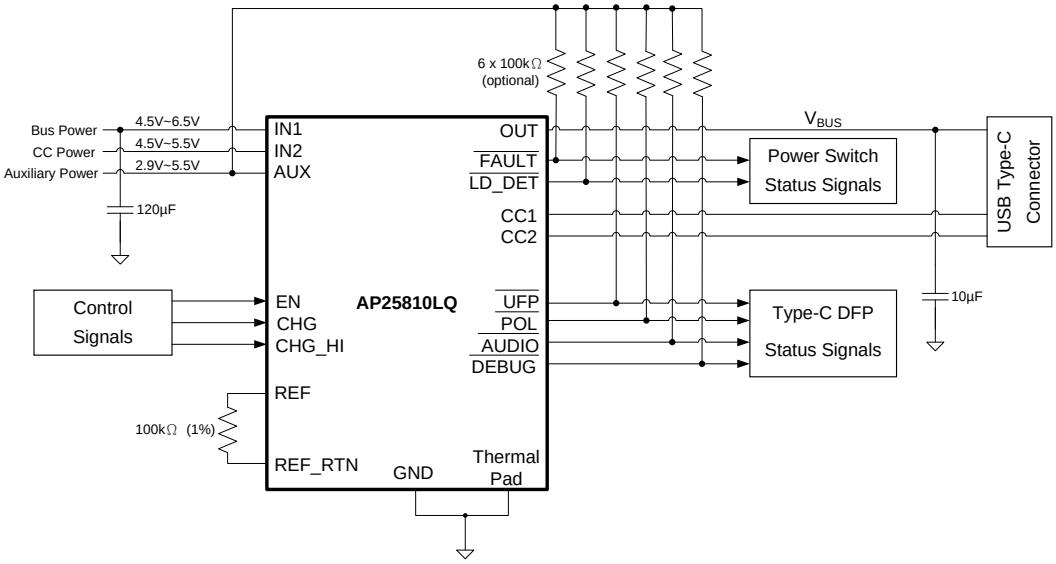
W-QFN3040-20 (Type A1)

Features

- AEC Qualified to AEC-Q100 Grade 1 Offering -40°C to +125°C
- USB Type-C Rev. 2.0 Compliant DFP Controller
- Connector Attach or Detach Detection
- STD, 1.5A or 3A Capability Advertisement on CC
- Super-Speed Polarity Determination
- V_{BUS} Application and Discharge
- V_{CONN} Application to Electronically Marked Cable
- Audio and Debug Accessory Identification
- 0.7µA (typ) IDDQ When Port Is Unattached
- Three Input Supply Options
  - IN1: USB Charging Supply
  - IN2: V_{CONN} Supply
  - AUX: Device Power Supply
- Power Wake Supports Low Power in System Hibernate (S4) and OFF (S5) Power States
- 30mΩ (typ) High-Side MOSFET
- Programmable 1.7A or 3.4A ILIM (±7.1%)
- Port Power Management Enables Power Resource Optimization Across Multiple Ports
- Transient Protection for CC1/CC2 Lines:
  - IEC 61000-4-2 Contact Discharge ±8kV
  - IEC 61000-4-2 Air Gap Discharge ±15kV
- Thermally Efficient Low-Profile Package
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**
- **The AP25810LQ is suitable for automotive applications requiring specific change control; this part is AEC-Q100 qualified, PPAP capable, and manufactured in IATF 16949 certified facilities.**
  https://www.diodes.com/quality/product-definitions/

Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

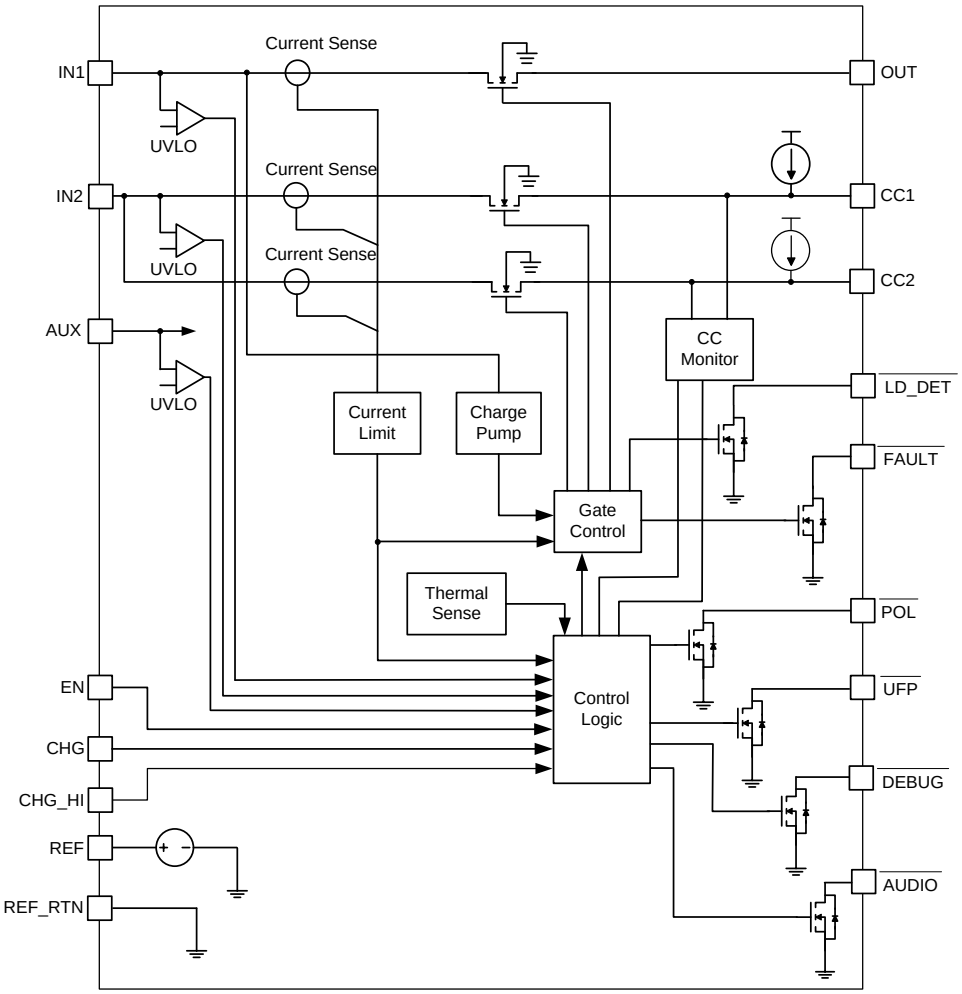
Typical Applications Circuit



Pin Descriptions

Pin Number	Pin Name	I/O	Pin Function
1	$\overline{\text{FAULT}}$	O	Fault event indicator. Open-drain logic output that asserts low to indicate a current-limit or thermal shutdown event due to overtemperature.
2, 3	IN1	I	V_{BUS} input supply. Internal power switch connects IN1 to OUT.
4	IN2	I	V_{CONN} input supply. Internal power switch connects IN2 to CC1 or CC2. Short to IN1 if only one supply is used.
5	AUX	I	Auxiliary input supply. Connect to an always-alive system rail to use the power-wake feature. Short to IN1 and IN2 if only one supply is used.
6	EN	I	Enable logic input. Turns the device on and off.
7	CHG	I	Charge-logic input to select between standard USB (500mA for a Type-C receptacle supporting only USB 2.0, and 900mA for Type-C receptacle supporting USB 3.1) or a Type-C current-sourcing ability.
8	CHG_HI	I	High-charge logic input to select between 1.5A and 3A Type-C current sourcing capability. Valid when CHG is set to Type-C current.
9	REF_RTN	I	Precision signal-reference return. Connect to the REF pin via a 100kΩ, 1% resistor.
10	REF	I	Analog input used to generate the internal current reference. Connect a 1% or better, 100ppm, 100kΩ resistor between this pin and REF_RTN.
11	CC1	I/O	Analog input/output that connects to the Type-C receptacle CC1 pin.
12	GND	—	Power ground
13	CC2	I/O	Analog input/output that connects to the Type-C receptacle CC2 pin.
14, 15	OUT	O	Power switch output
16	$\overline{\text{DEBUG}}$	O	Open-drain logic output that asserts when a Type-C debug accessory is identified on the CC lines.
17	$\overline{\text{AUDIO}}$	O	Open-drain logic output that asserts when a Type-C audio accessory is identified on the CC lines.
18	$\overline{\text{POL}}$	O	Polarity open-drain logic output that signals which Type-C CC pin is connected to the CC line. This gives the information needed to multiplex the super-speed lines. Asserted when the CC2 pin is connected to the CC line in the cable.
19	$\overline{\text{UFP}}$	O	Open-drain logic output that asserts when a Type-C UFP is identified on the CC lines.
20	$\overline{\text{LD\_DET}}$	O	Load-detect open-drain logic output that signals when a device set to source Type-C 3A current is sourcing over 1.95A, nominal.
—	Thermal Pad	—	Thermal pad on the bottom of the package. The thermal pad is internally connected to GND and is used to heat-sink the device to the circuit board. Connect the thermal pad to the GND plane.

Functional Block Diagram



Absolute Maximum Ratings (@ T_A = +25°C, unless otherwise specified.) (Note 4)

Symbol		Parameter		Ratings	Unit
ESD	HBM	Human body model ESD protection		±2	kV
	CDM	Charged device model ESD protection		±750	V
	IEC system level	IEC 61000-4-2. Contact discharge, CC1/CC2 (Note 5)		±8	kV
	IEC system level	IEC 61000-4-2. Air gap discharge, CC1/CC2 (Note 5)		±15	kV
Pin voltage, V		IN1, IN2, AUX, EN, CHG, CHG_HI, REF, $\overline{\text{LD\_DET}}$, $\overline{\text{FAULT}}$, $\overline{\text{UFP}}$, $\overline{\text{POL}}$, $\overline{\text{AUDIO}}$, $\overline{\text{DEBUG}}$, OUT, CC1 & CC2		-0.3 to +7	V
		REF_RTN		Internally connected to GND	V
Pin positive source current, I_{SRC}		OUT, REF, CC1, CC2		Internally limited	A
Pin positive sink current, I_{SNK}		OUT (while applying V_{BUS})		5	A
		CC1, CC2 (while applying V_{CONN})		1	A
		$\overline{\text{LD\_DET}}$, $\overline{\text{FAULT}}$, $\overline{\text{UFP}}$, $\overline{\text{POL}}$, $\overline{\text{AUDIO}}$, $\overline{\text{DEBUG}}$		Internally limited	mA
$R_{\theta JA}$		Thermal resistance, junction to ambient (Note 6)	W-QFN3040-20 (Type A1)	40	°C/W
$R_{\theta JC}$		Thermal resistance, junction to case (Note 6)	W-QFN3040-20 (Type A1)	5	°C/W
$T_{J(max)}$		Maximum junction temperature		+180	°C
T_{ST}		Storage temperature		-65 to +150	°C

Notes: 4. Stresses greater than those listed under *Absolute Maximum Ratings* can cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to *Absolute Maximum Ratings* for extended periods can affect device reliability.

5. EVM have been tested per typical circuit with capacitors connected to the V_{IN} and V_{OUT}.

6. $R_{\theta JA}$ and $R_{\theta JC}$ are measured at T_A = +25°C on a high effective thermal conductivity four-layer test board per JEDEC 51-7.

Recommended Operating Conditions (Note 7)

Symbol	Parameter		Min	Max	Unit
V_{IN}	Supply voltage	IN1	4.5	6.5	V
		IN2	4.5	5.5	V
		AUX	2.9	5.5	V
V_{OUT}	Output voltage	OUT	0	6.5	V
V_I	Input voltage	EN, CHG, CHG_HI	0	5.5	V
V_{IH}	High-level input voltage	EN, CHG, CHG_HI	1.17	—	V
V_{IL}	Low-level voltage	EN, CHG, CHG_HI	—	0.58	V
V_{PU}	Pullup voltage	Used on $\overline{\text{LD\_DET}}$, $\overline{\text{FAULT}}$, $\overline{\text{UFP}}$, $\overline{\text{POL}}$, $\overline{\text{AUDIO}}$, $\overline{\text{DEBUG}}$	0	5.5	V
I_{SRC}	Positive source current	OUT	—	3	A
		CC1 or CC2 when supplying V_{CONN}	—	350	mA
I_{SNK}	Positive sink current (10ms moving average)	$\overline{\text{LD\_DET}}$, $\overline{\text{FAULT}}$, $\overline{\text{UFP}}$, $\overline{\text{POL}}$, $\overline{\text{AUDIO}}$, $\overline{\text{DEBUG}}$	—	10	mA
I_{SNK_PULSE}	Positive repetitive pulse sink current	$\overline{\text{LD\_DET}}$, $\overline{\text{FAULT}}$, $\overline{\text{UFP}}$, $\overline{\text{POL}}$, $\overline{\text{AUDIO}}$, $\overline{\text{DEBUG}}$	—	Internally limit	mA
R_{REF}	Reference resistor		98	102	kΩ
T_A	Operating ambient temperature		-40	+125	°C

Note: 7. Refer to the *Typical Application Circuit*.

Electrical Characteristics

(-40°C ≤ T_J ≤ +125°C, 4.5V ≤ V_{IN1} ≤ 6.5V, 4.5V ≤ V_{IN2} ≤ 5.5V, 2.9V ≤ V_{AUX} ≤ 5.5V; V_{EN} = V_{CHG} = V_{CHG_HI} = V_{AUX}, R_{REF} = 100kΩ. Typical values are at +25°C. All voltages are with respect to GND. I_{OUT} and I_{OS} defined positive out of the indicated pin, unless otherwise specified.)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
OUT – POWER SWITCH						
$R_{DS(ON)}$	On-resistance (Note 8)	T_J = +25°C, I_{OUT} = 3A	—	30	37	mΩ
		-40°C ≤ T_J ≤ +85°C, I_{OUT} = 3A	—	30	46	
		-40°C ≤ T_J ≤ +125°C, I_{OUT} = 3A	—	30	55	
I_{REV}	OUT to IN reverse leakage current	V_{OUT} = 6.5V, V_{IN1} = V_{EN} = 0V -40°C ≤ T_J ≤ +85°C, I_{REV} is current out of IN1 pin	—	0	3	μA
OUT – CURRENT LIMIT						
I_{OS}	Short-circuit current limit (Notes 8 & 9)	V_{CHG} = 0V or V_{CHG} = V_{AUX} and V_{CHG_HI} = 0V	1.58	1.7	1.9	A
		V_{CHG} = V_{AUX} and V_{CHG_HI} = V_{AUX} (Note 9)	3.16	3.4	3.8	
		R_{REF} = 10Ω (Note 9)	—	—	7	
OUT – DISCHARGE						
R_{DIS}	Discharge resistance	V_{OUT} = 4V, UFP signature removed from CC lines, time < t_{w_DCHG}	10	20	60	Ω
R_{BDIS}	Bleed discharge resistance	V_{OUT} = 4V, No UFP signature on CC lines, time > t_{w_DCHG}	100	150	250	kΩ
REF						
V_O	Output voltage	—	0.78	0.8	0.82	V
I_{OS}	Short-circuit current (Note 9)	R_{REF} = 10Ω	9.5	—	15.3	μA
$\overline{FAULT}$						
V_{OL}	Output low voltage	$I_{\overline{FAULT}}$ = 1mA	—	—	350	mV
I_{OFF}	Off-state leakage	$V_{\overline{FAULT}}$ = 5.5V	—	—	1	μA
$\overline{LD\_DET}$						
V_{OL}	Output low voltage	$I_{\overline{LD\_DET}}$ = 1mA	—	—	350	mV
I_{OFF}	Off-state leakage	$V_{\overline{LD\_DET}}$ = 5.5V	—	—	1	μA
I_{TH}	OUT sourcing, rising threshold current for load detect (Note 9)	—	1.8	1.95	2.25	A
—	Hysteresis (Note 9)	—	—	125	—	mA
CC1, CC2 – V_{CONN} POWER SWITCH						
$R_{DS(ON)}$	On-resistance	T_J = +25°C, I_{OUT} = 250mA	—	365	420	mΩ
		-40°C ≤ T_J ≤ +85°C, I_{OUT} = 250mA	—	365	530	
		-40°C ≤ T_J ≤ +125°C, I_{OUT} = 250mA	—	365	600	
CC1, CC2 – V_{CONN} POWER SWITCH – CURRENT LIMIT						
I_{OS}	Short-circuit current limit (Note 9)	—	380	450	520	mA
		R_{REF} = 10Ω (Note 9)	—	—	800	
CC1, CC2 – CONNECT MANAGEMENT – DANGLING ELECTRONICALLY MARKED CABLE MODE						
I_{SRC}	Sourcing current on the pass-through CC Line	0V ≤ V_{CCx} ≤ 1.5V	64	80	96	μA
	Sourcing current on the Ra CC line	0V ≤ V_{CCx} ≤ 1.5V	64	80	96	

Notes: 8. Pulse-testing techniques maintain junction temperature close to ambient temperature; thermal effects must be taken into account separately.
9. Specification is guarantee by design.

Electrical Characteristics (continued)

(-40°C ≤ T_J ≤ +125°C, 4.5V ≤ V_{IN1} ≤ 6.5V, 4.5V ≤ V_{IN2} ≤ 5.5V, 2.9V ≤ V_{AUX} ≤ 5.5V; V_{EN} = V_{CHG} = V_{CHG_HI} = V_{AUX}, R_{REF} = 100kΩ. Typical values are at +25°C. All voltages are with respect to GND. I_{OUT} and I_{OS} defined positive out of the indicated pin, unless otherwise specified.)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
CC1, CC2 – CONNECT MANAGEMENT – ACCESSORY MODE						
I_{SRC}	CCx sourcing current (CC2 – audio, CC1-debug)	0V ≤ V_{CCx} ≤ 1.5V	64	80	96	µA
	CCx sourcing current (CC1 – audio, CC2-debug)	0V ≤ V_{CCx} ≤ 1.5V	—	0	—	
CC1, CC2 – CONNECT MANAGEMENT – UFP MODE						
I_{SRC}	Sourcing current with either IN1 or IN2 in UVLO	0V ≤ V_{CCx} ≤ 1.5V V_{IN1} < $V_{TH\_UVLO\_IN1}$ or V_{IN2} < $V_{TH\_UVLO\_IN2}$	64	80	96	µA
I_{SRC}	Sourcing current	V_{CHG} = 0V and V_{CHG_HI} = 0V 0V ≤ V_{CCx} ≤ 1.5V	75	80	85	µA
		V_{CHG} = V_{AUX} and V_{CHG_HI} = 0V 0V ≤ V_{CCx} ≤ 1.5V	170	180	190	
		V_{CHG} = V_{AUX} and V_{CHG_HI} = V_{AUX} 0V ≤ V_{CCx} ≤ 2.45V	312	330	348	
$\overline{UFP}$, $\overline{POL}$, $\overline{AUDIO}$, $\overline{DEBUG}$						
V_{OL}	Output low voltage	I_{SNK_PIN} = 1mA	—	—	250	mV
I_{OFF}	Off-state leakage	V_{PIN} = 5.5V	—	—	1	µA
EN, CHG, CHG_HI – LOGIC INPUTS						
V_{TH}	Rising threshold voltage	—	—	0.925	1.15	V
V_{TH}	Falling threshold voltage	—	0.65	0.875	—	V
—	Hysteresis	—	—	45	—	mV
I_{IN}	Input current	V_{EN} = 0V or 6.5V	-0.5	—	0.5	µA
OVERTEMPERATURE SHUTDOWN						
T_{TH_OTSD2}	Rising threshold temperature for device shutdown (Note 9)	—	+155	—	—	°C
—	Hysteresis (Note 9)	—	—	+20	—	°C
T_{TH_OTSD1}	Rising threshold temperature for OUT/ V_{CONN} switch shutdown in current limit (Note 9)	—	+135	—	—	°C
—	Hysteresis (Note 9)	—	—	+20	—	°C
IN1						
$V_{TH\_UVLO\_IN1}$	Rising threshold voltage for UVLO	—	3.9	4.1	4.3	V
—	Hysteresis	—	—	100	—	mV
$I_{IN1(DIS)}$	Disabled supply current	V_{EN} = 0V, -40°C ≤ T_J ≤ +85°C	—	—	1	µA
$I_{IN1(CC\_OPEN)}$	Enabled supply current with CC lines open	-40°C ≤ T_J ≤ +85°C	—	—	1	µA
$I_{IN1(Ra)}$	Enabled supply current with accessory or dangling electronically marked cable signature on CC lines	—	—	—	4	µA
$I_{IN1(Rd)}$	Enabled supply current with UFP attached	V_{CHG} = 0V, or V_{CHG} = V_{AUX} and V_{CHG_HI} = 0V	—	150	200	µA
		—	—	160	220	

Note: 9. Specification is guarantee by design.

Electrical Characteristics (continued)

(-40°C ≤ T_J ≤ +125°C, 4.5V ≤ V_{IN1} ≤ 6.5V, 4.5V ≤ V_{IN2} ≤ 5.5V, 2.9V ≤ V_{AUX} ≤ 5.5V; V_{EN} = V_{CHG} = V_{CHG_HI} = V_{AUX}, R_{REF} = 100kΩ. Typical values are at +25°C. All voltages are with respect to GND. I_{OUT} and I_{OS} defined positive out of the indicated pin, unless otherwise specified.)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
IN2						
$V_{TH\_UVLO\_IN2}$	Rising threshold voltage for UVLO	—	3.9	4.1	4.3	V
—	Hysteresis	—	—	100	—	mV
$I_{IN2(DIS)}$	Disabled supply current	V_{EN} = 0V, -40°C ≤ T_J ≤ +85°C	—	—	1	μA
$I_{IN2(CC\_OPEN)}$	Enabled supply current with CC lines open	-40°C ≤ T_J ≤ +85°C	—	—	1	μA
$I_{IN2(Ra)}$	Enabled supply current with accessory or dangling electronically marked cable signature on CC lines	—	—	—	4	μA
$I_{IN2(Rd)}$	Enabled supply current with UFP signature on CC lines (Includes IN current that provides the CC output current to the UFP Rd resistor)	V_{CHG} = 0V, 0V ≤ V_{CCx} ≤ 1.5V	—	120	140	μA
		V_{CHG} = V_{IN} and V_{CHG_HI} = 0V 0V ≤ V_{CCx} ≤ 1.5V	—	210	250	
		0V ≤ V_{CCx} ≤ 2.45V	—	360	400	
AUX						
$V_{TH\_UVLO\_AUX}$	Rising threshold voltage for UVLO	—	2.65	2.75	2.85	V
—	Hysteresis	—	—	100	—	mV
$I_{AUX(DIS)}$	Disabled supply current	V_{EN} = 0V, -40°C ≤ T_J ≤ +85°C	—	—	1	μA
$I_{AUX(CC\_OPEN)}$	Enabled internal supply current with CC lines open	-40°C ≤ T_J ≤ +85°C	—	0.2	1	μA
$I_{AUX(Ra)}$	Enabled supply current with accessory or dangling active cable signature on CC lines	—	—	160	200	μA
$I_{AUX(Rd\_noIN)}$	Enabled supply current with UFP termination on CC lines and with either IN1 or IN2 in UVLO	V_{IN1} < $V_{TH\_UVLO\_IN1}$ or V_{IN2} < $V_{TH\_UVLO\_IN2}$	—	145	200	μA
$I_{AUX(Rd)}$	Enabled supply current with UFP termination on CC lines	—	—	120	150	μA

Switching Characteristics

(-40°C ≤ T_J ≤ +125°C, 4.5V ≤ V_{IN1} ≤ 6.5V, 4.5V ≤ V_{IN2} ≤ 5.5V, 2.9V ≤ V_{AUX} ≤ 5.5V; V_{EN} = V_{CHG} = V_{CHG_HI} = V_{AUX}, R_{REF} = 100kΩ. Typical values are at +25°C. All voltages are with respect to GND. I_{OUT} and I_{OS} defined positive out of the indicated pin, unless otherwise specified.)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
OUT – POWER SWITCH						
t_r	Output-voltage rise time	V_{IN1} = 5V, C_L = 1µF, R_L = 100Ω (measured from 10% to 90% of final value)	1.2	1.8	2.5	ms
t_f	Output-voltage fall time		—	0.10	0.35	ms
t_{on}	Output-voltage turn-on time	V_{IN1} = 5V, C_L = 1µF, R_L = 100Ω	2.5	3.5	5	ms
t_{off}	Output-voltage turn-off time		—	0.10	0.35	ms
OUT – CURRENT LIMIT						
t_{ios}	Current-limit response time to short circuit (Note 9)	V_{IN1} – V_{OUT} = 1V, R_L = 10mΩ, see Figure 1	—	3.5	—	µs
$\overline{\text{FAULT}}$						
t_{DEGA}	Asserting deglitch due to overcurrent	—	5.5	8.2	10.7	ms
$t_{DEGA(OC)}$	Asserting deglitch due to overtemperature in current limit (Note 9)	—	—	0	—	ms
$t_{DEGA(OT)}$	Deasserting deglitch	—	5.5	8.2	10.7	ms
$\overline{\text{LD\_DET}}$						
t_{DEGA}	Asserting deglitch	—	45	65	96	ms
t_{DEGD}	Deasserting deglitch	—	1.45	2.15	2.9	s
OUT – DISCHARGE						
—	R_{DCHG} discharge time	V_{OUT} = 1V, time I_{SNK_OUT} > 1mA after UFP signature removed from CC lines	39	65	96	ms
CC1, CC2 - V_{CONN} POWER SWITCH						
t_r	Output-voltage rise time	V_{IN2} = 5V, C_L = 1µF, R_L = 100Ω (measured from 10% to 90% of final value)	0.15	0.25	0.40	ms
t_f	Output-voltage fall time		0.18	0.22	0.35	ms
t_{on}	Output-voltage turn-on time	V_{IN2} = 5V, C_L = 1µF, R_L = 100Ω	0.9	1.5	2	ms
t_{off}	Output-voltage turn-off time		0.15	0.4	0.55	ms
CC1, CC2 – V_{CONN} POWER SWITCH – CURRENT LIMIT						
t_{res}	Current limit response time to short circuit (Note 9)	V_{IN2} – V_{CONN} = 1V, R = 10mΩ, see Figure 1	—	1	—	µs
$\overline{\text{UFP}}$, $\overline{\text{POL}}$, $\overline{\text{AUDIO}}$, $\overline{\text{DEBUG}}$						
t_{DEGR}	Asserting deglitch	—	100	150	200	ms
t_{DEGF}	Deasserting deglitch	—	7.9	12.5	17.7	ms

Typical Performance Characteristics

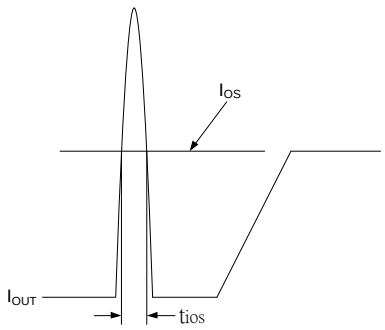


Figure 1. Output Short-Circuit Timing Diagram

Typical Performance Characteristics (T_A = +25°C, V_{IN1} = 5V, V_{IN2} = 5V, V_{AUX} = 5V, C_{IN} = 150µF, C_L = 10µF, unless otherwise specified.)

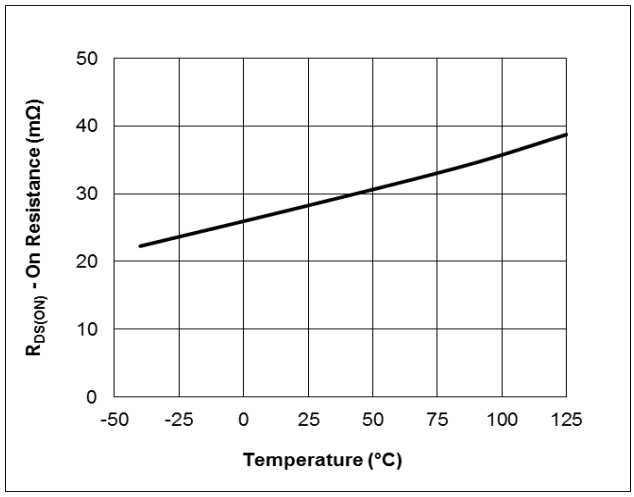


Figure 2. VBUS Current Limiting Switch On Resistance vs. Temperature

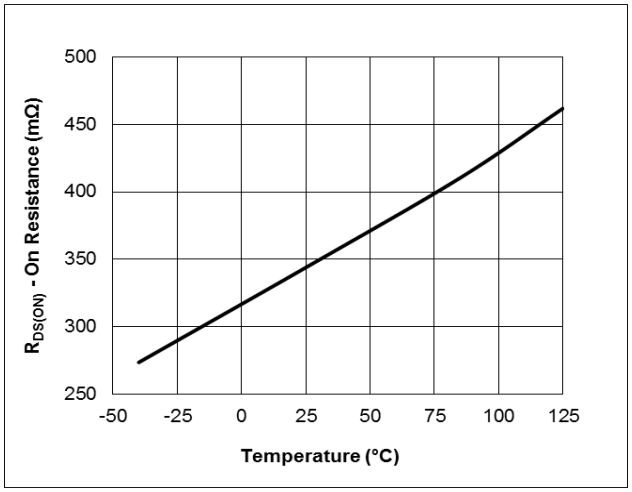


Figure 3. VCONN Current Limiting Switch On Resistance vs. Temperature

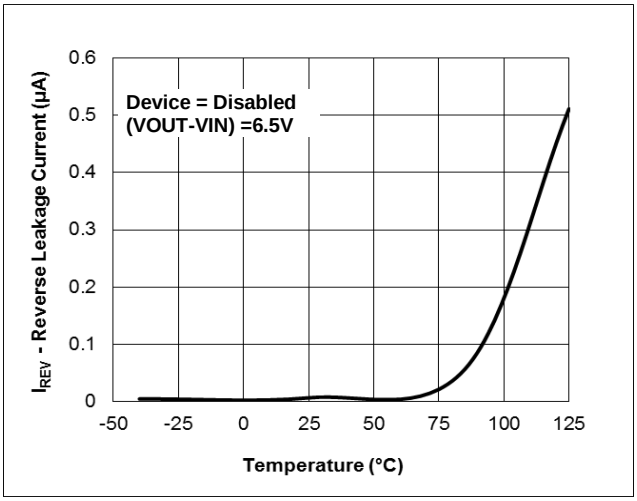


Figure 4. OUT Reverse Leakage Current vs. Temperature

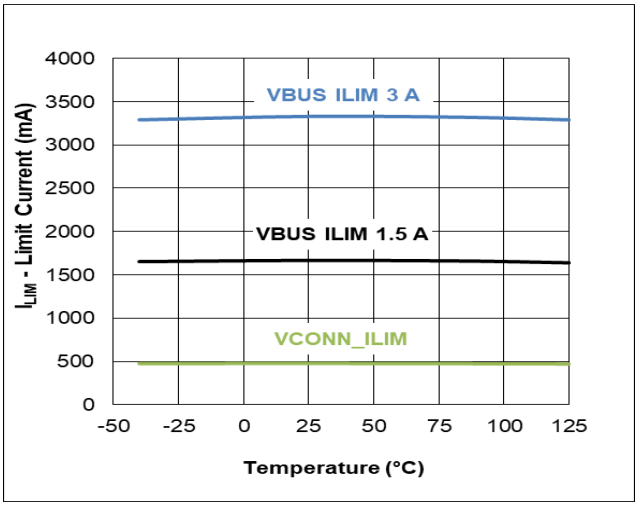


Figure 5. ILIM for VBUS and VCON vs. Temperature

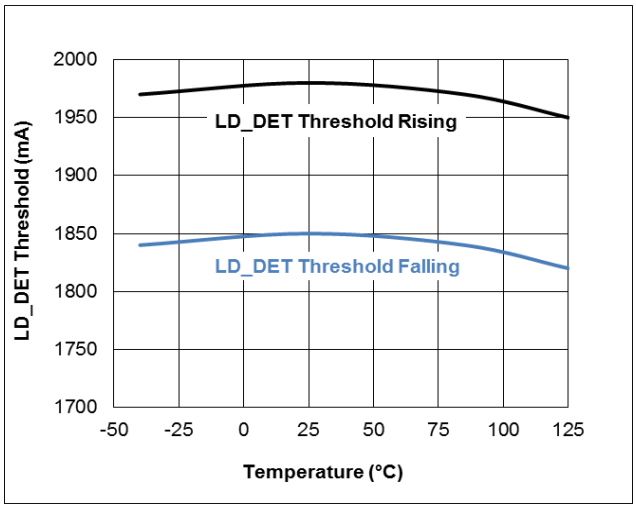


Figure 6. LD_DET Threshold vs. Temperature

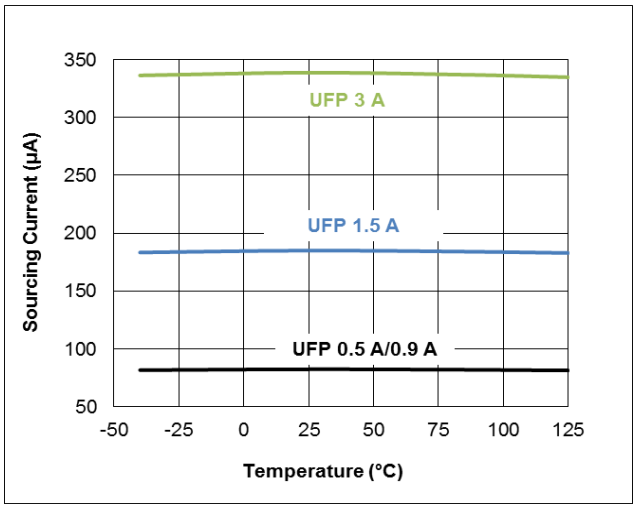


Figure 7. CC Sourcing Current to UFP vs. Temperature

Typical Performance Characteristics (continued) (T_A = +25°C, V_{IN1} = 5V, V_{IN2} = 5V, V_{AUX} = 5V, C_{IN} = 150µF, C_L = 10µF, unless otherwise specified.)

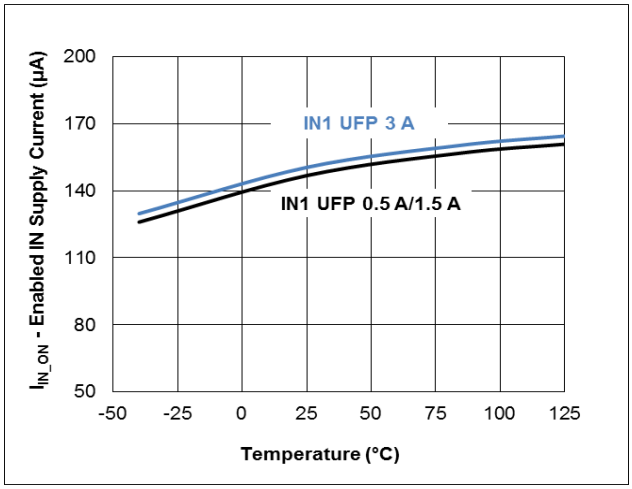


Figure 8. IN1 Current with UFP vs. Temperature

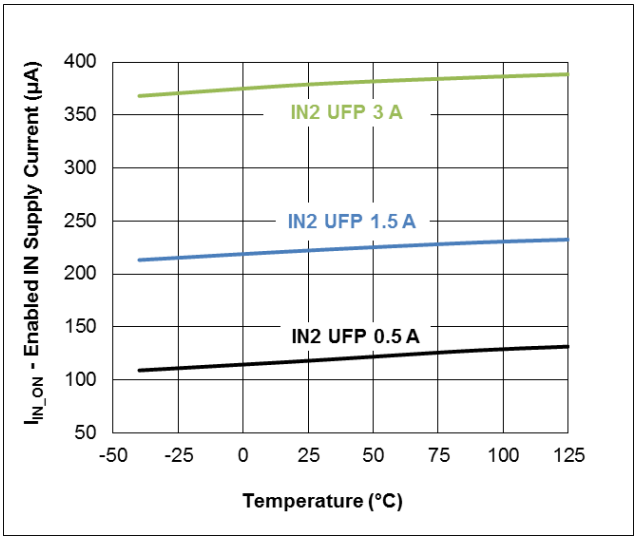


Figure 9. IN2 Current with UFP vs. Temperature

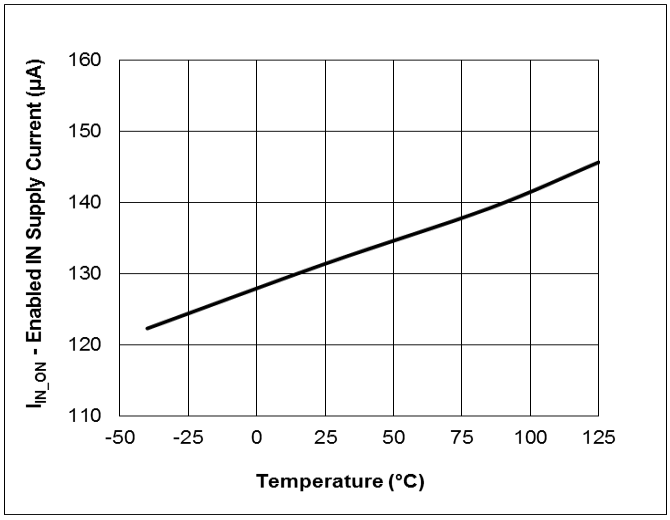
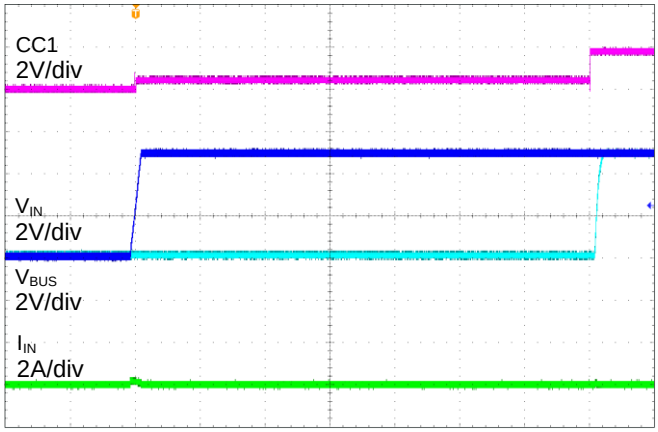


Figure 10. AUX Current with UFP vs. Temperature

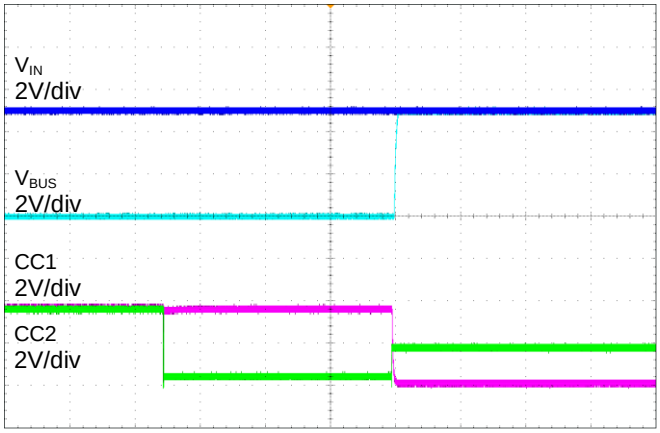
Application Curves (T_A = +25°C, V_{IN1} = 5V, V_{IN2} = 5V, V_{AUX} = 5V, C_{IN} = 150µF, C_L = 10µF, unless otherwise specified.)



20ms/div

Basic startup: IN1 = IN2 = AUX = EN = CHG = CHG_HI = 5V, CC1 = Rd, CC2 = open

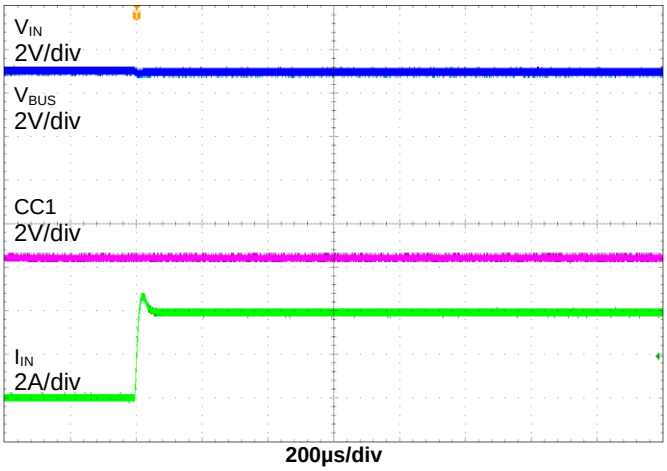
Figure 11. Basic Startup



40ms/div

IN1 = IN2 = AUX = EN = CHG = CHG_HI = 5V, CC1 = open, CC2 = open → Rd

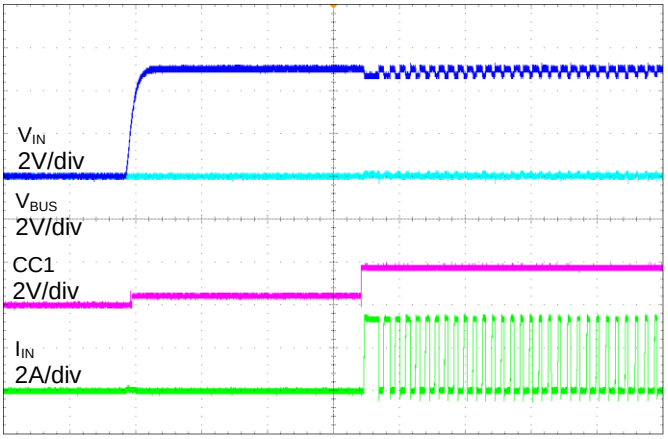
Figure 12. Startup



200µs/div

IN1 = IN2 = AUX = EN = 5V; CHG = CHG_HI = 0V, CC1 = open, CC2 = Rd, OUT = open → 5 Ω

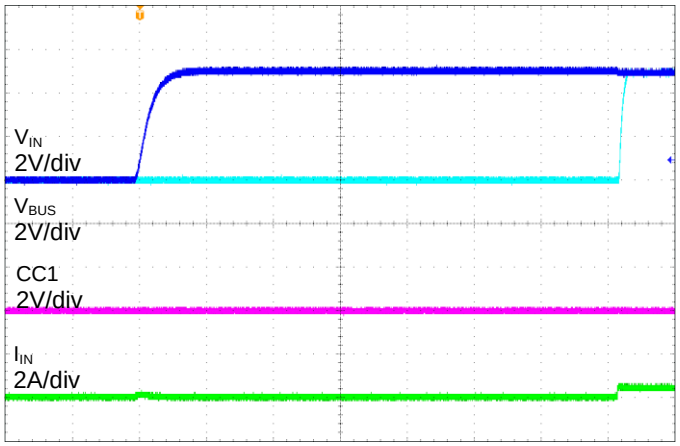
Figure 13. Load Step



40ms/div

IN1 = IN2 = AUX = EN = CHG = CHG_HI = 5V, CC1 = Rd, CC2 = open, OUT = shorted

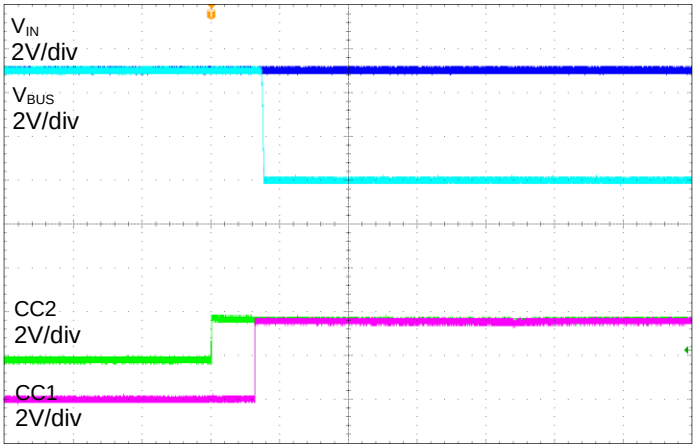
Figure 14. Hot-Plug to Short



20ms/div

IN1 = IN2 = AUX = EN = CHG = CHG_HI = 5V, CC1 = short, CC2 = Rd

Figure 15. Short On CC1

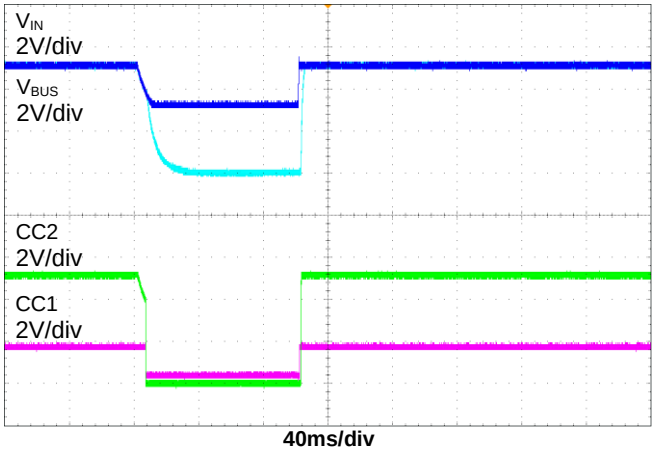


20ms/div

IN1 = IN2 = AUX = EN = CHG = CHG_HI = 5V, CC1 = open, CC2 = Rd → open

Figure 16. Remove Rd

Application Curves (continued) (T_A = +25°C, V_{IN1} = 5V, V_{IN2} = 5V, V_{AUX} = 5V, C_{IN} = 150µF, C_L = 10µF, unless otherwise specified.)



40ms/div

V_{IN} 5V → 3.5V → 5V,
IN1 = IN2 = AUX = EN = CHG = CHG_HI = 5V,
CC1 = Rd, CC2 = Ra

Figure 17. Brownout Test

Detailed Description

Overview

The AP25810LQ device is a highly integrated USB-C downstream-facing port (DFP) controller with built-in power switch developed for the new USB-C connector and cable. The device provides all the functionalities needed to support a USB-C DFP in a system where USB power delivery (PD) source capabilities (for example, V_{BUS} > 5V) are not implemented.

USB-C Basic

For a detailed description of the Type-C specification, see the USB-IF website to download the latest released version. Some of the basic concepts of the Type-C specification that pertain to understanding the operation of the AP25810LQ device (a DFP device) are described as follows.

USB-C removes the need for different plug and receptacle types for host and device functionality. The Type-C receptacle replaces both Type-A and Type-B receptacles because the Type-C cable is pluggable in either direction between host and device. A host-to-device logical relationship is maintained via the configuration channel (CC). Optionally, hosts and devices can be either providers or consumers of power when USB PD communication is used to swap roles.

All USB-C ports operate in one of the following three data modes:

- Host mode: the port can only be host (provider of power).
- Device mode: the port can only be device (consumer of power).
- Dual-role mode: the port can be either host or device.

Port types:

- DFP (downstream-facing port): Host
- UFP (upstream-facing port): Device
- DRP (dual-role port): Host or device

Valid DFP-to-UFP connections:

- Table 1 describes valid DFP-to-UFP connections.
- Host-to-host and device-to-device have no functions.

Table 1. DFP-to-UFP Connections

	HOST-MODE PORT	DEVICE-MODE PORT	DUAL-ROLE PORT
Host-mode port	No function	Works	Works
Device-mode port	Works	No function	Works
Dual-role port	Works	Works	Works (Note 10)

Note: 10. This may be automatic or manually driven.

Configuration Channel

The function of the configuration channel (CC) is to detect connections and configure the interface across the USB-C cables and connectors.

Functionally, the configuration channel serves the following purposes:

- Detect connection to the USB ports
- Resolve cable orientation and twist connections to establish USB data bus routing
- Establish DFP and UFP roles between two connected ports
- Discover and configure power: USB-C current modes or USB power delivery
- Discover and configure optional alternate and accessory modes
- Enhance flexibility and ease of use

Detailed Description (continued)

Typical flow of DFP to UFP configuration is shown in Figure 18:

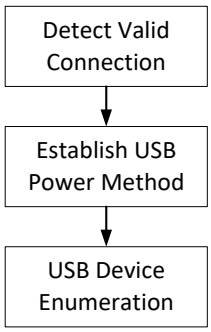


Figure 18. Flow of DFP to UFP Configuration

Detecting a Connection

DFPs and DRPs fulfill the role of detecting a valid connection over USB-C. Figure 19 shows a DFP-to-UFP connection made with Type-C cable. As shown in Figure 19, the detection concept is based on being able to detect terminations in the product that has been attached. A pullup and pulldown termination model is used. A pullup termination can be replaced by a current source.

- In the DFP-UFP connection, the DFP monitors both CC pins for a voltage lower than the unterminated voltage.
- A UFP advertises Rd on both its CC pins (CC1 and CC2).
- A powered cable advertises Ra on only one of the CC pins of the plug. Ra is used to inform the source to apply V_{CONN}.
- An analog audio device advertises Ra on both CC pins of the plug, which identifies it as an analog audio device. V_{CONN} is not applied on either CC pin in this case.

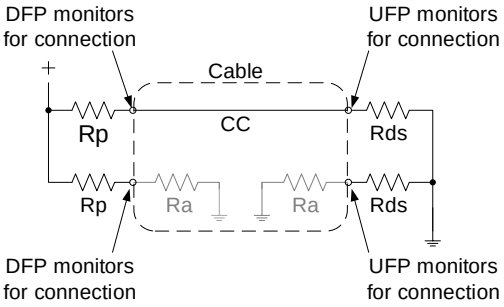


Figure 19. DFP-UFP Connection

The AP25810LQ is a DFP Type-C port controller with integrated power switch for V_{CONN} and V_{BUS}. The AP25810LQ does not support BC1.2 charging modes since it does not interact with USB D+/D- data lines. It can be used in conjunction with a BC 1.2 device to support BC1.2 and Type-C charging modes in a single Type-C DFP port. The AP25810LQ can be used in a USB 2.0 only or USB 3.1 port implementation. When used in a USB 3.1 port, the AP25810LQ can control an external super speed MUX to handle the Type-C flippable feature.

Feature Description

Configuration Channel Pins CC1 and CC2

The AP25810LQ has CC1 and CC2 that serve to detect an attachment to the port and resolve cable orientation. These pins are also used to establish current broadcast to a valid UFP, configure V_{CONN}, and detect Debug or Audio Adapter Accessory attachment.

Table 2. AP25810LQ Response to Various Attachments to Its Port

AP25810LQ TYPE-C PORT	CC1	CC2	AP25810LQ Response (Note 11)					
			OUT	V_{CONN} on CC1 or CC2	$\overline{POL}$	$\overline{UFP}$	$\overline{AUDIO}$	$\overline{DEBUG}$
Nothing attached	OPEN	OPEN	OPEN	NO	Hi-Z	Hi-Z	Hi-Z	Hi-Z
UFP connected	Rd	OPEN	IN1	NO	Hi-Z	LOW	Hi-Z	Hi-Z
UFP connected	OPEN	Rd	IN1	NO	LOW	LOW	Hi-Z	Hi-Z
Powered cable, no UFP connected	OPEN	Ra	OPEN	NO	Hi-Z	Hi-Z	Hi-Z	Hi-Z
Powered cable, no UFP connected	Ra	OPEN	OPEN	NO	Hi-Z	Hi-Z	Hi-Z	Hi-Z
Powered cable, UFP connected	Rd	Ra	IN1	CC2	Hi-Z	LOW	Hi-Z	Hi-Z
Powered cable, UFP connected	Ra	Rd	IN1	CC1	LOW	LOW	Hi-Z	Hi-Z
Debug accessory connected	Rd	Rd	OPEN	NO	Hi-Z	Hi-Z	Hi-Z	LOW
Audio-adapter accessory connected	Ra	Ra	OPEN	NO	Hi-Z	Hi-Z	LOW	Hi-Z

Note: 11. $\overline{UFP}$, $\overline{POL}$, $\overline{AUDIO}$ and $\overline{DEBUG}$ are open-drain outputs; pull high with 100kΩ to AUX when used. Tie to GND or leave open when not used.

Current Capability Advertisement and Overload Protection

The AP25810LQ supports all three Type-C current advertisements as defined by the USB-C standard. Current broadcast to a connected UFP is controlled by the CHG and CHG_HI pins. For each broadcast level the device protects itself from a UFP that draws current in excess of the port's USB-C current advertisement by setting the current limit as shown in Table 3.

Table 3. USB-C Current Advertisement

CHG	CHG_HI	CC Capability Broadcast	Current Limit (Typ)	Load Detect Threshold (Typ)
0	0	STD	1.7A	NA
0	1	STD	1.7A	NA
1	0	1.5A	1.7A	NA
1	1	3A	3.4A	1.95A

Under overload conditions, the internal current-limit regulator limits the output current to selected I_{LIM} for OUT and fixed internal V_{CONN} current limit as shown in the *Electrical Characteristics*. When an overload condition is present, the device maintains a constant output current, with the output voltage determined by (I_{OS} x R_{LOAD}). Two possible overload conditions can occur. The first overload condition occurs when either: 1) input voltage is first applied, enable is true, and a short circuit is present (load which draws $I_{OUT} > I_{OS}$), or 2) input voltage is present and the AP25810LQ is enabled into a short circuit. The output voltage is held near zero potential with respect to ground and the AP25810LQ ramps the output current to I_{OS}. The AP25810LQ limits the current to I_{OS} until the overload condition is removed or the device begins to thermal cycle. This is demonstrated with the Hot-Plug to Short waveform (Figure 14) in the application curve where the device was enabled into a short, and subsequently cycles current off and on as the thermal protection engages.

The second condition is when an overload occurs while the device is enabled and fully turned on. The device responds to the overload condition within time t_{ios} (see Figure 1) when the specified overload (per *Electrical Characteristics*) is applied. The response speed and shape vary with the overload level, input circuit, and rate of application. The current-limit response varies between simply settling to I_{OS} or turn-off and controlled return to I_{OS}. Similar to the previous case, the AP25810LQ limits the current to I_{OS} until the overload condition is removed or the device begins to thermal cycle.

Feature Description (continued)

The AP25810LQ thermal cycles if an overload condition is present long enough to activate thermal limiting in any of the above cases. This is due to the relatively large power dissipation [(V_{IN} – V_{OUT}) x I_{OS}] driving the junction temperature up. The device turns off when the junction temperature exceeds +135°C (min) while in current limit. The device remains off until the junction temperature cools +20°C and then restarts. The AP25810LQ current limit profile is shown in Figure 20.

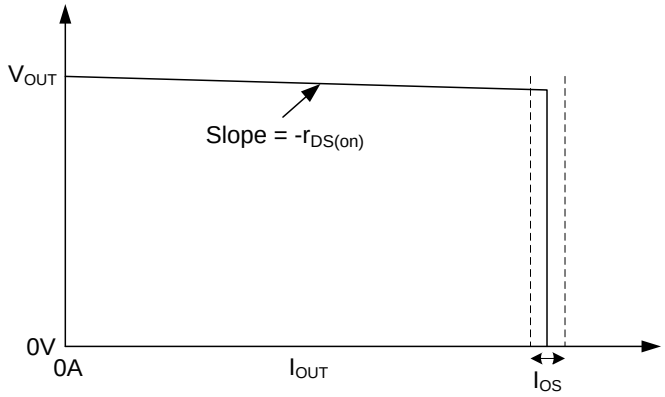


Figure 20 Current Limit Profile

Undervoltage Lockout (UVLO)

The undervoltage lockout (UVLO) circuit disables the power switch until the input voltage reaches the UVLO turn-on threshold. Built-in hysteresis prevents unwanted on/off cycling due to input voltage droop during turn on.

Device Power Pins (IN1, IN2, AUX, OUT, and GND)

The device has multiple input power pins; IN1, IN2 and AUX. IN1 is connected to OUT by the internal power FET and serves the supply for the Type-C charging current. IN2 is the supply for V_{CONN} and ties directly between the V_{CONN} power switch on its input and CC1 or CC2 on its output. AUX or auxiliary input supply provides power to the chip.

In the simplest implementation where multiple supplies are not available, IN1, IN2, and AUX can be tied together. However, in mobile systems (battery powered) where system power savings is paramount, IN1 and IN2 can be powered by the high power DC-DC supply (> 3A capability) while AUX can be connected to the low power supply that typically powers the system microcontroller when the system is in hibernate or sleep power state. A ceramic bypass capacitor close to the device from INx/AUX to GND is recommended to alleviate bus transients.

The recommended operating voltage range for IN1/IN2 is 4.5V to 5.5V while AUX can be operated from 2.9V to 5.5V. However, IN1, the high power supply, can operate up to 5.5V. This higher input voltage affords a larger IR drop budget in systems where a long cable harness is used and results in high IR drops with 3A charging current while meeting the USB spec for V_{BUS} at connector ≥ 4.75V.

Figure 21 illustrates the point. In this example IN1 is at 5V which restricts the IR drop budget from DC-DC to connector to 250mV.

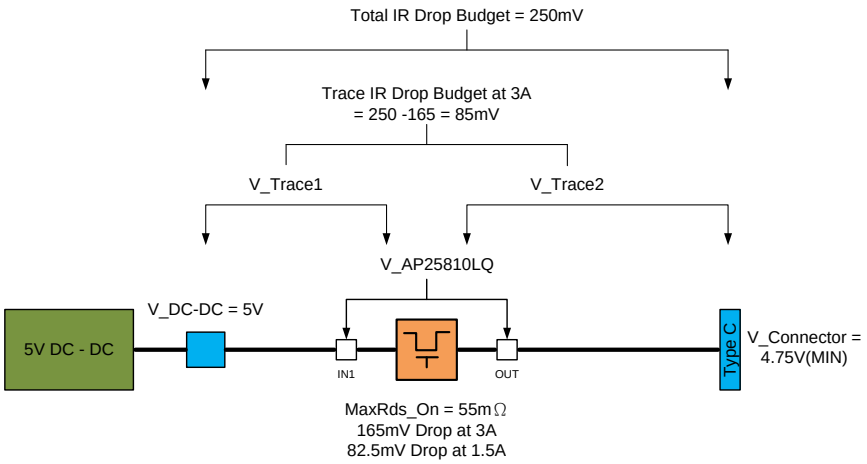


Figure 21. Total IR Loss Budget

Feature Description (continued)

FAULT Response

The $\overline{FAULT}$ pin is an open-drain output that asserts (active low) when device OUT current exceeds its programmed value and the overtemperature threshold is crossed (T_{TH_OTSD1}). Refer to the *Electrical Characteristics* for overcurrent and temperature values. The $\overline{FAULT}$ signal remains asserted until the fault condition is removed and the device resumes normal operation. The AP25810LQ is designed to eliminate false overcurrent fault reporting by using an internal deglitch circuit. Connect $\overline{FAULT}$ with a pullup resistor to AUX. $\overline{FAULT}$ can be left open or tied to GND when not used.

Thermal Shutdown

The device has two internal overtemperature shutdown thresholds, T_{TH_OTSD1} and T_{TH_OTSD2}, to protect the internal MOS from damage and ensure overall safety of the system. $T_{TH\_OTSD2} > T_{TH\_OTSD1}$. $\overline{FAULT}$ is asserted low to signal a fault condition when device temperature exceeds T_{TH_OTSD1} and the current limit switch is disabled. However, when T_{TH_OTSD2} is exceeded, all open-drain outputs are left open and the device is disabled such that minimal power/heat is dissipated. The device attempts to power up when temperature decreases by 20°C.

REF

A 100kΩ (1% or better recommended) resistor is connected from this pin to REF_RTN. This pin sets the reference current required to bias the internal circuitry of the device. The overload current limit tolerance and CC currents depend upon the accuracy of this resistor, using a ±1% low temperature coefficient resistor, or better, yields the best current limit accuracy and overall device performance.

Audio Accessory Detection

The USB-C spec defines an audio adapter decode state which allows implementation of an analog USB-C to 3.5mm headset adapter. The AP25810LQ detects an audio accessory device when both CC1 and CC2 pins see VRa voltage (when pulled to ground by Ra resistor). The device asserts the open-drain AUDIO pin low to indicate the detection of such a device.

Table 4. Audio Accessory Detection

CC1	CC2	$\overline{AUDIO}$	STATE
Ra	Ra	Asserted (pulled low)	Audio-adapter accessory connected

Platforms supporting the audio accessory function can be triggered by the $\overline{AUDIO}$ pin to enable accessory mode circuits to support the audio function. When the Ra pulldown is removed from the CC2 pin, $\overline{AUDIO}$ is deasserted or pulled high. The AP25810LQ device monitors the CC2 pin for audio device detach. When this function is not needed (for example in a data-less port), $\overline{AUDIO}$ can be tied to GND or left open.

Debug Accessory Detection

The Type-C spec supports an optional debug-accessory mode, used for debug only and not to be used for communicating with commercial products. When the AP25810LQ device detects VRd voltage on both CC1 and CC2 pins (when pulled to ground by an Rd resistor), it asserts $\overline{DEBUG}$ low. With $\overline{DEBUG}$ asserted, the system can enter debug mode for factory testing or a similar functional mode. $\overline{DEBUG}$ deasserts or pulls high when Rd is removed from CC1. The AP25810LQ device monitors the CC1 pin for debug-accessory detach. If the debug-accessory mode is not used, tie $\overline{DEBUG}$ to GND or leave it open.

Table 5. Debug Accessory Detection

CC1	CC2	$\overline{POL}$	STATE
Rd	Rd	Asserted (pulled low)	Debug accessory connected

Plug Polarity Detection

Reversible Type-C plug orientation is reported by the $\overline{POL}$ pin when a UFP is connected. However, when no UFP is attached, $\overline{POL}$ remains deasserted, irrespective of cable plug orientation. Table 6 describes the $\overline{POL}$ state based on which of the device CC pins detect V_{Rd} from an attached UFP pulldown.

Table 6. Plug Polarity Detection

CC1	CC2	$\overline{POL}$	STATE
Rd	Open	Hi-Z	UFP connected
Open	Rd	Asserted (pulled low)	UFP connected with reverse plug orientation

Feature Description (continued)

Figure 22 shows an example implementation which uses the POL terminal to control the SEL terminal on the PI3PCIE3212 device. The PI3PCIE3212 device provides switching on the differential channels between Port B and Port C to Port A, depending on cable orientation. For details on the PI3PCIE3212 device, see the PI3PCIE3212 data sheet.

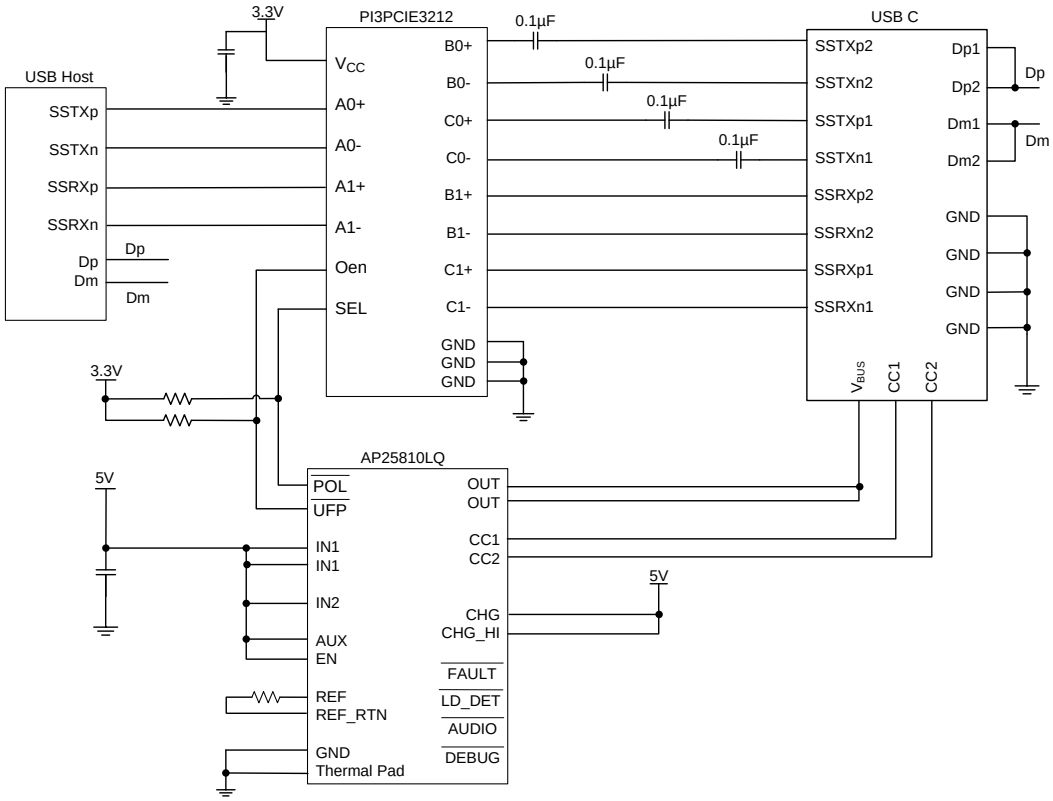


Figure 22. Example Implementation

Device Enable Control

The logic enable pin (EN) controls the power switch and device supply current. The supply current is reduced to less than 1µA when a logic low is present on EN. The EN pin provides a convenient way to turn on or turn off the device while it is powered. The enable input threshold has built-in hysteresis. When this pin is pulled high, the device is turned on or enabled. When the device is disabled (EN pulled low) the internal FETs tied to IN1 and IN2 are disconnected, all open-drain outputs are left open (Hi-Z), and the monitor block for CC1 and CC2 is turned off. The EN terminal should not be left floating.

Load Detect

The load-detect function in the device is enabled when the device is set to broadcast high-current V_{BUS} charging (CHG = CHG_HI = High) on the CC pin. In this mode, the device monitors the OUT current to a UFP; if the current exceeds 1.95A (typ), the $\overline{LD\_DET}$ pin asserts. Because $\overline{LD\_DET}$ is an open-drain output, pull it high with 100kΩ to AUX when used; tie it to GND or leave it open when not used.

Feature Description (continued)

Power Wake

The power-wake feature supported in the AP25810LQ device offers the mobile-systems designer a way to save on system power when no UFP is attached to the Type-C port. See Figure 23. To enable power wake, the UFP pins from device No. 1 and No. 2 are tied together (each with its own 100kΩ pullup) to the enable pin of a 5V, 6A DC-DC buck converter. When no UFP is detected on both Type-C ports, the EN pin of the DC-DC converter is pulled high, thereby disabling it. Because both AP25810LQ devices are powered by an always-on 3.3V LDO, turning off the supply to IN1 and IN2 does not affect its operation in detach state. Anytime a UFP is detected on either port, the corresponding AP25810LQ UFP pin is pulled low, enabling the DC-DC converter to provide charging current to the attached UFP. Turning off the high-power DC-DC converter when ports are unattached saves on system power. This method can save a significant amount of power, because the AP25810LQ device only requires < 5µA when no UFP device is connected.

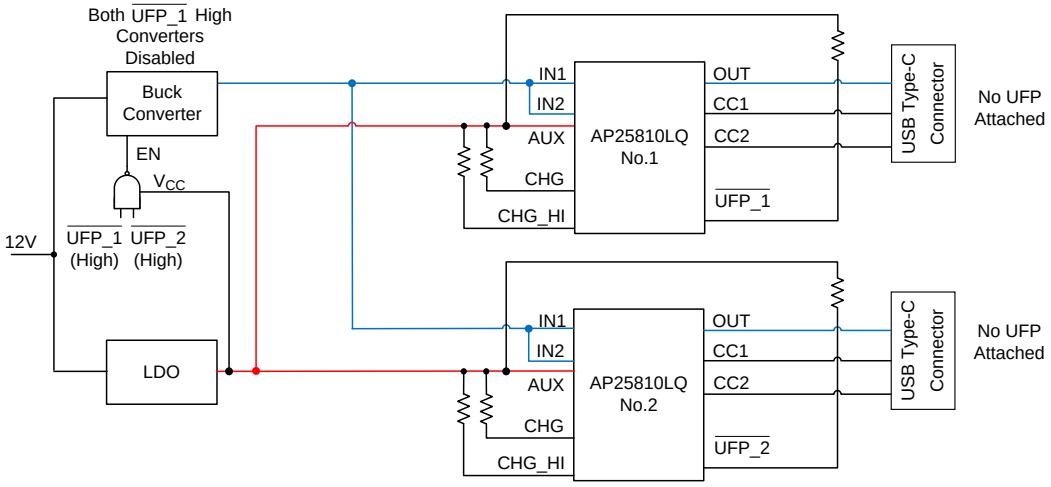


Figure 23 Power Wake

Table 7. Recommended Buck Converter

Part Number	Max Operating VIN [V]	VOUT [V]	Max IOUT [A]	Package
AP62600	18	Adjustable, 5.0	6.0	V-QFN2030-12 (Type A)
AP63356/7	32	Adjustable, 5.0	3.5 (Note 12)	V-DFN3020-13 (Type A)
AP6435x	40	Adjustable, 5.0	3.5 (Note 12)	SO-8EP
AP6450x	40	Adjustable, 5.0	5.0	SO-8EP

Note: 12. 3.5A is for 3A single Type-C port or dual ports with 1.5A capability each.

Table 8. Recommended LDO

Part Number	Max Operating VIN [V]	VOUT [V]	Max IOUT [mA]	Package
AP2205-33	24	3.3	200	SOT25, SOT89
AP7370-33	18	3.3	300	SOT25, SOT89, U-DFN2020-6, SOT23
AP7380-33	24	3.3	150	SOT89, SOT25

Table 9. Recommended NAND Gate

Part Number	Max Operating VCC [V]	# of Gate	# of Inputs	Package
74AUP1G00	3.6	1	2	SOT353, X2-DFN0808-4, X2-DFN1010-6, X2-DFN1409-6, X2-DFN14140-6
74LVCE1G00	5.5	1	2	SOT25, SOT353

Feature Description (continued)

Port Power Management (PPM)

PPM is the intelligent and dynamic allocation of power made possible with the use of the $\overline{LD\_DET}$ pin. PPM is for systems that have multiple charging ports but cannot power them all at their maximum charging current simultaneously.

Goals of PPM are:

- Enhanced user experience, as it is unnecessary for the user to search for a high-current charging port.
- Lowered cost and size of the power supply needed for implementing high-current charging in a multiport system.

Implementing PPM in a System with Two Type-C Ports

Figure 24 shows PPM and power wake implemented in a system with two Type-C ports both initially set to broadcast high-current charging (3A, CHG and CHG_HI pulled high via a 100kΩ to AUX). To enable PPM tie the $\overline{LD\_DET}$ pin from AP25810LQ #1 to CHG_HI of AP25810LQ #2 and vice versa as shown in Figure 24. Each device independently monitors charging current drawn by its attached UFP.

IN1 and IN2 are connected to a DC-DC power source, a 6A synchronous step-down converter. AUX is powered by a low quiescent current 3.3V LDO. With no UFP attached to either Type-C port, the AP25810LQ is powered by the LDO. This method saves a significant amount of power, considering that the AP25810LQ requires less than 2μA when no USB device is connected.

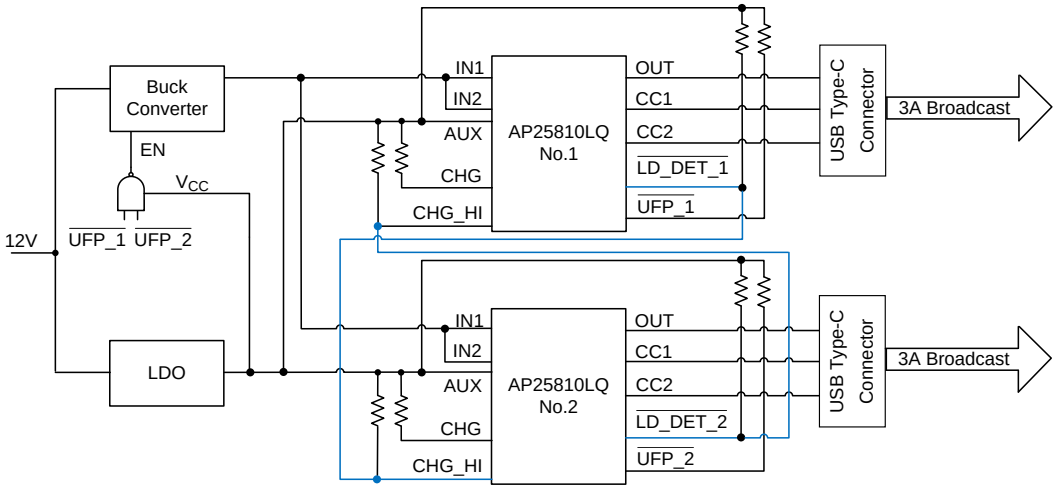


Figure 24. PPM and Power Wake Implemented

PPM Operation

When no UFP is attached, or either of the two attached UFPs is drawing current less than the $\overline{LD\_DET}$ threshold (1.95A typical), the $\overline{LD\_DET}$ output for both devices is high (shown in blue in Figure 25). Now when a UFP is attached to device No. 1 that draws a charging current higher than the $\overline{LD\_DET}$ threshold (1.95A), this causes $\overline{LD\_DET}$ to assert or pull low (shown in red in Figure 25). Because the $\overline{LD_DET}$pins of the No. 1 and No. 2 devices are connected to the CHG_HI pins of each other, a high-current detection on device No. 1 forces device No. 2 to broadcast 1.5A or medium charging-current capability on its CC pin. The Type-C specification requires a UFP to monitor the CC pins continuously and adjust its current consumption (within 60ms) to remain within the value advertised by the DFP.

Figure 26 shows the case when a UFP attached to device No. 1 reduces its charging current below the $\overline{LD\_DET}$ threshold, which causes $\overline{LD\_DET}$ to deassert, thereby toggling the device No. 2 CH_HI pin from low to high.

This scheme:

- Delivers a better user experience, as the user has no worry about the maximum charging current rating of the host ports. Both ports initially advertise high-current charging.
- Enables a smaller and lower-cost power supply, as the loading is controlled and never allowed to exceed 5A.

Feature Description (continued)

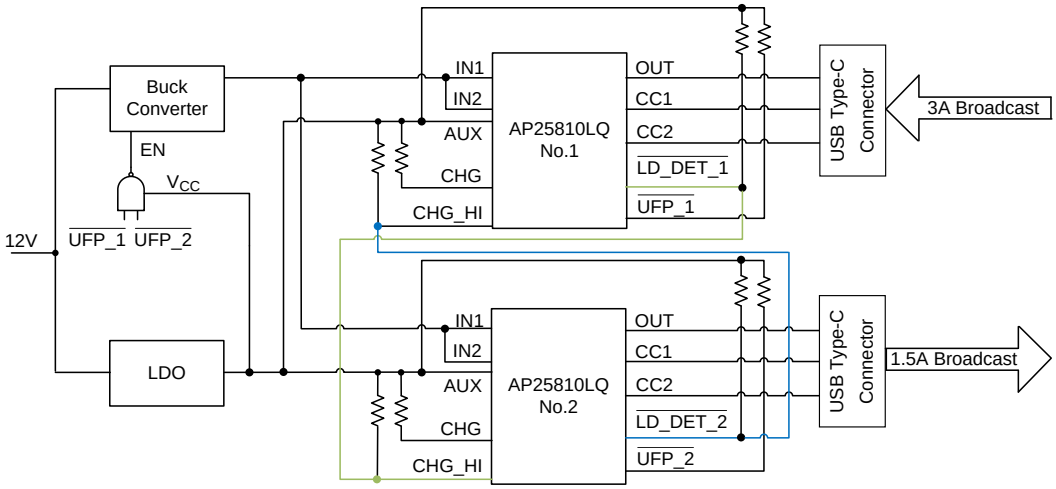


Figure 25. 3A USB Device Connected

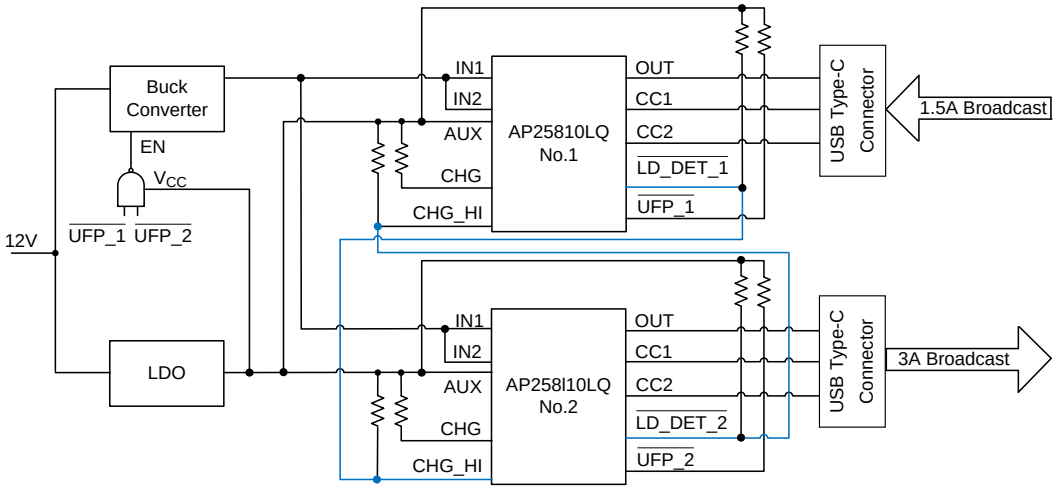


Figure 26. 1.5A USB Device Connected

Device Functional Modes

The AP25810LQ device is a Type-C controller with integrated power switch that supports all Type-C functions in a downstream facing port. The device is also used to manage current advertisement and protection for a connected UFP and active cable. The device starts its operation by monitoring the AUX bus. When V_{AUX} exceeds the undervoltage-lockout threshold, the device samples the EN pin. A high level on this pin enables the device, and normal operation begins. Having successfully completed its startup sequence, the device now actively monitors its CC1 and CC2 pins for attachment to a UFP. When a UFP is detected on either the CC1 or CC2 pin, the internal MOSFET starts to turn on after the required debounce time is met. The internal MOSFET starts conducting and allows current to flow from IN1 to OUT. If Ra is detected on the other CC pin (not connected to the UFP), V_{CONN} is applied to allow current to flow from IN2 to the CC pin connected to Ra. For a complete listing of various device operational modes, see Table 2.

Application Information

The AP25810LQ is a Type-C DFP controller that supports all Type-C DFP required functions. The AP25810LQ only applies power to V_{BUS} when it detects that a UFP is attached and removes power when it detects the UFP is detached. The device exposes its identity via its CC pin advertising its current capability based on CHG and CHG_HI pin settings. The AP25810LQ also limits its advertised current internally and provides robust protection to a fault on the system VBUS power rail.

After a connection is established by the AP25810LQ, the device is capable of providing V_{CONN} to power circuits in the cable plug on the CC pin that is not connected to the CC wire in the cable. V_{CONN} is internally current limited and has its own supply pin IN2. Apart from providing charging current to a UFP, the AP25810LQ also supports Audio and Debug accessory modes.

The following design procedure can be used to implement a full featured Type-C DFP.

Design Requirements

Input and Output Capacitance

Input and output capacitance improves the performance of the device. The actual capacitance should be optimized for the particular application. For all applications, a 0.1µF or greater ceramic bypass capacitor between INx and GND is recommended as close to the device as possible for local noise decoupling.

All protection circuits, such as the AP25810LQ device, have the potential for input voltage overshoots and output voltage undershoots. Input voltage overshoots can be caused by either of two effects. The first cause is an abrupt application of input voltage in conjunction with input power-bus inductance and input capacitance when the INx pin is high-impedance (before turn-on). Theoretically, the peak voltage is 2 times the applied voltage. The second cause is due to the abrupt reduction of output short-circuit current when the AP25810LQ device turns off and energy stored in the input inductance drives the input voltage high. Input voltage droops may also occur with large load steps and as the AP25810LQ output is shorted. Applications with large input inductance (for instance, connecting the evaluation board to the bench power supply through long cables) may require large input capacitance to prevent the voltage overshoot from exceeding the absolute maximum voltage of the device.

The fast current-limit speed of the AP25810LQ device to hard output short circuits isolates the input bus from faults. However, ceramic input capacitance in the range of 1µF to 22µF adjacent to the AP25810LQ input aids in both response time and limiting the transient seen on the input power bus. Momentary input transients to 6.5V are permitted. Output voltage undershoot is caused by the inductance of the output power bus just after a short has occurred and the AP25810LQ device has abruptly reduced the OUT current. Energy stored in the inductance drives the OUT voltage down, and potentially negative, as it discharges. An application with large output inductance (such as from a cable) benefits from the use of a high-value output capacitor to control voltage undershoot.

When implementing 5.0A USB-standard application, 120µF minimum output capacitance is required. Typically, a 150µF electrolytic capacitor is used, which is sufficient to control voltage undershoots. Because in Type-C applications, DFP is a cold socket when no UFP is attached, the output capacitance should be placed at the INx pin versus the OUT pin, as is done in USB-A ports. It is also recommended to put a 10µF ceramic capacitor on the OUT pin for better voltage bypass.

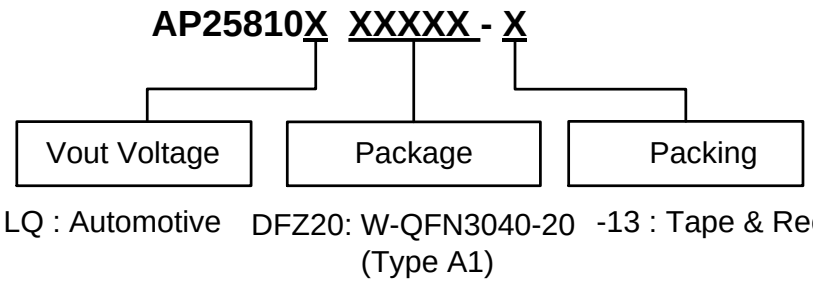
Detailed Design Procedure

The AP25810LQ device supports up to three different input voltages, based on the application. In the simplest implementation, all input pins are tied to a single voltage source set to 5V. However, it is recommended to set a slightly higher (100mV to 200mV) input voltage, when possible, to compensate for IR loss from the source to the Type-C connector.

Other design considerations are listed as follows:

- Place at least 120µF of bypass capacitance close to the INx pins versus the OUT pin, as Type-C is a cold socket connector.
- A 10µF bypass capacitor is recommended to be placed near a Type-C receptacle VBUS pin to handle load transients.
- Depending on the maximum current-level advertisement supported by the Type-C port in the system, set the CHG and CHG_HI levels accordingly.
- EN, CHG, and CHG_HI pins can be tied directly to GND or VAUX without a pullup resistor.
- CHG and CHG_HI can also be dynamically controlled by a microcontroller to change the current advertisement level to the UFP.
- When an open-drain output of the AP25810LQ device is not used, it can be left open or tied to GND.
- Use a 1% 100kΩ resistor to connect between the REF and REF_RTN pins, placing it close to the device pin and isolated from switching noise on the board.

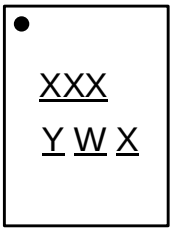
Ordering Information



Orderable Part Number	Part Number Suffix	Package Code	Package	Packing	
				Qty.	Carrier
AP25810LQDFZ20-13	-13	DFZ20	W-QFN3040-20 (Type A1)	3000	13” Tape & Reel

Marking Information

(Top View)



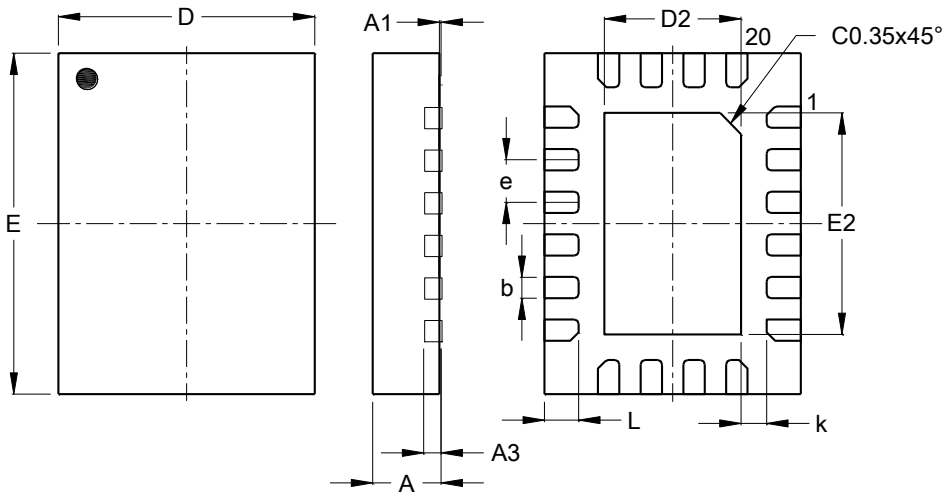
XXX : Identification Code
Y : Year : 0 to 9 (ex: 4 = 2024)
W : Week : A to Z : week 1 to 26;
a to z : week 27 to 52; z represents week 52 and 53
X : Internal Code

Orderable Part Number	Package	Identification Code
AP25810LQDFZ20-13	W-QFN3040-20 (Type A1)	5BQ

Package Outline Dimensions

Please see http://www.diodes.com/package-outlines.html for the latest version.

W-QFN3040-20 (Type A1)

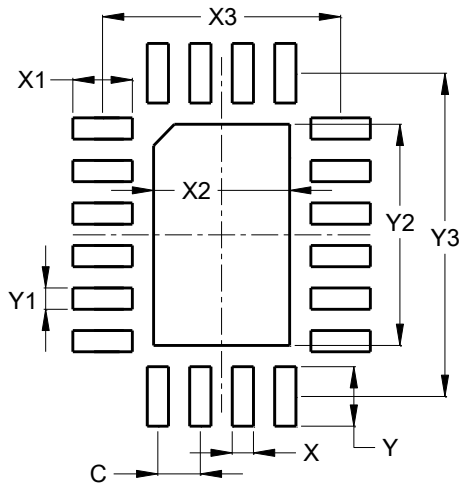


W-QFN3040-20 (Type A1)			
Dim	**Min**	**Max**	**Typ**
A	0.70	0.80	0.75
A1	0.00	0.05	0.02
A3	0.203 REF		
b	0.15	0.25	0.20
D	3.00 BSC		
D2	1.55	1.65	1.60
E	4.00 BSC		
E2	2.55	2.65	2.60
e	0.50 BSC		
k	0.20	--	--
L	0.35	0.45	0.40
All Dimensions in mm			

Suggested Pad Layout

Please see http://www.diodes.com/package-outlines.html for the latest version.

W-QFN3040-20 (Type A1)



Dimensions	Value (in mm)
C	0.500
X	0.250
X1	0.700
X2	1.600
X3	2.800
Y	0.700
Y1	0.250
Y2	2.600
Y3	3.800

Mechanical Data

- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals: Finish – Matte Tin Plated Leads, Solderable per MIL-STD-202, Method 208 e3
- Weight: 0.03728 grams (Approximate)

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