HIGH-PERFORMANCE MULTI-MODE PWM CONTROLLER FOR IoT

Description

The AP3129 is a highly integrated multi-mode peak current controller, which specially provides high efficiency at light load for IoT application. Meanwhile, the AP3129 features a proprietary audible noise elimination technology to ease the acoustic noises from electronic and magnetic components.

The AP3129 is a multi-mode controller, which changes operating mode according to load conditions. Under heavy-load condition, the device operates in CCM (continuous-conduction mode) with a fixed switching frequency of 65kHz, which is helpful to system design with small transformer size. When the loading is decreasing, it enters QR (Quasi Resonant) or Green mode with valley switching for the higher power conversion efficiency. At light load or no load, the IC will operate with its proprietary burst mode to minimize power consumption with the minimum switching frequency (about 22kHz).

The controller architecture is designed to authorize a transient peak power excursion for peak load. It means the frequency can be increased from 65kHz to 130kHz until the peak event disappears.

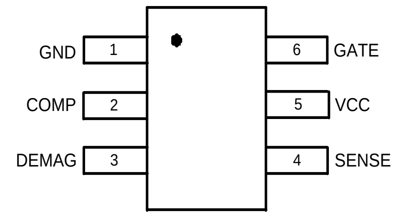
In addition, piecewise linear line compensation ensures accurate constant output power limit over an entire line voltage range.

Features

- Multiple Operation Modes
  - 130kHz Maximum Frequency for Peak Load
  - 65kHz Fixed-Frequency CCM Operation for Full Load
  - 80kHZ Maximum Clamping Frequency for QR Mode
  - Valley Switching Operation in Green Mode
  - Burst Mode Control for Light Load
- High Efficiency at Light Load (> 90% Efficiency at 10% Load)
- Proprietary Audible Noise Elimination Technology
- Soft Start During Startup Process
- Internal Slope Compensation
- Frequency Dithering for Reducing EMI
- VCC Maintain Mode
- Low No-Load Consumption
- Comprehensive System Protection Features
  - Secondary Winding Short Protection
  - VCC Overvoltage Protection (VOVP)
  - Line Overvoltage Protection (LOVP)
  - Overload Protection (OLP)
  - Cycle-by-Cycle Overcurrent Protection
  - Pin-Fault Protection
  - Brown-In/Out Protection (BNI/BNO)
  - Secondary Side OVP (SOVP) and UVP (SUVP)
  - Internal OTP
- SOT26 (Type CJ) is Available
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**
- **For automotive applications requiring specific change control (i.e. parts qualified to AEC-Q100/101/104/200, PPAP capable, and manufactured in IATF 16949 certified facilities), please contact us or your local Diodes representative.**
  https://www.diodes.com/quality/product-definitions/

Pin Assignments

(Top View)



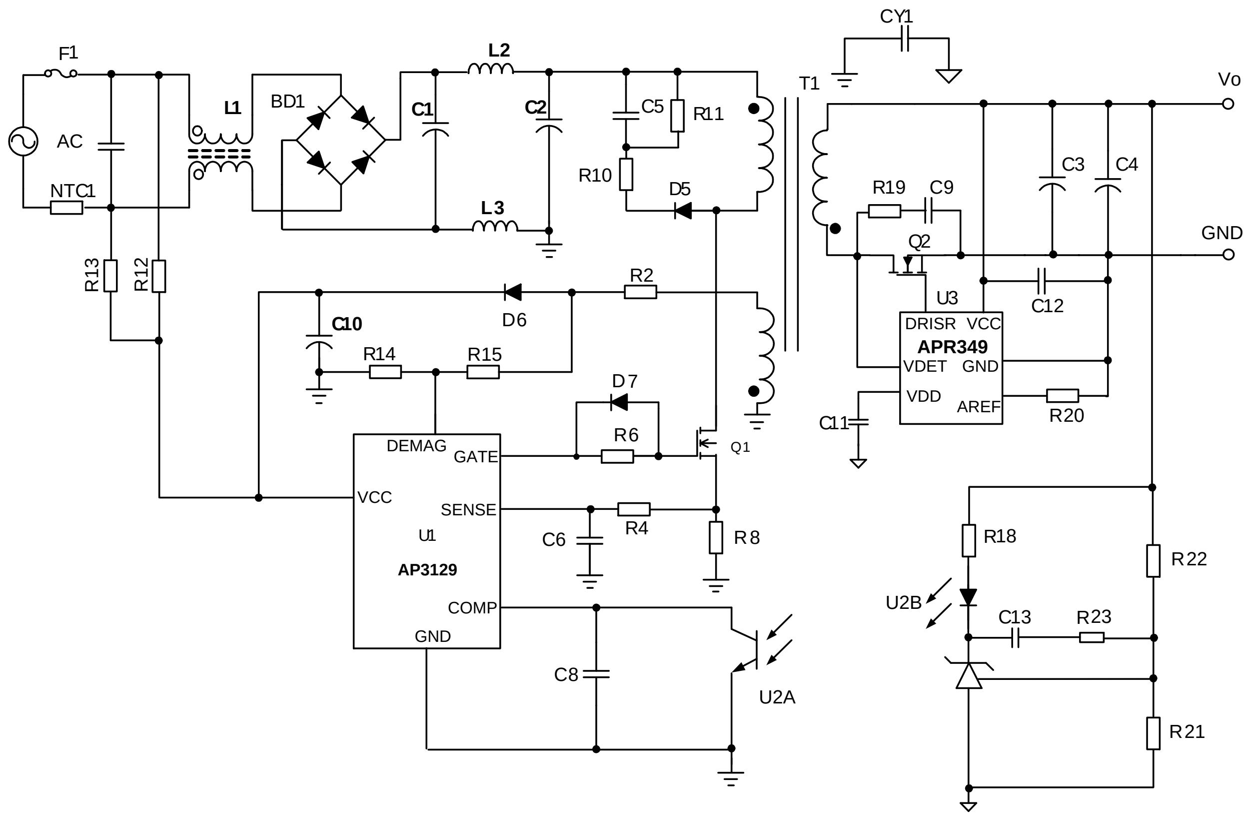
SOT26 (Type CJ)

Applications

- IoT (Internet of Thing) offline power
- Home appliances: smart speakers, AC fans, rice cookers, shavers, milk machines
- TV/Monitor standby power
- AC/DC adapters or quick chargers

Notes: 1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

Typical Applications Circuit

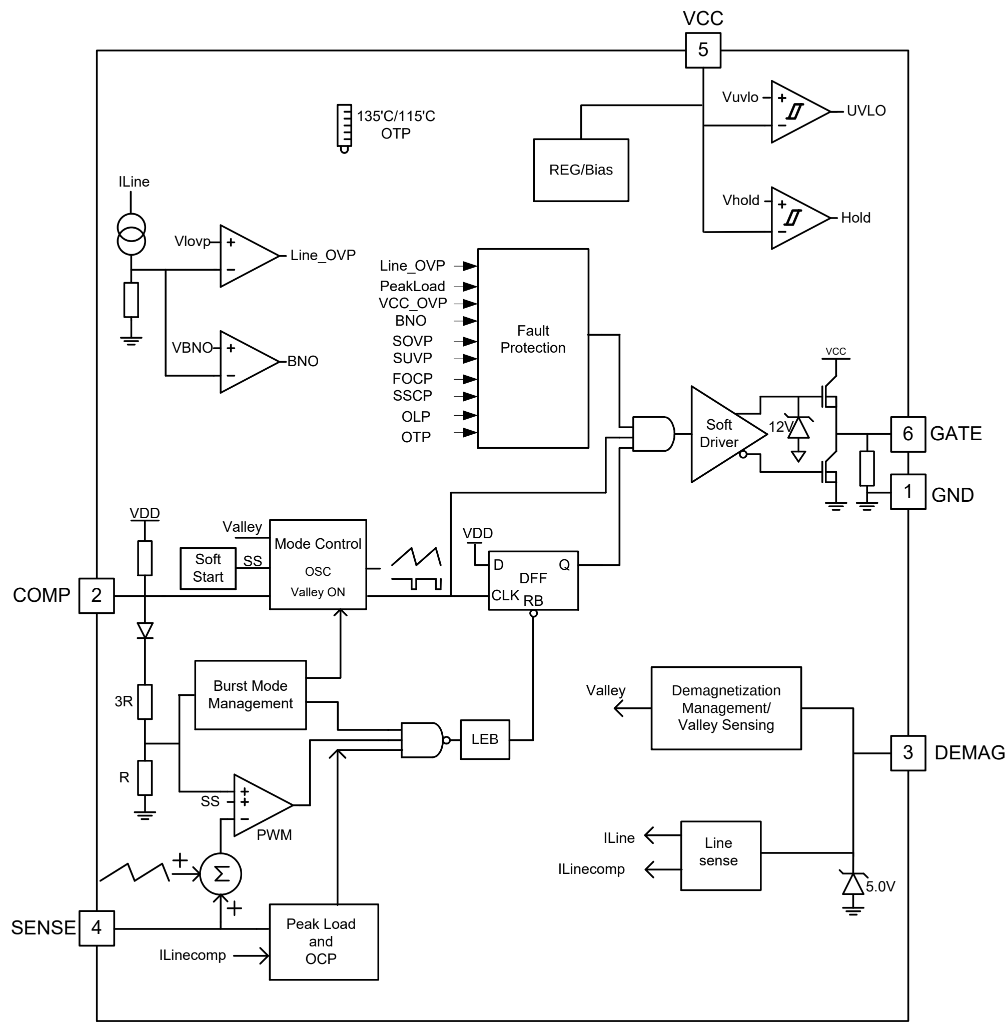


Typical Application

Pin Descriptions

Pin Number	Pin Name	Function
1	GND	Ground
2	COMP	Feedback Input. Directly Connected to the Optocoupler.
3	DEMAG	Demagnetization Input. Sense Voltage from Auxiliary Winding.
4	SENSE	Current Sense
5	VCC	Supply Voltage of Driver and Control Circuits
6	GATE	Gate Driver Output

Functional Block Diagram



Absolute Maximum Ratings (Note 4)

Symbol	Parameter	Rating	Unit
V_{CC}	Power Supply Voltage	32	V
V_{COMP}, V_{SENSE}, V_{DEMAG}	COMP, SENSE, DEMAG Pins Input Voltage (Note 5)	-0.3 to 7	V
V_{GATE}	Gate Pin Voltage (Note 5)	-0.3 to 16	V
θ_{JA}	Thermal Resistance (Junction to Ambient) (Note 6)	149	°C/W
θ_{JC}	Thermal Resistance (Junction to Case) (Note 6)	75	°C/W
P_D	Power Dissipation at T_A < +25°C	500	mW
T_J	Operating Junction Temperature	-40 to +150	°C
T_{STG}	Storage Temperature Range	-65 to +150	°C
ESD	Human Body Model	2,000	V
	Charge Device Model	800	V

Notes:
4. Stresses greater than those listed under *Absolute Maximum Ratings* can cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to *Absolute Maximum Ratings* for extended periods can affect device reliability.
5. If -0.3V to -0.5V negative voltage is applied to DEMAG/SENSE/GATE pin, the period of negative pulse is lower than 0.4µs.
6. Test condition: Device mounted on FR-4 substrate PC board, 2oz copper, with $1inch^2$ cooling area.

Recommended Operating Conditions

Symbol	Parameter	Min	Max	Unit
V_{CC}	Supply Voltage	9	26	V
T_A	Ambient Temperature	-40	+85	°C

Electrical Characteristics (@ T_A = -40°C to +85°C, V_{CC} = 18V, unless otherwise specified.)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
Supply Voltage (VCC Pin)						
V_{CC_OVP}	VCC OVP Threshold Voltage	—	26.5	28	29.5	V
V_{CC_ON}	VCC On Threshold Voltage	—	16.5	18	19.5	V
V_{CC_UVLO}	VCC UVLO Threshold Voltage	—	5.8	6.3	6.8	V
V_{CC_ET}	VCC Holdup Mode Entry Point	—	6.5	7.3	8.0	V
V_{CC_EX}	VCC Holdup Mode Exit Point	—	—	V_{CC_ET}+0.8	—	V
I_{CC_ST}	Startup Current	$V_{CC} < V_{CC\_ON}$	—	1	5	μA
I_{CC_OP}	Operating Current	V_{COMP} = 0V, I_{DEMAG} = 0mA	300	376	425	μA
		V_{COMP} = 1.2V, V_{CC} = 16V	0.75	0.9	1.15	mA
GATE Section (GATE Pin)						
V_{GATE_H}	GATE High Voltage	I_{SOURCE} = 20mA, V_{CC} = 16V	10	11.5	13.5	V
V_{GATE_L}	GATE Low Voltage	I_{SINK} = 20mA, V_{CC} = 16V	—	0.06	0.20	V
$t_{GATE\text{-}RISE}$	Rising Time	C_L = 1nF	—	350	—	ns
$t_{GATE\text{-}FALL}$	Falling Time	C_L = 1nF	—	50	—	ns
Current Sense Section (SENSE Pin)						
V_{TH_OCP1}	Threshold of OCP1 at Low Line	—	0.5	0.525	0.55	V
Rocp1	Rocp at Low Line	Idem = 500μA	31	36	41	kΩ
V_{TH_OCP2}	Threshold of OCP2 at Low Line	—	0.8	0.825	0.85	V
V_{SOCP}	Threshold Voltage of Secondary Rectifier Short Protection	—	1.2	1.25	1.3	V
Rocp2	Rocp at Low Line	—	36	41	46	kΩ
$V_{TH\text{-}SSCP}$	SSCP Voltage	—	30	50	70	mV
t_{LEB}	Leading Edge Blanking Time	—	120	240	370	ns
t_{PD}	Internal Propagation Delay Time	—	—	80	—	ns
t_{D_OCP1}	Over-Power Protection Debounce Time	(Note 7)	40	60	80	ms
t_{D_OCP2}	Peak Load Protection Debounce Time	(Note 7)	10	17	25	ms
Feedback Section (COMP Pin)						
V_{COMP_OP}	Open-Loop Voltage	COMP Pin Open-Circuited	4.0	4.5	—	V
V_{COMP_PK}	Over Peak Load Protection	—	3.6	3.9	4.25	V
R_{COMP}	Internal Pullup Resistor	—	22	27	31	kΩ
$K_{COMP\text{-}SENSE}$	The Ratio of V_{COMP} to V_{SENSE}	—	2.7	3.2	3.7	V/V
$V_{FB\text{-}PEAK\text{-}START}$	Start of Peak Frequency Rising	Low Line (Note 8)	—	3.45	—	V
		High Line (Note 8)	—	2.45	—	V
$V_{FB\text{-}PEAK\text{-}END}$	End of Peak Frequency Rising	(Note 8)	—	$V_{FB\text{-}PEAK\text{-}START}$+0.2	—	V
V_{FOLD_EN}	Frequency Foldback Enter Voltage	Low Line	—	2.05	—	V
		High Line (Note 8)	—	1.925	—	V
V_{FOLD_EX}	Frequency Foldback Exit Voltage	(Note 8)	—	V_{FOLD_EN}-0.35	—	V
V_{BURST_ENTRY}	Burst Mode Entry Voltage	Low Line	1.40	1.50	1.60	V
		High Line	1.37	1.47	1.57	V
V_{BURST_HYS}	Burst Mode Hysteresis Voltage	—	—	0.030	—	V

Notes: 7. Data measured in IC test mode.
8. Guaranteed by design.

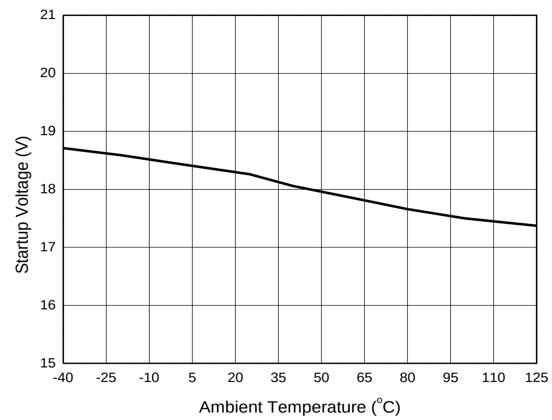
Electrical Characteristics (@ T_A = -40 to +85°C, V_{CC} = 18V, unless otherwise specified.) (continued)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
Oscillator Section						
$f_{SW\_PL\_MAX}$	Maximum Switching Frequency in Peak Load Mode	—	120	130	140	kHz
f_{SW_MIN}	Minimum Switching Frequency	—	20	22.5	25	kHz
f_{SW_CCM}	Frequency of CCM	High Line	60	65	70	kHz
		Low Line	60	65	70	
D_{MAX}	Maximum Duty for Peak Load	—	75	79	83	%
t_{MAX_ON}	Maximum t_{ON} for Valley-on Switching Mode	—	11	13.5	16	µs
DEMAG Section (DEMAG Pin)						
t_{BLK_DEMAG}	Blanking Time	(Note 8)	—	1.4	—	µs
V_{TH_OVP}	V_{OUT} OVP Threshold Voltage	—	2.7	2.8	2.9	V
V_{TH_UVP}	V_{OUT} UVP Threshold Voltage	—	0.4	0.5	0.6	V
t_{D_UVP}	Blanking Time of V_{OUT_UVP}	—	15	25	35	ms
V_{ZCD_DEMAG}	Zero Current Detection Threshold Voltage	(Note 7)	—	35	—	mV
t_{OUT}	Timeout After Last Zero Current Detection	Correlation with t_{BLK_DEMAG} (Note 8)	—	5	—	µs
$V_{CLP\text{-}L}$	Low Level for Clamping Voltage	I_{DEMAG} = -200µA	-120	-50	—	mV
$V_{CLP\text{-}H}$	High Level for Clamping Voltage	I_{DEMAG} = 1mA	4.5	5	—	V
I_{DEMAG_BNI}	Brown-In Protection Threshold Current	Correlation with I_{DEMAG_BNO} (Note 8)	—	-120	—	µA
I_{DEMAG_BNO}	Brown-Out Protection Threshold Current	—	-120	-110	-100	µA
t_{D_BNO}	Debounce Time of Brown Out	(Note 8)	—	60	—	ms
$I_{DEMAG\text{-}HLSW}$	High/Low Line Switching Threshold Current	—	225	-255	285	µA
I_{DEMAG_OVP}	Bulk OVP Protection Threshold Current	—	-770	-690	-610	µA
$t_{D\_BulkOVP}$	Delay Time of Bulk OVP	(Note 8)	—	3.0	—	s
Internal OTP Section						
OTP	OTP Enter	(Note 8)	—	+135	—	°C
	OTP Exit	(Note 8)	—	+115	—	°C

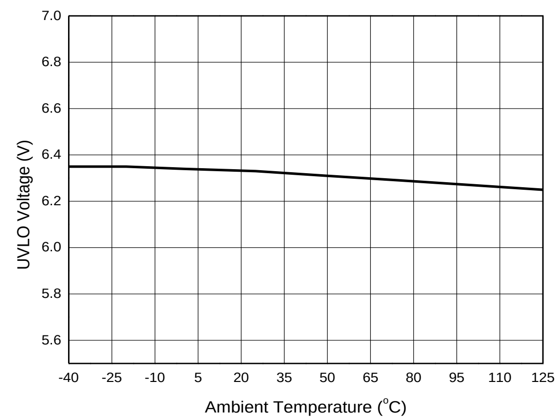
Notes: 7. Data measured in IC test mode.
8. Guaranteed by design.

Performance Characteristics

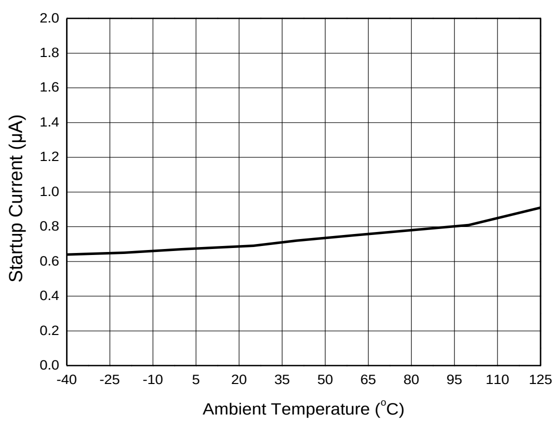
V_{CC_ON} Threshold vs. Ambient Temperature



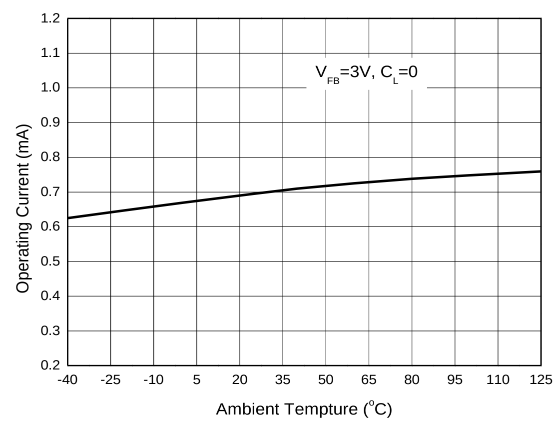
V_{CC_UVLO} Threshold vs. Ambient Temperature



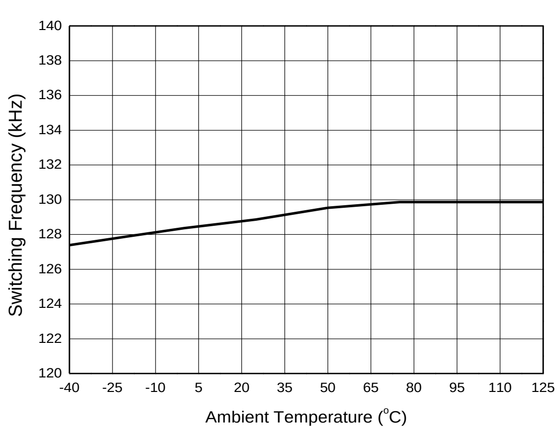
I_{CC_ST} Startup Current vs. Ambient Temperature



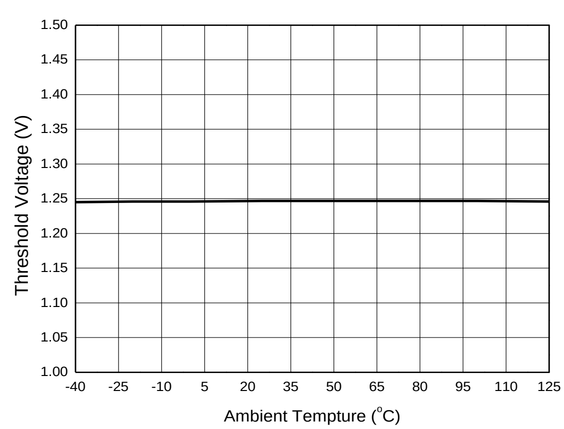
I_{CC_OP} Operating Current vs. Ambient Temperature



Maximum Switching Frequency in Peak Load vs. Ambient Temperature



Threshold Voltage of Secondary Rectifier Short Protection vs. Ambient Temperature



Operation Description

The AP3129 implements a multi-mode flyback converter utilizing peak current control the switch off event. It operates in continuous condition mode (CCM) and valley-on switching to provide high-efficiency solution. The IC is an ideal candidate where low parts count and cost effectiveness are the key parameters in AC-DC adapters.

Startup Timing

VCC capacitor charging current comes from divided resistor for X-CAP discharging in AC input terminal. When the VCC is rising up to the startup voltage (V_{CC_ON}), the current source turns off. And the AP3129 will output 4 switching pulses to detect the I_{DEMAG} current flowing through the DEMAG pin pullup resistor. Thus, the AC line voltage can be detected. If the input voltage is lower than the brown-in voltage, the IC will enter into restart status. Once the input voltage is higher than the brown-in voltage, the AP3129 will start working, the output voltage will ramp up, and the auxiliary winding voltage is going up accordingly. The V_{CC} voltage begins going down from V_{CC_ON} till VCC capacitor charging is taken over by the auxiliary winding voltage.

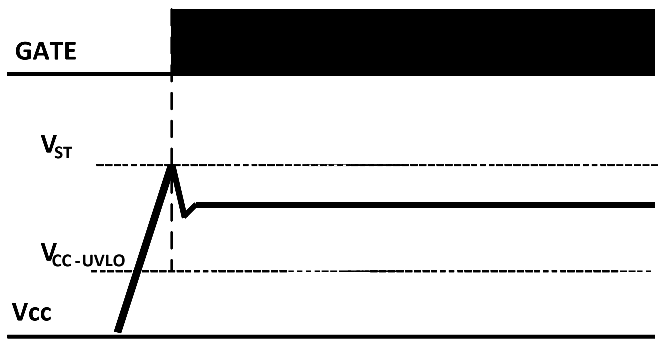


Figure 1. Startup Timing

Frequency Control Strategy

As shown in Figure 2, the AP3129 changes operating modes according to different load conditions. When the device operates in CCM mode in heavy load in low line voltage, it is advantageous to achieve high power conversion efficiency, and is possible to implement a small-sized adapter with a small transformer. There are some special applications (smart speakers, printers, etc.) where the output load heavily changes from a normal to a peak value. At this time, to avoid growing the transformer size, an optional technique consists in clamping the peak current up to a maximum value, and authorizes frequency increase to a certain point (130kHz) to let the converter deliver more power to output. This power excursion can only be temporary and its duration is set by the internal overload timer

When the loading goes low, the system enters into QR mode or green mode with valley-on switching, and it can significantly reduce switching loss, especially in high line. Thus, high power conversion efficiency can be achieved. In order to avoid an excessive switching loss at very high switching frequency operations, there is a fixed 80kHz frequency limitation. As the load decreases, the internal oscillators reduce its switching frequency according to the feedback level. Once the COMP pin voltage is lower than V_{BURST_ENTRY}, the controller enters burst mode, and the peak current freezes to a fixed value. Operating in this mode ensures high efficiency at low power and excellent no-load power performance. A minimum clamp frequency will prevent the switching frequency from dropping below 22kHz to eliminate the risk of audible noise.

Operation Description (continued)

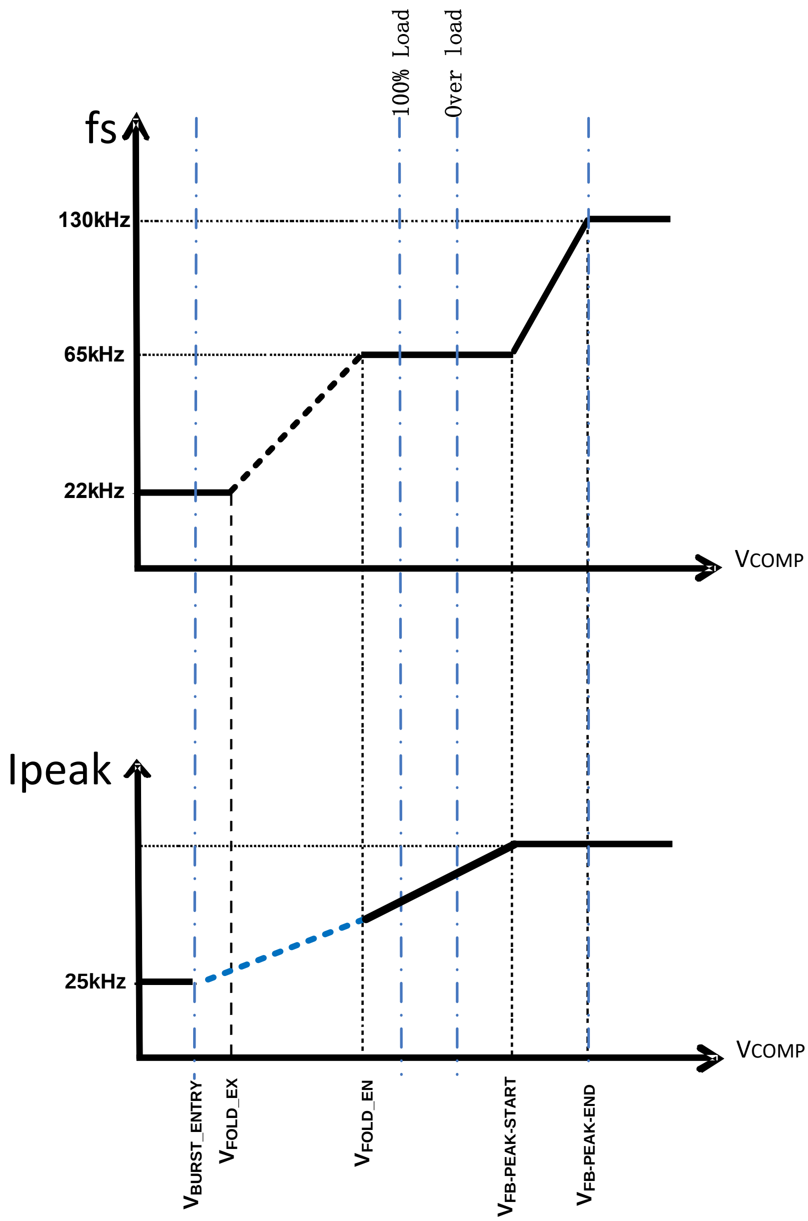


Figure 2. Operation Frequency Curve

Valley-On Switching

Valley-on switching is regarded as a soft switching technology which always turns on the primary MOSFET at the valley status of the Drain-to-Source voltage (V_{DS}). Compared to traditional hard switching, it can reduce the switching power loss of MOSFET and achieve good EMI behavior without additional BOM cost.

Operation Description (continued)

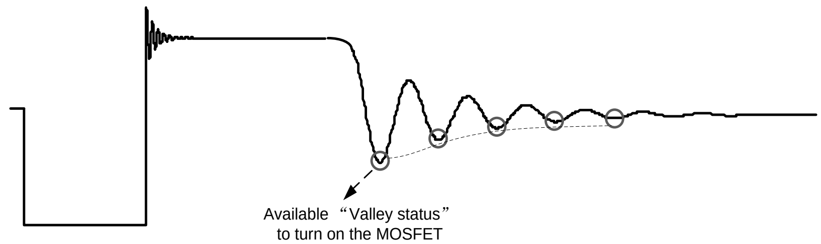


Figure 3. Valley Detection

Figure 3 shows the primary MOSFET V_{DS} waveform. When the secondary-side current drops to zero, the primary inductance L_M and the effective MOSFET output capacitor C_{OSS} begins to resonant. The resonant frequency is approximately $1/2\pi\sqrt{LM * Coss}$. The IC controller takes advantage of the drain voltage ringing and turns on the power switch at the drain ringing voltage valley to reduce switching loss and EMI. The valley is detected by the DEMAG pin through a pair of voltage dividers. At the primary MOSFET turning-off time once the voltage on the DEMAG pin is detected below 35mV, one "valley status" is counted. According to the frequency control strategy of the AP3129, one proper "valley status" will be selected to turn on the MOSFET. To prevent a false-trigger of the V_{DS} ring caused by a leakage inductance, the valley detection function is blanked within the t_{BLK_DEMAG} when the primary MOSFET turns off. When the COMP voltage decreases, the current "valley-on status" is forced to shift to another available "valley-on status". The maximum valley number for turn-on reaches to the tenth. When the valley quantities exceed tenth valleys, the system will operate in hard switching conditions.

Frequency Jittering

The AP3129 integrates an active frequency-dithering function to improve the EMI performance. As shown in Figure 4, an internal low frequency modulation signal varies the pace at which the oscillator frequency is modulated, and produces a periodical excursion. This helps spread out energy in conducted noise analysis. To improve the EMI performance during low power and middle power level, the jittering circuit persists in working in frequency foldback mode because of an innovative implementation of the AP3129.

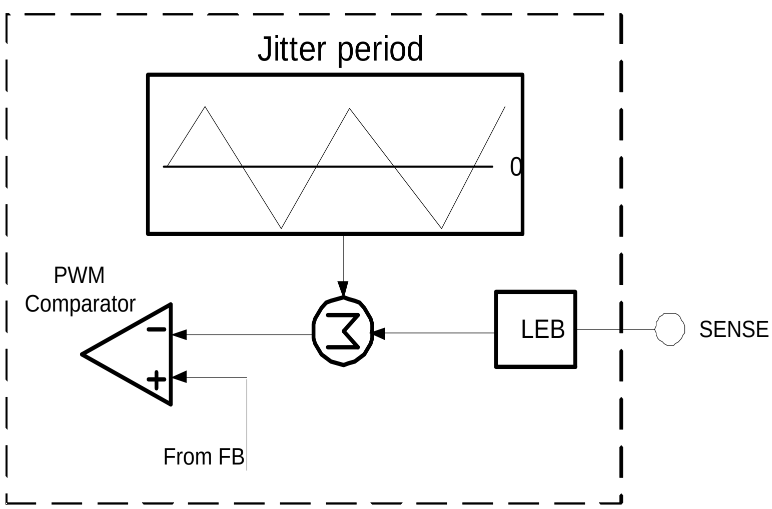


Figure 4. Frequency Jittering

Operation Description (continued)

VOUT OVP & UVP

The AP3129 provides output OVP and UVP protection function. The auxiliary winding voltage during secondary rectifier conducting period reflects the output voltage. A divided voltage network is connected to the auxiliary winding and DEMAG pin. The DEMAG pin will detect the equivalent output voltage with a delay of t_{BLK_DEMAG} from the falling edge of the GATE driver signal, as shown in Figure 5. The detected voltage will be compared to the inner SOVP and SUVP threshold voltage. If the SOVP or SUVP threshold is reached continuously by 6 switching cycles, the SOVP or SUVP protection will be triggered, the AP3129 will shut down switching pulses, and the system will restart when the V_{CC} voltage falls below the UVLO voltage.

To prevent a false-trigger of the SUVP during startup process, the SUVP protection function will be ignored for a blank time of t_{D_UVP}.

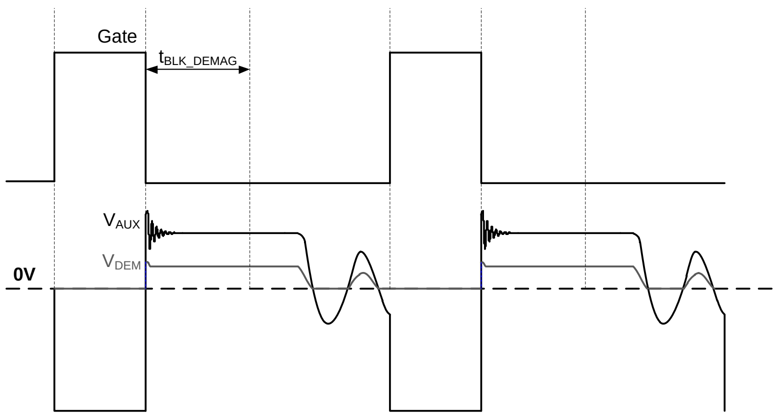


Figure 5. SOVP and SUVP

Soft Driver

The AP3129 gate sinking current is higher than 600mA, and the drive control includes three steps (see Figure 6). The first step is from 0V to 2V driving voltage, and the second step is from 2V to 6V within a period of 250ns. The third step is from 6V up to the gate clamp voltage. For the first-step and third-step, the gate voltage will be charged rapidly in a remarkable short time, which makes the MOSFET switching loss drop to a relatively low level. And the second step is expected to hold 250ns to get a relative long Miller time for improving EMI performance. This driver solution is a good balance of EMI performance and efficiency.

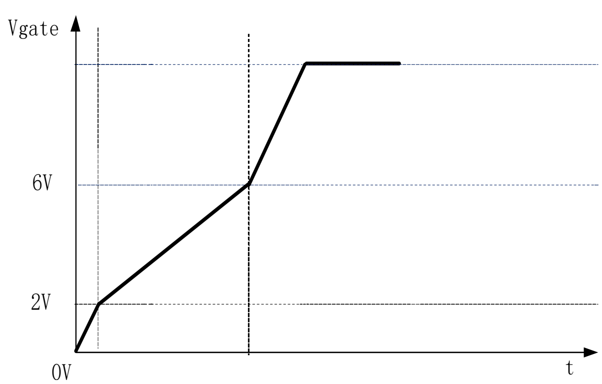


Figure 6. Soft Driver

Operation Description (continued)

Overload Protection (OCP1/OCP2)

An integrated overload protection circuit provides a relatively constant power limit across over the whole line voltage. As shown in Figure 5, during the turn-on time, the Vaux drops to –N*VIN, N being the turns ratio between the primary winding and the auxiliary winding and VIN being the input bulk voltage. The negative plateau voltage of the DEMAG pin has a proportion amplitude of the input voltage, so an integrated sensing circuit in AP3129 measures the input bulk voltage via the DEMAG pin. As the output power of system reaches a defined set limit, the corresponding V_{SENSE} should touch an internal overpower reference voltage (V_{TH_OCP1}). If the overload situation lasts continuously for 60ms, an overload protection circuit would be triggered and the system would enter into restart mode.

If the output power and the feedback voltage continue to rise up, AP3129 would authorize a transient peak load with a higher V_{SENSE} threshold (V_{TH_OCP2}) and a higher switching frequency (130kHz) for a period of 60ms. When the feedback voltage reaches up to the open-loop level (V_{COMP_OPEN}), which lasts more than 15ms, the device will enter an auto-recovery hiccup status. If the fault situation lasts less than set-time 15ms, the feedback will returns to its regulation level and resets the timer of peak-load-control circuit.

Line Compensation

A higher OCP current often occurs along with turn-off delay time of the MOSFET at high line voltage. To obtain a constant OCP current value with universal input voltage, an effective line compensation circuitry must be applied to the AP3129. The function block is illustrated in Figure 7. The current I_{DEMAG}, which reflects line voltage, is scaled down and inversed to I_{L_OPP} within the AP3129, this I_{L_OPP} flows through the inner compensation resistor R_{OPP} and an external filtering resistor R_F. The final line compensation voltage is formed as:

$$V_S = V_{REF1} - I_{L\_OPP} * (R_{OPP} + R_F), \quad (I_{L\_OPP} = \frac{Vindc*Naux}{Np*Rdem*K})$$

Where, V_S is the sense voltage of R_S, “K” is the current proportional coefficient, and R_{OPP} is decided by line voltage.

R_{DEM} value is relevant with brown-in/out voltage, which is fixed (105kΩ recommended) to specific turn-ratio transformer system.

In a real system, the line compensation can be checked according to OCP1 under 115Vac line voltage condition. The corresponding parameters are set by V_{REF1} = 0.525V, K = 24, R_{OPP} = 40kΩ, R_F = 1kΩ

As is indicated from the above formula, when the V_{REF1} and R_{DEM} values are fixed, changing R_F is an alternative way to adjust the line compensation, especially at high line voltage. Once the R_F value is confirmed, it also needs to adjust the C_F simultaneously to offer enough RC time to filter the spike on the SENSE pin.

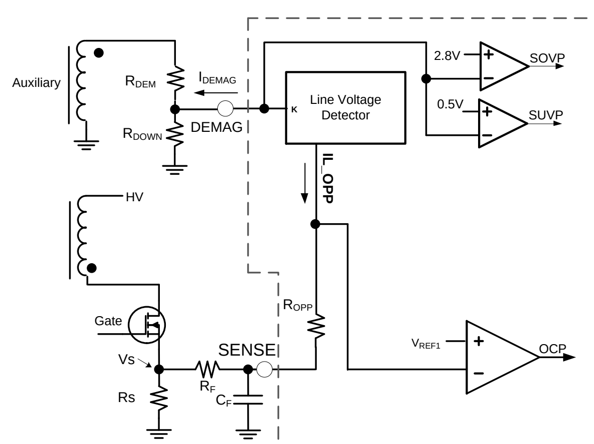


Figure 7. Line Compensation

Operation Description (continued)

Slope Compensation

The primary current is followed by the COMP voltage. When the primary peak current reaches the reference determined by V_{COMP}, the gate driver will be turned off. In order to avoid sub-harmonic oscillation, slope compensation is essential for peak-current mode when the duty cycle is above 50%. Even though the duty is below 50%, it is desirable to add a slope compensation to decrease the influence of external noise. The AP3129 offers an internal slope compensation signal (typically 33mV/µs) that can easily be summed up to the sensed current. Sub harmonic oscillations can thus be compensated. This allows the AP3129 to work with a wide input voltage.

Overtemperature Protection

The AP3129 integrates an internal temperature protection to prevent permanent damage by overtemperature. If the junction temperature exceeds the temperature protection threshold of +130°C, the IC will trigger the internal OTP and stop switching. Meanwhile, if the VCC drops to VCC UVLO threshold V_{CC_UVLO}, the controller enters restart mode. A built-in hysteresis ensures that if the internal temperature drops to +115°C, the IC will recover operation.

Others System Protection

V_{BULK_OVP}, FOCP, SSCP, VCC OVP, SCP

The AP3129 provides versatile protections to ensure the reliability of the power system. V_{BULK_OVP} represents line voltage overvoltage protection. If the detected AC line voltage is higher than V_{BULK_OVP} and sustains for 2.8s, the V_{BULK_OVP} protection will be triggered.

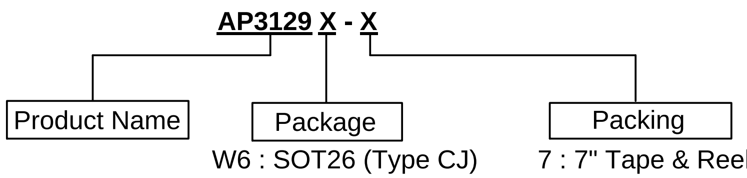
FOCP (Fast overcurrent protection) is an ultra-fast short-current protection which is helpful to prevent catastrophic damage of the system when the secondary rectifier is shorted. The primary peak current will be monitored by the SENSE pin through a primary sense resistor. Whenever the sampled voltage reaches the threshold of $V_{TH\text{-}FOCP}$ for 6 switching cycles continuously, the FOCP will be activated to shut down the switching pulse.

SSCP (Sensor short-circuit protection) might be triggered when the SENSE pin is shorted to the ground. The SSCP module senses the voltage across the primary sense resistor with a several microsecond delay time after the rising edge of the primary GATE signal. This sensed signal is compared with $V_{TH\text{-}SSCP}$. If it is lower than $V_{TH\text{-}SSCP}$ for 6 switching cycles, the SSCP will be triggered and the drive signal will be disabled. To prevent a false-trigger, the SSCP is valid only within the initial 25ms after startup.

VCC overvoltage protection is used to prevent IC damage from overvoltage stress. All these protections described will restart the system when the V_{CC} voltage falls below UVLO.

If the power supply experiences a severe overloading situation or the output of the system is under a short-circuit test, the driving pulses will stop and V_{CC} will fall down as the auxiliary pulses are missing. When V_{CC} drops below V_{CC_UVLO}, the controller consumption is down to a few µA and V_{CC} slowly rises up again via resistive starting network. When V_{CC} reaches up to V_{CC_ON}, the controller purposely ignores the restart cycle and waits for another V_{CC} cycle. AP3129 naturally reaches a remarkable low input power by lowering the duty ratio in fault condition.

Ordering Information

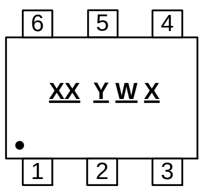


Part Number	Package	Identification Code	Packing	
			Qty.	Carrier
AP3129W6-7	SOT26 (Type CJ)	B4	3000	Tape & Reel

Marking Information

Package Type: SOT26 (Type CJ)

(Top View)

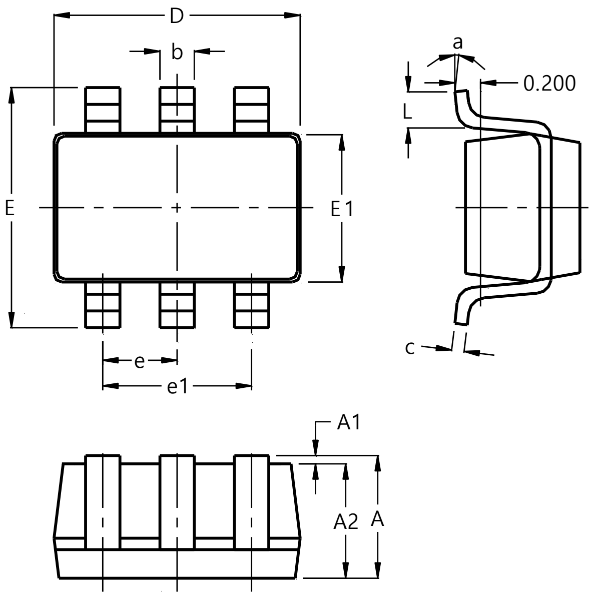


XX : Identification Code
Y : Year 0 to 9 (ex: 3 = 2023)
W : Week : A to Z : week 1 to 26;
a to z : week 27 to 52; z represents
week 52 and 53
X : Internal Code

Package Outline Dimensions

Please see http://www.diodes.com/package-outlines.html for the latest version.

SOT26 (Type CJ)

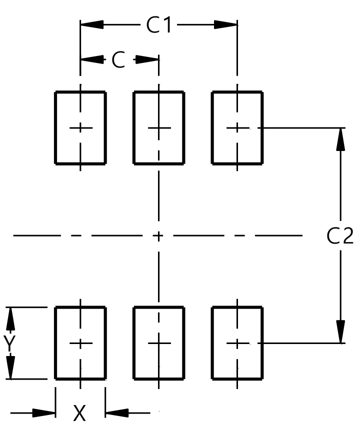


SOT26 (Type CJ)			
Dim	**Min**	**Max**	**Typ**
A	1.050	1.250	--
A1	0.00	0.10	--
A2	1.050	1.150	--
b	0.300	0.500	--
c	0.100	0.200	--
D	2.820	3.020	--
E	2.650	2.950	--
E1	1.500	1.700	--
e	0.950BSC		
e1	1.800	2.000	--
L	0.300	0.600	--
a	0°	8°	--
All Dimensions in mm			

Suggested Pad Layout

Please see http://www.diodes.com/package-outlines.html for the latest version.

SOT26 (Type CJ)



Dimensions	Value (in mm)
C	0.95
C1	1.90
C2	2.40
X	0.60
Y	1.00

Mechanical Data

- Moisture Sensitivity: Level 3 per JESD22-A113
- Terminals: Finish – Matte Tin Plated Leads, Solderable per JESD22-B102 e3
- Weight: 0.016/0.017 grams (Approximate)

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