Description

The AP43771V is a highly integrated USB Type-C® power delivery controller targeted for USB Type-C adapter and charger application. It is compatible with Qualcomm® QC4/4+/QC5 protocol, which supports USB power delivery specification Rev3.1 V1.2 (including optional PPS support).

The AP43771V can support PPS APDO (Augmented Power Data Object) with 20mV/step voltage resolution and 50mA/step current resolution for power management. Also embedded is cable-loss compensation and SOP command for e-Marker detection.

The AP43771V can provide a robust protection scheme with built-in OVP/OCP/SCP/OTP features.

Dedicated part number AP43771VFBZ-13-FR01 (W-DFN3030-14 (Type A1)) with standard firmware provides a preloaded 8-power-profile menu. System manufacturers could easily select a desired power profile (Constant Voltage CV and Constant Current CC) through a single resistor attached to the relevant pin (OTP pin) to meet output power requirements of a USB PD charger or adaptor.

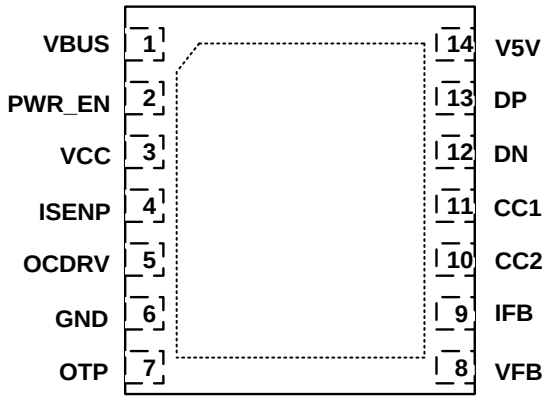
Supporting emerging multiple Type-C PD applications, the AP43771V (W-QFN4040-24 (Type A1)) with customized firmware can be used for implementing smart power sharing scheme. It monitors status of other I2C interface connected ports and leverages the embedded MCU for command execution through I2C interface to re-allocate desired power profile for each Type-C port.

Features

- Compatible with USB PD Rev3.1 V1.2
- USB-IF PD Certificated with TID: 4305
- Qualcomm QC4/4+/QC5 Protocol Certificated (QC20201127203)
- 16kB OTP (One-Time Programmable) Memory
- Built-in Regulator for CV and CC Control
- Support SCP/OTP/OVP/UVP with Auto Restart
- Support Power Saving Mode
- Driver for Output Enable nMOS Switch
- Current Sensing with 10mΩ Resistance for Better Efficiency
- Support E-Marker Cable Detection
- Support I2C Interface (W-QFN4040-24 (Type A1) Only)
- Operating Voltage Range: 3.3V to 24V
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**
- **For automotive applications requiring specific change control (i.e. parts qualified to AEC-Q100/101/104/200, PPAP capable, and manufactured in IATF 16949 certified facilities), please contact us or your local Diodes representative. https://www.diodes.com/quality/product-definitions/**

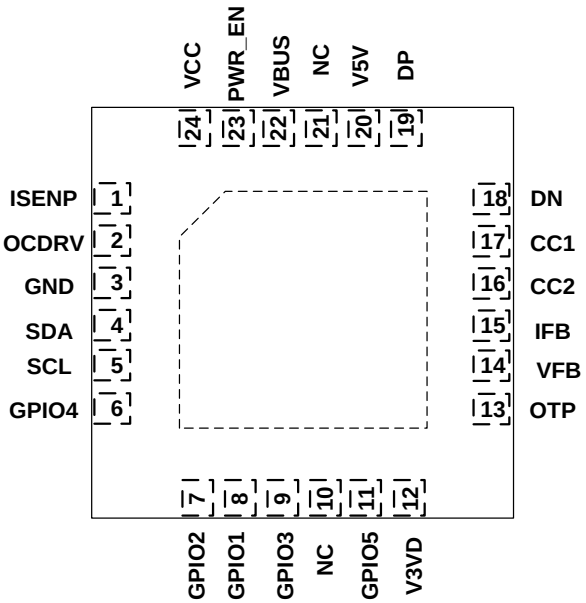
Pin Assignments

(Top View)



W-DFN3030-14 (Type A1)

(Top View)



W-QFN4040-24 (Type A1)

Applications

- Type-C USB adapters/chargers
- USB PD converters

Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

Typical Applications Circuit

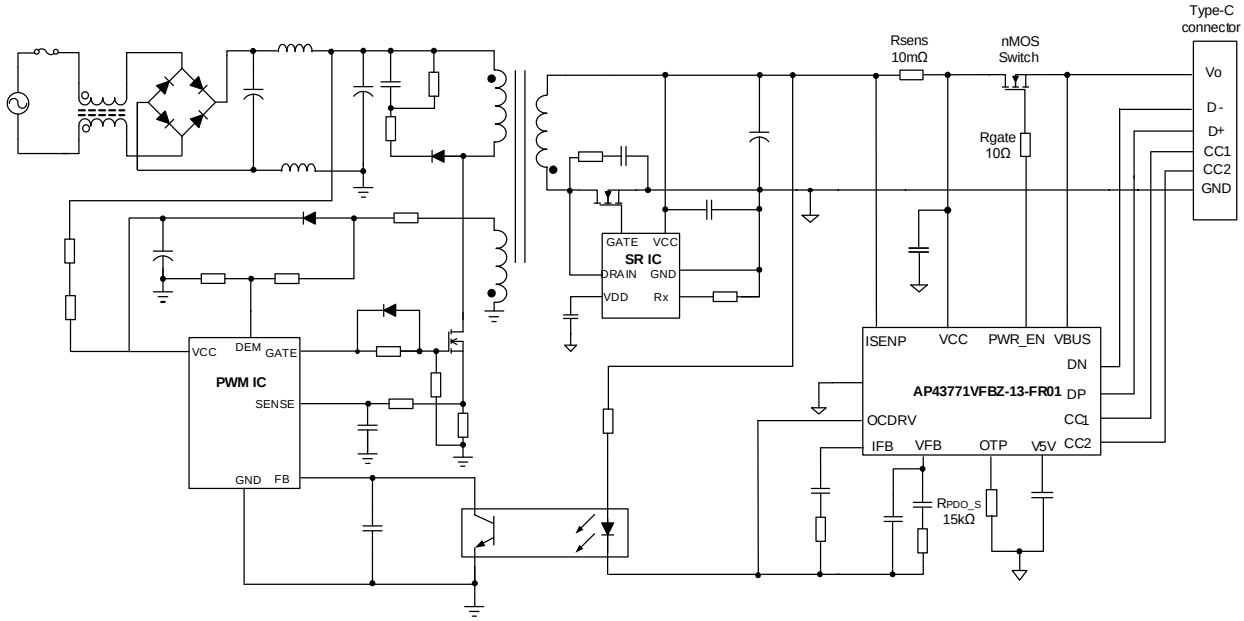


Figure 1. Traditional 65W Single Type-C Port USB PD Charger Application with AP43771VFBZ-13-FR01 (Standard Firmware Inside)

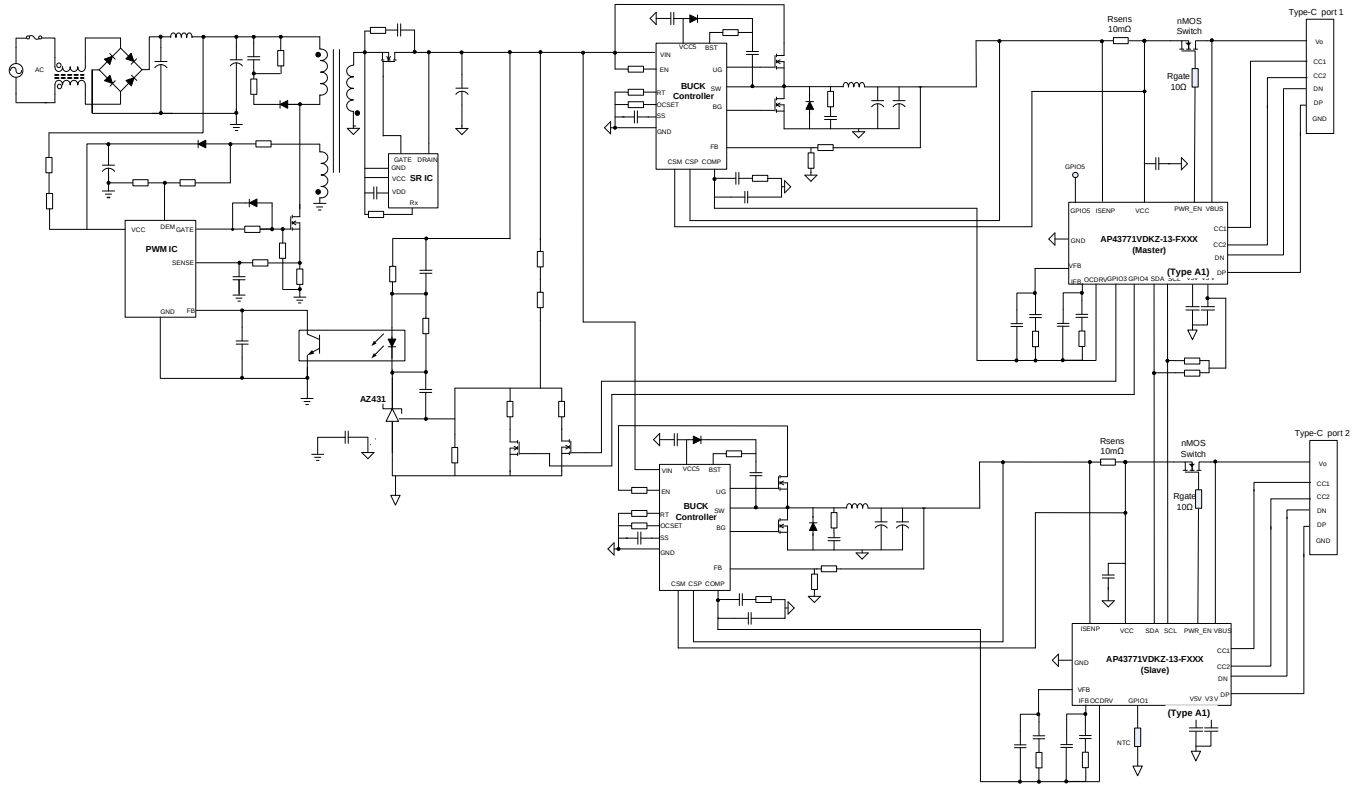


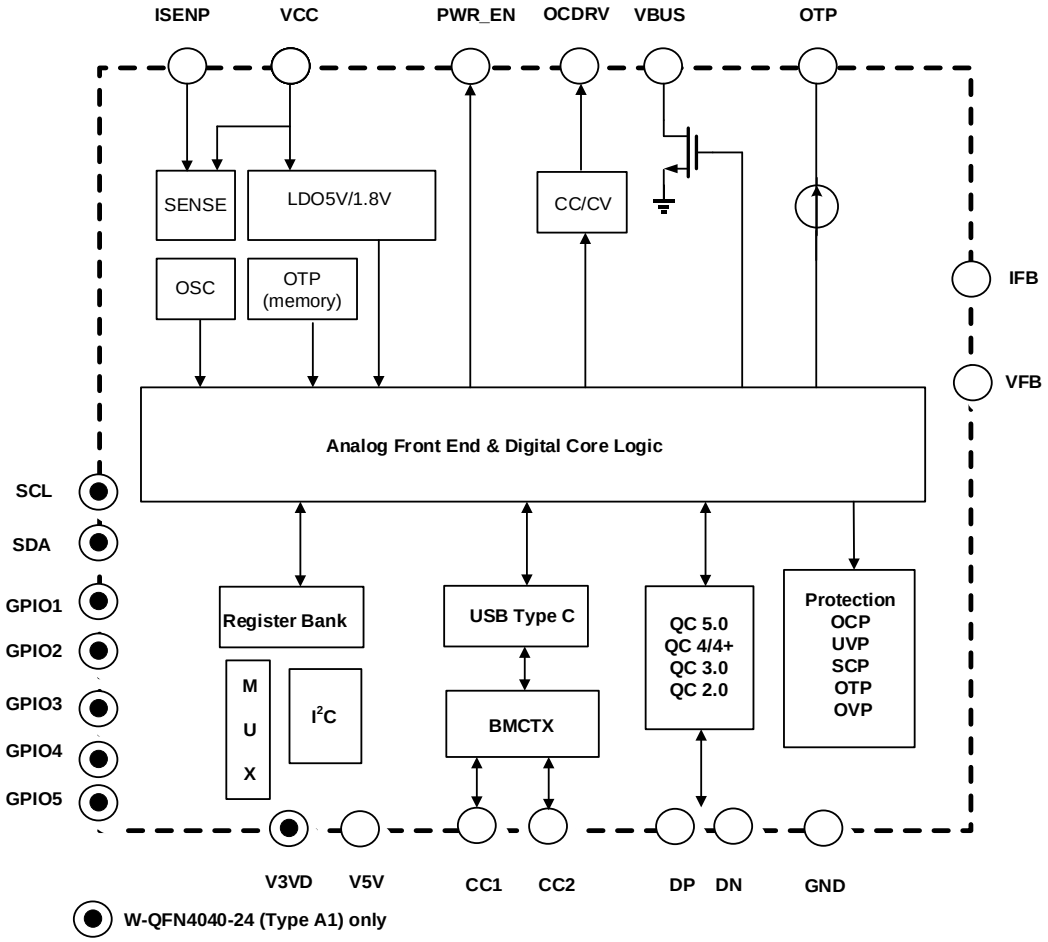
Figure 2. Dual C-Ports USB PD Charger Application with AP43771VDKZ-13-FXXX (Customized Firmware Inside)

Pin Descriptions

W-DFN3030-14 (Type A1)		Function
Pin Number	Pin Name	
1	VBUS	Output Terminal for Discharge Path.
2	PWR_EN	nMOS Switch gate control to switch the nMOS on or off.
3	VCC	The Power Supply of the IC. A 1μF cap is required to connect this pin to GND pin.
4	ISENP	Current Sense Positive Node, connect to the positive node of the external current sensing resistor.
5	OCDRV	CC/CV Output. Open-Drain Output for Optocoupler.
6	GND	Ground
7	OTP	Functional option 1: 100μA Current Source output for NTC connected to ground. This NTC is used to monitor temperature variation. Functional option 2: for dedicated part number AP43771VFBZ-13-FR01, connect a resistor to ground for selecting a desired power profile.
8	VFB	CV Input. Negative Node of CV OPAMP for Optocoupler.
9	IFB	CC Input. Negative Node of CC OPAMP for Optocoupler.
10	CC2	Type-C Configuration Channel 2 (CC2). The CC2 pin detects, configures, and manages the connections across a USB Type-C cable.
11	CC1	Type-C Configuration Channel 1 (CC1). The CC1 pin detects, configures, and manages the connections across a USB Type-C cable.
12	DN	Type-C_DN
13	DP	Type-C_DP
14	V5V	Output of the internal 5V LDO with VCC as input. A 1μF cap is required to connect this pin to GND.

W-QFN4040-24 (Type A1)		Function
Pin Number	Pin Name	
1	ISENP	Current Sense Positive Node, connect to the positive node of the external current sensing resistor.
2	OCDRV	CC/CV Output. Open-Drain Output for Optocoupler.
3	GND	Ground
4	SDA	I2C Data, need to be pulled up externally.
5	SCL	I2C Clock, need to be pulled up externally.
6	GPIO4	General-Purpose Input or Output
7	GPIO2	General-Purpose Input or Output
8	GPIO1	General-Purpose Input or Output
9	GPIO3	General-Purpose Input or Output
10	NC	No Connection
11	GPIO5	General-Purpose Input or Output
12	V3VD	Output of the internal 3V LDO, connect to a ceramic capacitor.
13	OTP	100μA Current Source output for NTC connected to ground. This NTC is used to monitor temperature variation.
14	VFB	CV Input. Negative Node of CV OPAMP for Optocoupler.
15	IFB	CC Input. Negative Node of CC OPAMP for Optocoupler.
16	CC2	Type-C Configuration Channel 2 (CC2). The CC2 pin detects, configures, and manages the connections across a USB Type-C cable.
17	CC1	Type-C Configuration Channel 1 (CC1). The CC1 pin detects, configures, and manages the connections across a USB Type-C cable.
18	DN	Type-C_DN
19	DP	Type-C_DP
20	V5V	Output of the internal 5V LDO with VCC as input. A 1μF cap is required to connect this pin to GND.
21	NC	No Connection
22	VBUS	Output Terminal for Discharge Path.
23	PWR_EN	nMOS Switch gate control to switch the nMOS on or off.
24	VCC	The power supply of the IC. A 1μF cap is required to connect this pin to GND pin.

Functional Block Diagram



Absolute Maximum Ratings (Note 4)

Symbol	Parameter	Rating		Unit
V_{CC}	Input Voltage at VCC Pin	-0.3 to 24		V
V_{FB}, V_{IFB}, V_{OTP}	Input Voltage at VFB, IFB, OTP Pins	-0.3 to 7		V
V_{BUS}, V_{PWR_EN}, V_{ISENP}, V_{OCDRV}	Input Voltage at VBUS, PWR_EN, ISENP, OCDRV Pins	-0.3 to 24		V
—	Voltage from PWR_EN to VCC Pin	-16 to 7		V
V_{V5V}	Input Voltage at V5V Pin	-0.3 to 7		V
V_{CC1}, V_{CC2}	Input Voltage at CC1, CC2 Pins	-0.3 to 7		V
V_{DP}, V_{DN}	Input Voltage at DP, DN Pins	-0.3 to 7		V
V_{GPIO1} - V_{GPIO5}, V_{SDA}, V_{SCL}	Input Voltage at GPIO1-5, SDA, SCL Pins (Note 5)	-0.3 to 5		V
T_J	Operating Junction Temperature	-40 to +150		°C
T_{STG}	Storage Temperature	-65 to +150		°C
T_{LEAD}	Lead Temperature (Soldering, 10s)	+300		°C
θ_{JA}	Thermal Resistance (Junction to Ambient) (Note 6)	W-DFN3030-14 (Type A1)	54	°C/W
		W-QFN4040-24 (Type A1)	28	
θ_{JC}	Thermal Resistance (Junction to Case) (Note 6)	W-DFN3030-14 (Type A1)	34	°C/W
		W-QFN4040-24 (Type A1)	16	
—	ESD (Human Body Model) Voltage on DP, DN Pins	6		kV
—	ESD (Human Body Model) Voltage on VBUS, ISENP, PWR_EN, VCC, OCDRV, OTP, V5V, IFB, VFB, CC1, CC2 Pins	2		kV
—	ESD (Charged Device Model)	750		V

Notes:
4. Stresses greater than those listed under *Absolute Maximum Ratings* can cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to *Absolute Maximum Ratings* for extended periods can affect device reliability.
5. When GPIO1-5, SDA, SCL pins are pulled high to a voltage source, it is strongly recommended to series a resistor with minimum 10k value.
6. Test condition: device mounted on FR-4 substrate PC board, 2oz copper, with the minimum footprint.

Recommended Operating Conditions

Symbol	Parameter	Min	Max	Unit
V_{CC}	Power Supply Voltage	3.3	24	V
T_{OP}	Operating Temperature Range	-40	+85	°C

Electrical Characteristics (@T_A = +25°C, unless otherwise specified.)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
VCC PIN SECTION						
V_{ST}	Startup Voltage	—	2.5	2.8	3.2	V
V_{UVLO}	Minimum Operating Voltage	—	2.4	2.7	3	V
V_{CC_HYS}	V_{CC} Hysteresis (V_{ST}-V_{UVLO})	—	0.05	—	—	V
$I_{CC\_DEEP\ SLEEP}$	V_{IN} Current in Deep Sleep Mode	CC1/2 Detach after 3s V_{CC} = 5V	—	550	900	μA
I_{CC_OPR}	Operating Supply Current	V_{CC} = 5V	—	3.3	6	mA
VOLTAGE CONTROL LOOP SECTION						
V_{REF_CV5}	Reference Voltage for 5V CV Control	—	4.85	5	5.15	V
V_{REF_CV9}	Reference Voltage for 9V CV Control	—	8.73	9	9.27	V
V_{REF_CV12}	Reference Voltage for 12V CV Control	—	11.64	12	12.36	V
V_{CABLE}	Cable Compensation (Note 7)	—	22	32	42	mV/A
I_{OS}	Maximum OCDRV Pin Sink Current	V_{OUT} = 5V	10	16	30	mA
PROTECTION FUNCTION SECTION						
V_{OVP5V}	OVP_5V Enable Voltage (Note 8)	—	5.6	6	6.8	V
V_{OVP9V}	OVP_9V Enable Voltage (Note 8)	—	9.9	10.8	12.1	V
V_{OVP12V}	OVP_12V Enable Voltage (Note 8)	—	13.2	14.4	16.2	V
$t_{DEBOUNCE\_OVP}$	OVP Debounce Time (Note 9)	—	—	90	—	ms
V_{UVP5V}	UVP_5V Enable Voltage	—	3.3	3.7	4.4	V
V_{UVP9V}	UVP_9V Enable Voltage	—	5.9	6.8	7.7	V
V_{UVP12V}	UVP_12V Enable Voltage	—	7.9	9.1	10	V
I_{OVD}	Overvoltage Discharge Current	V_{CC} = 5V	150	200	250	mA
t_{OCP}	OCP Deglitch Time (Note 10)	—	—	30	—	ms
$t_{RESTART\_INTERVAL\_SCP}$	Restart Interval Time under SCP (Note 10)	—	—	0.8	—	s
T_{OTP}	Internal OTP Temperature (Note 10)	—	—	+140	—	°C
$I_{OTP\_EXTERNAL}$	External OTP Current	—	90	100	110	μA
T_{HYS}	OTP Recovery Hysteresis Temperature (Note 10)	—	—	+25	—	°C
t_{SLEEP}	Enter Sleep Mode Time after Cable Detached (Note 10)	—	—	3	—	s
t_{OV_DELAY}	Delay from OVP Threshold Trip to nMOS Gate Turn-Off (Note 10)	—	—	—	50	μs
t_{UV_DELAY}	Delay from UVP Threshold Trip to nMOS Gate Turn-Off (Note 10)	—	—	30	—	ms
CC1/CC2, DP/DN PIN SECTION						
V_{L_RD3A}	Low-Voltage Threshold Used to Distinguish R_D Attached or Detached for 3A Delivery	—	—	1.35	—	V
V_{H_RD3A}	High-Voltage Threshold Used to Distinguish R_D Attached or Detached for 3A Delivery	—	—	2.0	—	V
I_{RD3A}	CC1/CC2 Current Source for 3A Advertisement	V_{CC} = 5V	304	330	356	μA
V_{OVP_DN}	DN Line Overvoltage Protection Threshold	—	4.1	4.5	4.8	V
V_{OVP_DP}	DP Line Overvoltage Protection Threshold	—	4.1	4.5	4.8	V

Notes:
7. Cable compensation voltage can be adjusted by setting from 0 to $V_{CABLE * N}$ (N: 0 to 7).
8. 120% OVP setting & 76% UVP setting.
9. OVP blanking time during V_O transition from high output voltage to low output voltage, such as 9V to 5V, or 12V to 5V.
10. Guaranteed by design.

Performance Characteristics

AP43771V Overview

The AP43771V is a protocol controller integrated with 8-bit 1T 8051 compatible MCU. It is compliant with the USB Power Delivery (PD) specification Rev3.0 supporting full range of Programmable Power Supply (PPS) up to 21V. It also supports USB BC1.2 and covers quick charger protocols which are implemented by High Voltage Dedicated Charging Port (HVDCP).

System Power-On Sequence

Once provided an external power source, the AP43771V will wake up, and the USB PD controller and MCU will be initialized. All analog control blocks will be ready and waiting for the PD negotiation process. Meanwhile, the AP43771V monitors the voltage and current conditions to avoid abnormal conditions from happening. Once any unacceptable condition happens, the AP43771V will go into the protection procedure according to the types of abnormal conditions.

CC Logic and V_{CONN} Switch

For the USB Type-C solution, two pins on the connector, CC1 and CC2, are used to establish and manage the Source-to-Sink connection, as shown in Figure 3. The CC1/CC2 voltage will be changed due to the resistor loading effect of source Rp / current source and sink Rd during the cable insertion. The AP43771V can then detect the voltage range and decide if the cable is attached, detached, or e-Marker embedded.

Once the cable is connected, both parties will negotiate which side will act as a Source or Sink by periodically changing the impedance on CC pin. The Source side will assign a pullup resistor / current source on its CC pin, and the Sink side will connect a pulldown resistor on CC pin. The AP43771V in this application will play as a Source to offer power to the Sink device, so a pullup resistor / current source is assigned on the CC pin. After the Source to Sink connection is built up, and the V_{CONN} switch is turned on by Source to feed power to the cable through unconnected CC pin as well. At the same time, the Type-C plug orientation can be detected by monitoring the voltage on CC pins (CC1 or CC2), and then the data path from Source to Sink is accomplished.

After the attachment, the VBUS can be supplied 5V power from Source by turning on the VBUS switch, and its current capability is assigned by the pullup resistor / current source on its CC pin.

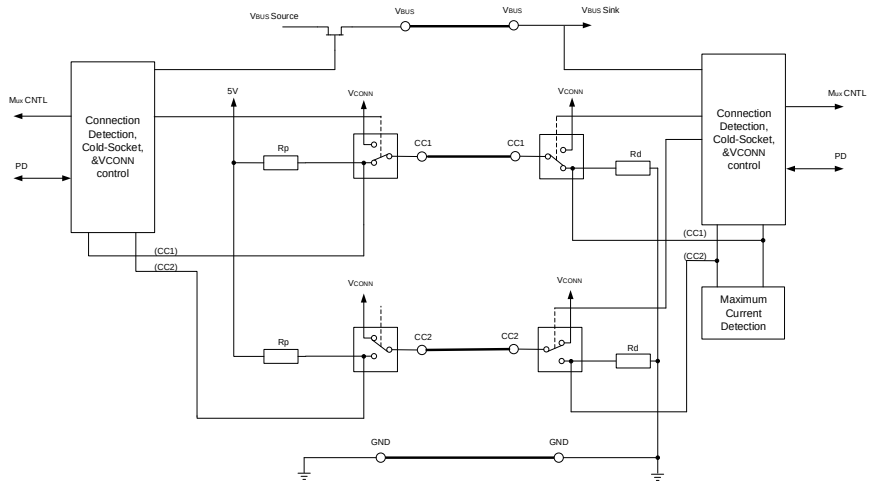


Figure 3. The USB Type-C CC Logic and V_{CONN} Switch

USB Power Delivery (PD) and Phy

The AP43771V supports PD communication over USB Type-C CC channel for advanced power delivery negotiation. A USB PD physical layer that consists of pair of transmitter and receiver for Biphase Marked Coding (BMC) packet communication are embedded.

The transmitter functions include receiving packet data from the protocol layer, calculating a CRC and appending, BMC encoding, packetizing and transmitting on the CC channel. The receiver functions perform clock recovering from pre-amble, packet start detecting, BMC decoding, packet data recovering, CRC validating, packet delivering to the protocol layer or dropping.

The AP43771V is compliant with the USB Power Delivery (PD) specification Rev3.1 supporting full range of Programmable Power Supply (PPS) up to 21V. It has been certified with USB IF TID: 4305.

Performance Characteristics (continued)

USB BC1.2 and HVDCP Protocols

The AP43771V supports USB Battery Charging Rev. 1.2 (BC1.2) and can cover High Voltage Dedicated Charging Port (HVDCP) Qualcomm QC2.0/3.0/4/4+/5 protocols to improve the charging speed between a mobile device and an adapter. The HVDCP leverages BC1.2 compliant signaling and can negotiate voltage and current request through DN/DP pin of USB connector. Meanwhile, some other popular protocols which use the same HVDCP mechanism like AFC, FCP and SCP are also available.

The AP43771V embeds the dedicated hardware to support HVDCP and can perform a better characteristic during the protocol handshaking for quick charging.

Voltage Transition

According to USB PD's protocol, the PD device requests different power profiles, and the AP43771V's power control blocks will change voltage and current values. The AP43771V provides corresponding Overvoltage Protection (OVP), Overcurrent Protection (OCP) scheme, and feedback system stability to guarantee monotonic voltage transition and avoid violating USB PD electrical specification.

The AP43771V provides zero-mismatch voltage methodology that is more flexible for customer system-design requirements. When UFP/DFP makes an acceptable power request deal, the AP43771V will change the VFB pin voltage according to the USB PD command. The voltage regulator control loop regulates the required V_{BUS} voltage according to V_{FB}. In addition, the shunt regulator is built-in to minimize the total external components and cost.

CV/CC Control Loop

The AP43771V uses Constant Voltage (CV) and Constant Current (CC) functions to control the output voltage and current as shown in Figure 4, where both loops are connected at OCDRV pin, and the feedback signal is photo-coupled from the PD controller to the primary power stage.

The CV loop regulates the output to be the expected voltage by sensing VCC through resistor divider to VFB and comparing it with a predetermined voltage set by a DAC converter. The signal difference drives OCDRV to control a photo coupler to the power stage, and then a negative feedback loop is accomplished to regulate VCC to the expected voltage. Here the DAC is used to set the expected VCC output voltage.

The CC loop controls the output to be the expected constant current by sensing the I*Rsense drop on voltage output and comparing IFB with a predetermined voltage set by a DAC converter. The signal difference drives OCDRV to control a photo coupler to the power stage, and then a negative feedback loop is completed to adjust the I*Rsense drop to be equal to the DAC setting. Thereby the corresponding constant current is obtained.

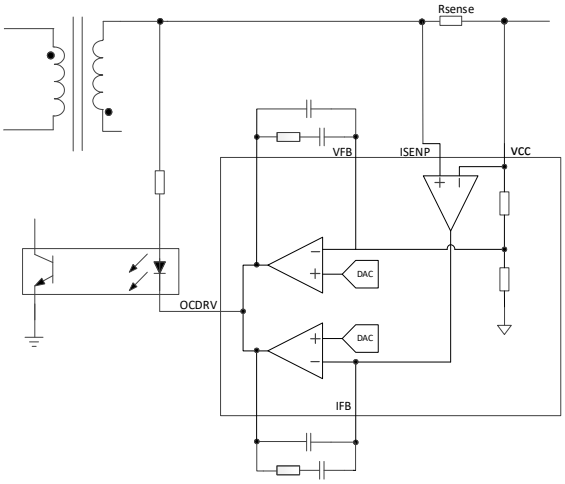


Figure 4. The CC/CV Control Loop in AP43771V

Performance Characteristics (continued)

VBUS nMOS Switch Control

The built-in charge-pump circuit generates a high-voltage gate driver (PWR_EN) to drive an external low cost high-side nMOS switch. A small resistance (10Ω) is suggested to connect the PWR_EN to the nMOS gate. Once the PDO (Power Data Object) negotiations have matched each other between source side and sink side, PWR_EN enables the nMOS switch and VBUS output is enabled. Otherwise, the nMOS switch will remain off. Meanwhile, during the normal operation of AP43771V, the nMOS switch is also used for power protection. Once power protection happens, the nMOS switch is turned off to protect the electrical appliances from possible damage. Meanwhile, it provides internal discharge path at VBUS pin to reduce the abnormal duration.

Discharge Path

To meet the timing requirements of the USB PD specification and field experience, the AP43771V supports the discharge paths (around 200mA sink) for VBUS pin and VCC pin to speed up the voltage drop time during PDO voltage transition, cable detaching, and power protection.

ADC Converter

The AP43771V supports an 8-bit successive approximation ADC. The input to the ADC is an analog input mux that supports multiple inputs from various voltage and current sources in the device. The output from the ADC is available to be read and used by the embedded MCU firmware. Through the data processing and appropriate algorithm, the smart controls and power protections for the AP43771V-embedded system come out.

Overall Features of Dedicated Part Number AP43771VFBZ-13-FR01

The AP43771VFBZ-13-FR01 is designed with standard firmware, preloaded 8 power profiles, where system manufacturers could field select a desired one through a corresponding resistor attached to the OTP pin to meet output profile requirements of a PD3.1 charger. Not only does this approach save OTP (One-Time-Programmable) programming cost, but it also greatly simplifies inventory management of PD decoder chips for various output power chargers. Meanwhile, it supports comprehensive safety protection schemes with standard receptacle output or captive cable. AP43771VFBZ-13-FR01 is available in W-DFN3030-14 (Type A1) package.

PDO Profile Selection and Protocol Supported (For AP43771VFBZ-13-FR01 Only)

There are a total of 8 preloaded Power profiles in the OTP memory of the AP43771VFBZ-13-FR01, illustrated in Table 1. By attaching a proper resistor with corresponding value and 1% accuracy for a desired power profile, system designers could field customize the AP43771VFBZ-13-FR01 to fit 20W to 96W different PD output power applications. Both the fixed PDO up to 20V and full range PPS with power limited mode are supported. In addition, the non-PD protocols like BC1.2, QC2.0, and other popular High Voltage Dedicated Charging Port (HVDCP), like AFC, FCP and SCP are available.

Table 1. Power Profile Selection Table

Power Profiles	USB PD PDO & APDO Configuration						Non-PD Protocols Configuration		Selection Resistance (Ω, 1%)
1	20W	5V/3A	9V/2.22A	12V/1.67A	—	—	QC 18W	FCP 20W	100k
		3.3V~5.9V/3A	3.3V~11V/2.2A	—	—	—	AFC 18W	SCP 20W	
2	25W	5V/3A	9V/2.77A	12V/2.08A	—	—	QC 18W	FCP 25W	82k
		3.3V~5.9V/3A	3.3V~11V/2.75A	—	—	—	AFC 18W	SCP 25W	
3	30W	5V/3A	9V/3A	—	15V/2A	20V/1.5A	QC 27W	FCP 30W	66k
		—	3.3V~11V/3A	—	3.3V~16V/2A	—	AFC 27W	SCP 30W	
4	30W	5V/3A	9V/3A	12V/2.5A	—	—	QC 27W	FCP 30W	52k
		3.3V~5.9V/3A	3.3V~11V/3A	—	—	—	AFC 27W	SCP 30W	
5	35W	5V/3A	9V/3A	—	15V/2.33A	20V/1.75A	QC 27W	FCP 35W	39k
		—	3.3V~11V/3A	—	3.3V~16V/2.3A	—	AFC 27W	SCP 35W	
6	45W	5V/3A	9V/3A	—	15V/3A	20V/2.25A	QC 27W	FCP 45W	26k
		—	3.3V~11V/4.05A	—	3.3V~16V/3A	—	AFC 27W	SCP 45W	
7	65W	5V/3A	9V/3A	—	15V/3A	20V/3.25A	QC 27W	FCP 60W	15k
		—	—	—	3.3V~16V/4.05A	3.3V~21V/3.25A	AFC 27W	SCP 60W	
8	96W	5V/5A	9V/5A	—	15V/5A	20V/4.8A	QC 27W	FCP 60W	5.1k
		—	—	—	3.3V~16V/5A	3.3V~21V/5A	AFC 27W	SCP 60W	

Notes:
11. All profiles support cable 90mΩ resistance compensation, DCP mode in 5V/3A, and Apple mode in 5V/3A.
12. All PPS profiles are set at power limited mode.
13. AFC mode is supported and is the same with QC mode.
14. FCP mode and SCP mode are supported up to 60W.
15. Overvoltage protection (OVP) is set at 120% of PDO output.
16. Undervoltage protection (UVP) is set at 75% of PDO output.
17. Short-circuit protection (SCP) is set at 0Ω load.
18. Overcurrent protection (OCP) is set at 110% of maximum load for fixed PDO, DCP and Apple modes, while constant-current protection is used in PPS, QC, AFC, FCP and SCP modes.
19. Vendor ID (VID) = 10817 is assigned in VDM command.
20. It is suggested to use 1% accuracy of selection resistance. If the resistor is left open or short, the power profile is set to 20W or 96W respectively.

Performance Characteristics (continued)

Power Protection Configuration (For AP43771VFBZ-13-FR01 Only)

The AP43771VFBZ-13-FR01 provides OVP/UVP/OCP/SCP power protection functions and also supports Constant Current (CC) function in PPS operation and other constant current modes. All of the protection thresholds are related to the requested power profile.

The OVP threshold is set at 120% of PDO output. Once the VBUS output voltage is higher than OVP threshold, the VBUS MOS is turned off and an internal discharge path from VBUS pin to ground to reduce the overvoltage duration.

The UVP threshold is set at 75% of PDO output. Once the VBUS output voltage drops to UVP threshold, the VBUS MOS is turned off to avoid the abnormal operation of the electrical appliances.

The OCP threshold is set at 110% of PDO maximum load for fixed PDO, DCP, and Apple modes. Once the VBUS output current is higher than OCP threshold, the AP43771VFBZ-13-FR01 will shut down VBUS output and send out “Hard Reset” command to the Sink device. For the PPS, QC, AFC, FCP, and SCP, the constant-current (CC) protection is used. Once the output current exceeds the allowed maximum current, the output voltage will drop sharply and trigger the UVP to turn off the VBUS output. When the output voltage drops below UVLO threshold, the AP43771VFBZ-13-FR01 will reset.

For the SCP power protection, it is triggered as soon as both the OCP and UVP happen. It is set with 0Ω load used.

Captive Cable Support Configuration (For AP43771VFBZ-13-FR01 Only)

The AP43771VFBZ-13-FR01 supports adapter with receptacle or captive cable. If captive cable is selected, the 8.5kΩ resistor should be connected from CC2 pin to ground, as shown in Figure 5 below.

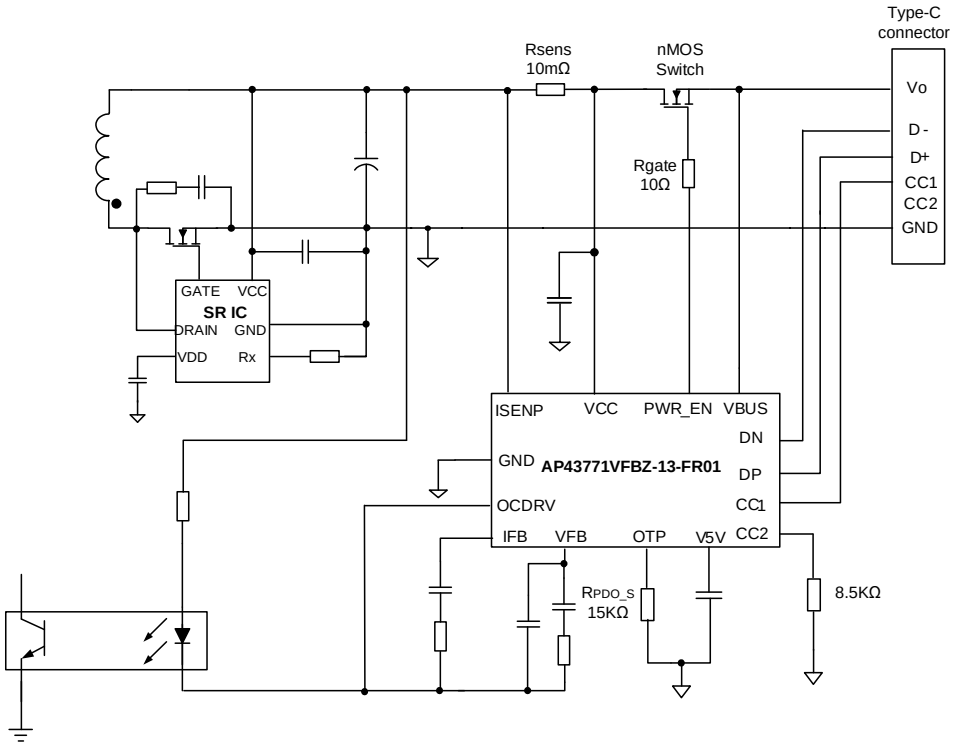


Figure 5. Captive Cable Is Supported Through a Resistor Connection from CC2 Pin to Ground

Performance Characteristics (continued)

I2C Interface (W-QFN4040-24 (Type A1) Only, for Customized Firmware Only)

To support multiple Type-C ports PD applications, the AP43771V (W-QFN4040-24 (Type A1)) can be used for implementing smart power sharing scheme. One AP43771V works as a Master to monitor status of other Slave AP43771V through I2C interface. The Master AP43771V can deliver I2C commands to the Slave AP43771V for re-allocating desired power profile for each Type-C port.

Due to the complicated conditions and diversified requirements in Multiple ports application, the power sharing function needs to be implemented with customized firmware.

AP43771V includes I2C Interface pins (SCL, SDA,) as below table shows, and I2C commands are supported by firmware so that It can monitor and change status of other I2C devices.

I2C Interface Pin List

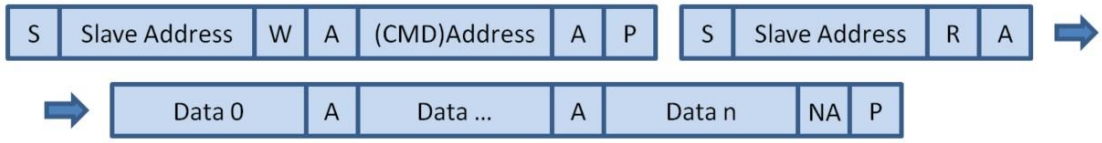
Pin No	Pin Name	Pin Function
4	SDA	I2C Data
5	SCL	I2C Clock

One AP43771V plays as an I2C either master or slave device. The I2C read and write operations are supported as below.

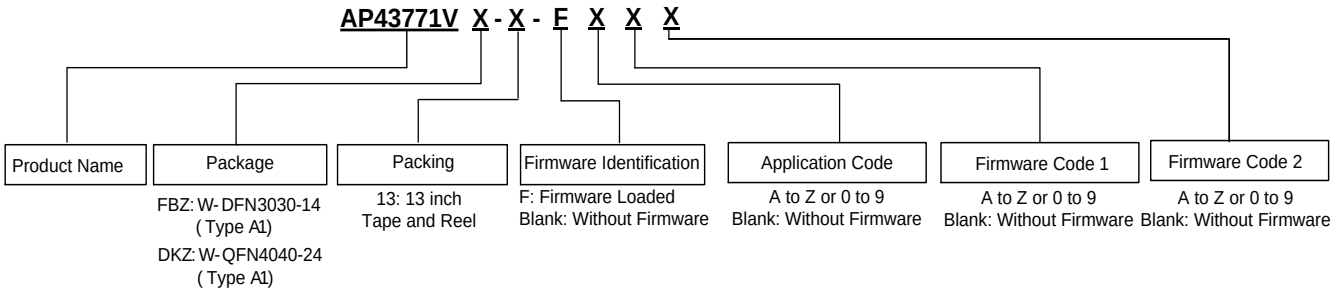
All transactions begin with a START (S) and be terminated by a STOP (P). A START condition is defined whenever a HIGH to LOW transition on the SDA while SCL is HIGH. A STOP condition is defined whenever a LOW to HIGH transition on the SDA while SCL is HIGH. START and STOP conditions are always generated by the master.

I2C Format for Write Data

I2C Format for Read Data



Ordering Information



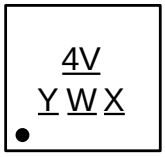
Orderable Part Number (Note 21)	Package	Identification Code	Firmware Inside	Packing	
				Qty.	Carrier
AP43771VFBZ-13-FR01	W-DFN3030-14 (Type A1)	4V	Standard Firmware (Function as described in Datasheet)	3000	13” Tape & Reel
AP43771VFBZ-13-FXXX			Customized Firmware		
AP43771VDKZ-13-FXXX	W-QFN4040-24 (Type A1)	6B	Customized Firmware		

Note: 21. It is recommended to order Standard Firmware device based on functions described in datasheet. For without firmware and customized options, please contact us or your local Diodes representative.

Marking Information

W-DFN3030-14 (Type A1)

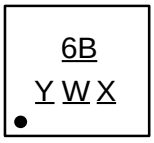
(Top View)



4V : Identification Code
Y : Year : 0 to 9 (ex: 4 = 2024)
W : Week : A to Z : week 1 to 26;
a to z : week 27 to 52; z represents week 52 and 53
X : Internal Code

W-QFN4040-24 (Type A1)

(Top View)

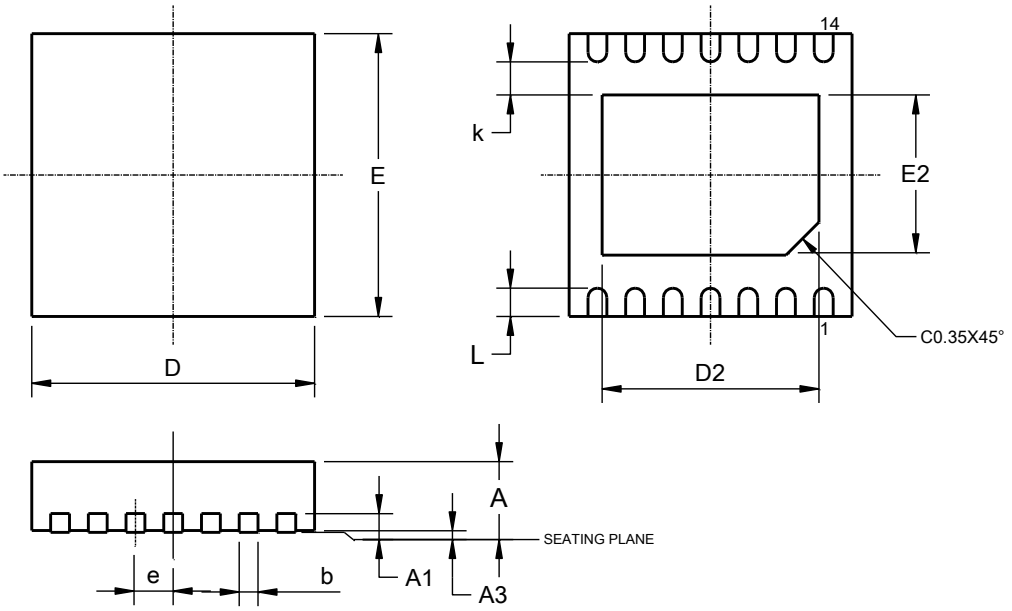


6B : Identification Code
Y : Year : 0 to 9 (ex: 4 = 2024)
W : Week : A to Z : week 1 to 26;
a to z : week 27 to 52; z Represents week 52 and 53
X : Internal Code

Package Outline Dimensions

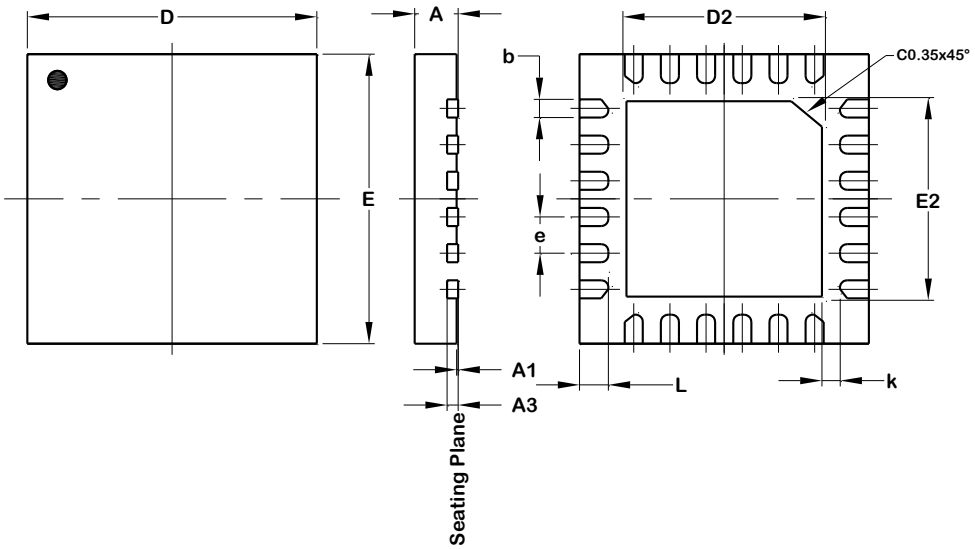
Please see http://www.diodes.com/package-outlines.html for the latest version.

W-DFN3030-14 (Type A1)



W-DFN3030-14 (Type A1)			
Dim	**Min**	**Max**	**Typ**
A	0.70	0.80	0.75
A1	0	0.05	0.02
A3	0.203REF		
b	0.15	0.25	0.20
D	3.00BSC		
D2	2.55	2.65	2.60
e	0.40BSC		
E	3.00BSC		
E2	1.65	1.75	1.70
k	0.20	--	--
L	0.35	0.45	0.40
All Dimensions in mm			

W-QFN4040-24 (Type A1)

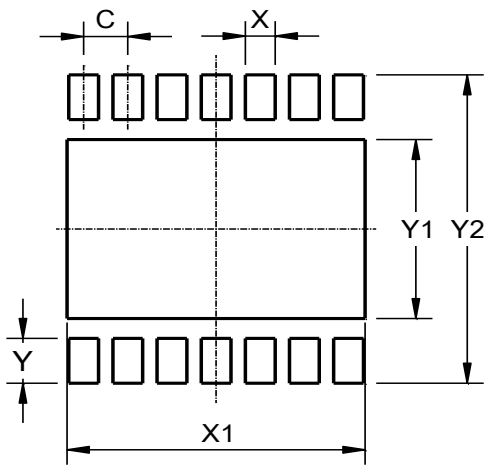


W-QFN4040-24 (Type A1)			
Dim	**Min**	**Max**	**Typ**
A	0.70	0.80	0.75
A1	0.00	0.05	0.02
A3	0.203 REF		
b	0.18	0.30	0.25
D	4.00 BSC		
D2	2.65	2.75	2.70
E	4.00 BSC		
E2	2.65	2.75	2.70
e	0.50 BSC		
k	0.20	--	--
L	0.35	0.45	0.40
All Dimensions in mm			

Suggested Pad Layout

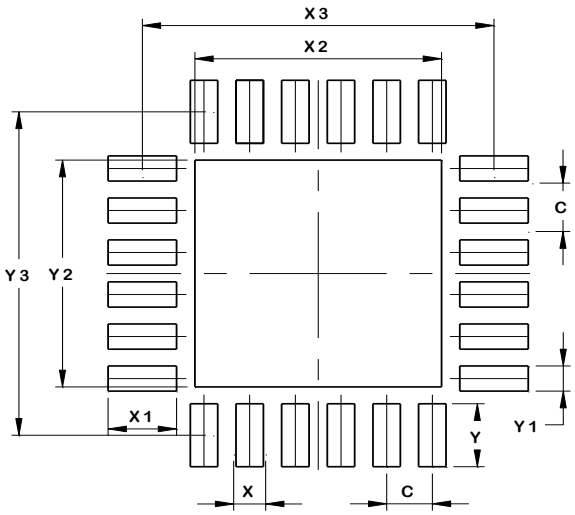
Please see http://www.diodes.com/package-outlines.html for the latest version.

W-DFN3030-14 (Type A1)



Dimensions	Value (in mm)
C	0.40
X	0.27
X1	2.70
Y	0.45
Y1	1.80
Y2	3.10

W-QFN4040-24 (Type A1)



Dimensions	Value (in mm)
C	0.500
X	0.300
X1	0.750
X2	2.700
X3	3.850
Y	0.750
Y1	0.300
Y2	2.700
Y3	3.850

Mechanical Data

- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals: Finish – Matte Tin Plated Leads, Solderable per J-STD-202 e3
- Weight:
  - W-DFN3030-14 (Type A1): 0.017 grams (Approximate)
  - W-QFN4040-24 (Type A1): 0.041 grams (Approximate)

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