AUTOMOTIVE-GRADE DUAL-CHANNEL USB TYPE-C PROTOCOL DECODER

Description

The AP43776Q is a highly integrated, dual-channel, USB Type-C®, PD3.1 / PPS, BC 1.2 and QC protocol decoder. It is certified to USB Type-C power delivery specification Rev 3.1 with PPS and Quick Charge™ QC5 protocol.

The device supports the full range of PPS APDO (augmented power data object) from 3.3V to 21V with 20mV/step voltage resolution and up to 6A current with 50mA/step resolution for power management. To enable an output current beyond 3A, the AP43776Q supports e-Marker cable detection with built-in VCONN switch, and with 30mA driving capability and overcurrent protection (OCP). Cable-loss compensations are also embedded.

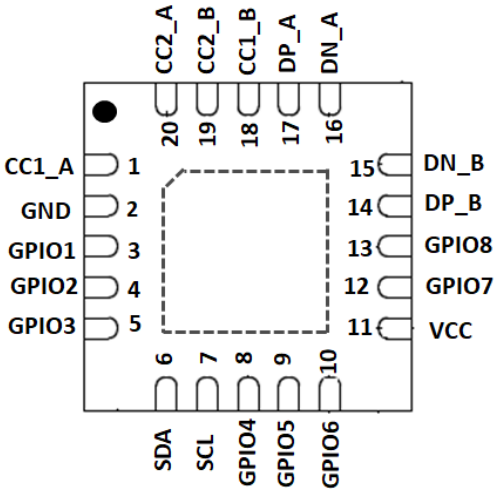
During power charging, the AP43776Q can support DisplayPort Alternate Mode by decoding out the CC signal and deliver the routing signal to the mux switch through the I2C interface, Meanwhile, the AP43776Q also supports BC1.2 CDP handshaking.

The AP43776Q provides an embedded MCU and built-in ADC converters for voltage and temperature measurement, where overtemperature protection (OTP) and other specific functions can be implemented through I2C pins and rich GPIO pins. Working in conjunction with two I2C-equipped Buck-Boost controllers, or converters which have PD3.1 PPS output circuitry, the AP43776Q serves as the I2C master and supports two independent PD3.1 PPS charging applications without using additional output enable MOS chips for each PD3.1 output port.

With built-in firmware, the AP43776Q supports various smart power-management functions such as a power-sharing scheme between two attached USB Type-C PD devices, low-battery power de-rating, thermal power de-rating, LED light indication, etc. Two AP43776Q devices can also be interconnected through a UART (GPIO) pin to implement a smart power-sharing scheme for all four connected USB Type-C ports attached to a fixed power source.

Pin Assignments

(Top View)



W-QFN4040-20

Features

- AEC-Q100 Qualified with the Following Results:
  - Device Temperature Grade 1: -40°C to +125°C TA Range
  - Device HBM ESD Classification Level H3A
  - Device CDM ESD Classification Level C5
- Dual-channel independent USB Type-C PD3.1/PPS decoder
- USB-IF PD3.1/PPS certificated TID: 9440
- Quick Charge™ QC5 certificated No.: QC20211008263
- PD3.1/ full range of PPS VOUT (3.3V to 21V)
- Compliant with BC1.2 DCP mode for QC2.0/3.0/4/4+/5
- USB Type-C PD DisplayPort Alternative mode
- BC 1.2 CDP (Charging Downstream Port) mode for Charging Downstream device and allow data transfer
- Built-in ADC and multi-channel multiplexer for voltage and temperature measurement
- e-Marker detection and VCONN 30mA capability
- Cable-loss compensations
- I2C Interface and Interrupt
- Multi-purpose I/Os to support different applications
- CC1/CC2 to VBUS short protection up to 24V
- Moisture detection between DP and DN
- Thermal protection through external NTC
- Output power de-rating for low battery
- Built-in MCU with 12KB OTP ROM for main application program with multi-time-programmable ROM (MTP ROM) blocks for customization
- W-QFN4040-20 (SWP) (4x4, 0.5mm pitch) package

Features (continued)

- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**
- **The AP43776Q is suitable for automotive applications requiring specific change control; this part is AEC-Q100 qualified, PPAP capable, and manufactured in IATF 16949 certified facilities.**
  https://www.diodes.com/quality/product-definitions/

Applications

- In-vehicle multi-port USB PD3.1 charging systems

Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

Typical Applications Circuit

Application 1:

Two USB Type-C-port car charger based on one AP43776Q + two DC/DC, where I2C bus is used for communication between the AP43776Q and two DC/DC controllers. It is shown that the USB Type-C output MOS switch is not needed.

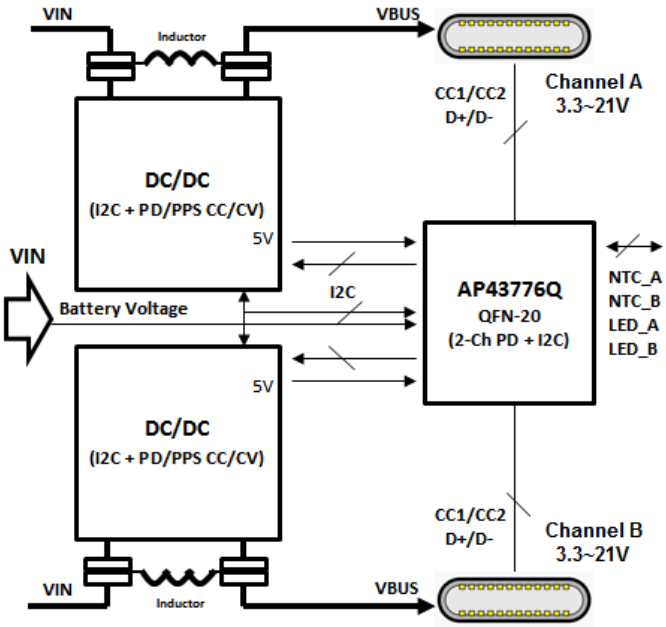


Figure 1. A two-channel car charger

Application 2:

Four USB Type-C-port car charger based on two AP43776Q + four DC/DC controllers, where smart power sharing is performed through the I2C and UART buses.

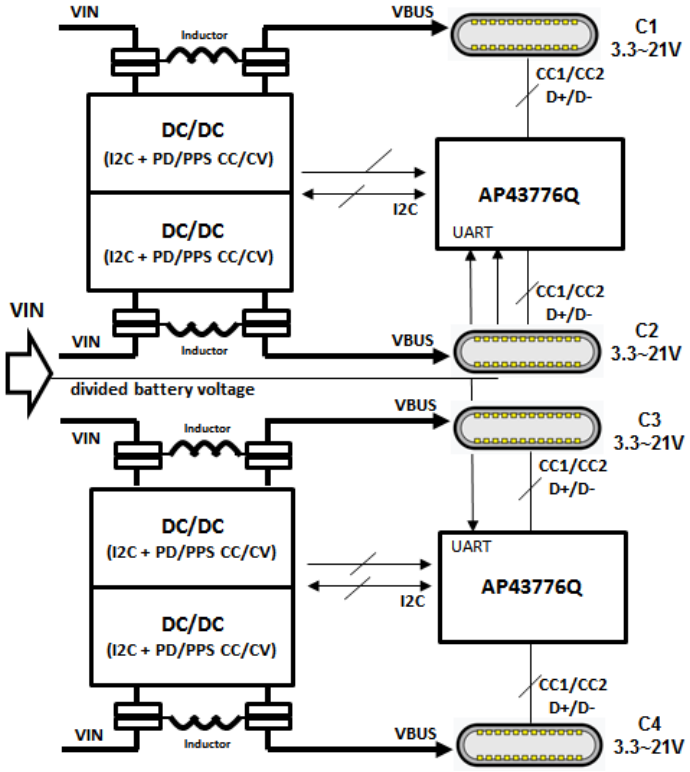


Figure 2. A four-channel car charger

Typical Applications Circuit (continued)

An example of the 120W dual-port Type-C PD3.1 PPS car charger is shown in Figure 3. Powered by the VREG pin (internal 5V regulator output) for the attached DC-DC controller and detecting the Vin through GPIO1, the AP43776Q may enter standby mode to disable DC/DC stage by controlling the GPIO2 pin. All PD decoded information and measured parameters of the operating conditions are processed through the CC1 and CC2 pins. The AP43776Q conveys necessary actions, such as constant voltage output, constant current output, and protection functions through the I2C interface. With built-in application firmware, VBUS MOS switches are not needed, and GPIO pins are used for battery detection, power sharing, temperature detection, LED indicators, and so on.

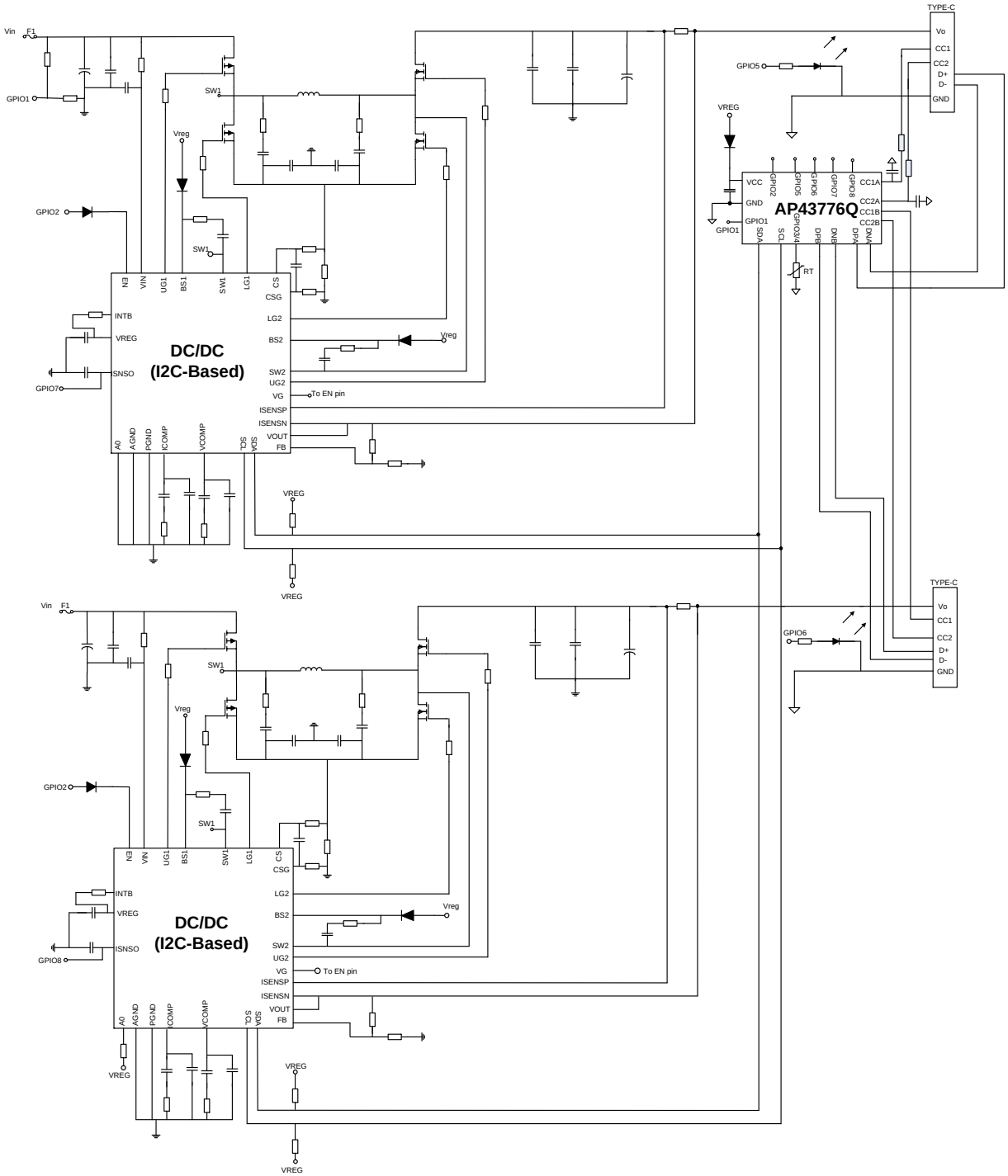


Figure 3. A 120W 2C PD3.1 PPS car charger design based on 2*DC/DC+1*AP43776Q

Typical Applications Circuit (continued)

Application 3: Alternate Mode and BC 1.2 CDP Mode Support

The AP43776Q not only supports power protocol decoding, but also provides data link capability. Figure 4 illustrates an AP43776Q application scenario of power source and data link.

One of the ports is used as a USB Type-C connector, which is connected to the Notebook host or smart phone device. The power from Down Facing Port (DFP) is sourced out to the Notebook/device, and the video data from Up Facing Port (UFP) is linked to the car navigation system through the AP43776Q supporting alternative mode. During the handshake, the AP43776Q decodes the alternative mode information of the Notebook host's or device's CC commands, and then the information is sent to the high-speed mux to switch the data path accordingly.

The other ports may be used as a Type-A connector supporting BC 1.2 CDP mode, where not only power is sourced out for the device, but also data may be linked to the car navigator at the same time.

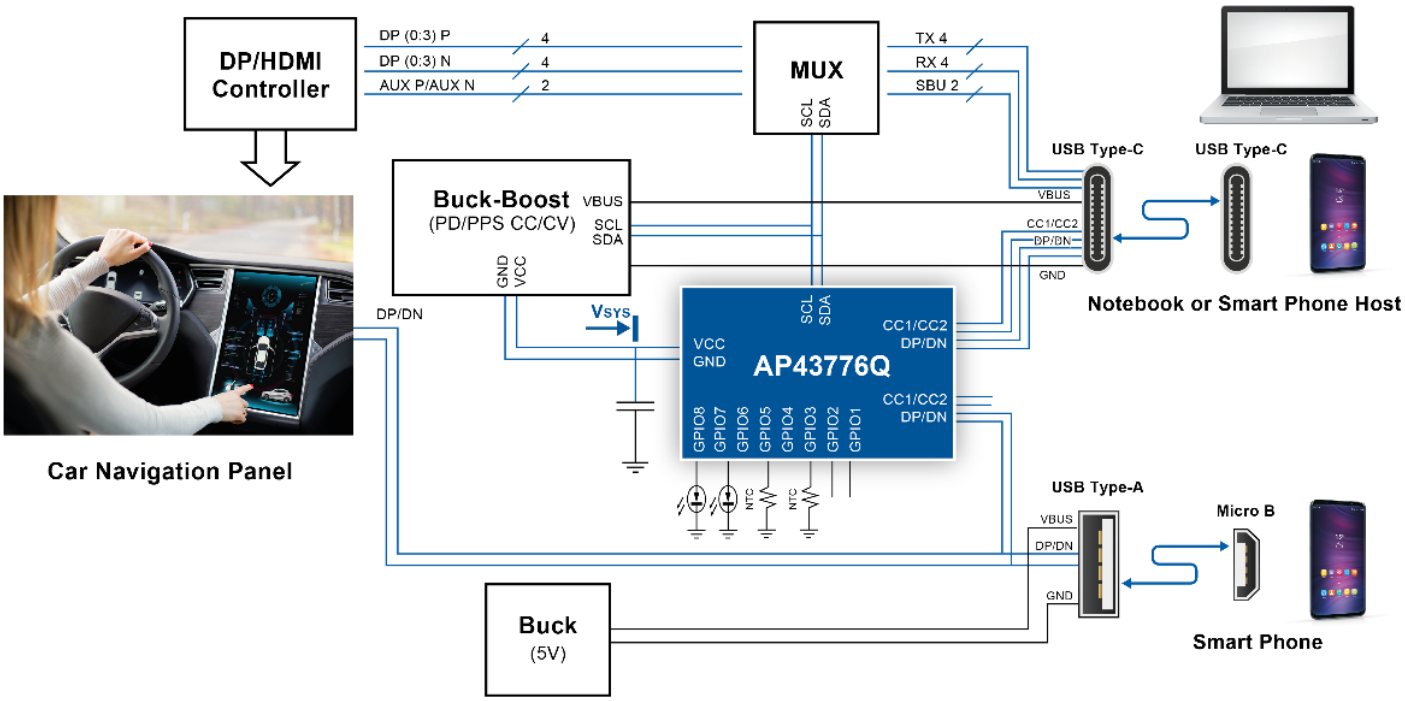


Figure 4. The AP43776Q supports DP alternative mode and BC 1.2 CDP mode for data link during power sourcing

Pin Descriptions

Pin Number	Pin Name	Function
1	CC1_A	Output to channel-A Type-C CC or VCONN pin.
2	GND	Ground pin.
3	GPIO1	Multipurpose I/O pin (defined for UART application).
4	GPIO2	Multipurpose I/O pin (defined for UART application).
5	GPIO3	Multipurpose I/O pin (defined for NTC application).
6	SDA	Data pin of I2C (defined for communication with I2C-based Buck-Boost or Buck IC).
7	SCL	Clock pin of I2C (defined for communication with I2C-based Buck-Boost or Buck IC).
8	GPIO4	Multi-purpose I/O pin with current source (defined for NTC application).
9	GPIO5	Multipurpose I/O pin (defined for LED indicator light).
10	GPIO6	Multipurpose I/O pin (defined for LED indicator light).
11	VCC	Power supply pin.
12	GPIO7	General-purpose I/O pin (defined for V/I report of Buck-Boost or Buck IC).
13	GPIO8	General-purpose I/O pin (defined for V/I report of Buck-Boost or Buck IC).
14	DP_B	Connected to channel-B Type-C DP pin.
15	DN_B	Connected to channel-B Type-C DN pin.
16	DN_A	Connected to channel-A Type-C DN pin.
17	DP_A	Connected to channel-A Type-C DP pin.
18	CC1_B	Output to channel-B Type-C CC or VCONN pin.
19	CC2_B	Output to channel-B Type-C CC or VCONN pin.
20	CC2_A	Output to channel-A Type-C CC or VCONN pin.
—	Exposed Pad	Connected to PCB Ground.

Functional Block Diagram

The AP43776Q is an MCU-based, dual-channel, USB Type-C, PD3.1/PPS and QC5 protocol decoder. The device's functional block diagram is shown below. With its hardware transceivers and multiplexed ADC, the rich multipurpose GPIOs can support many different kinds of applications.

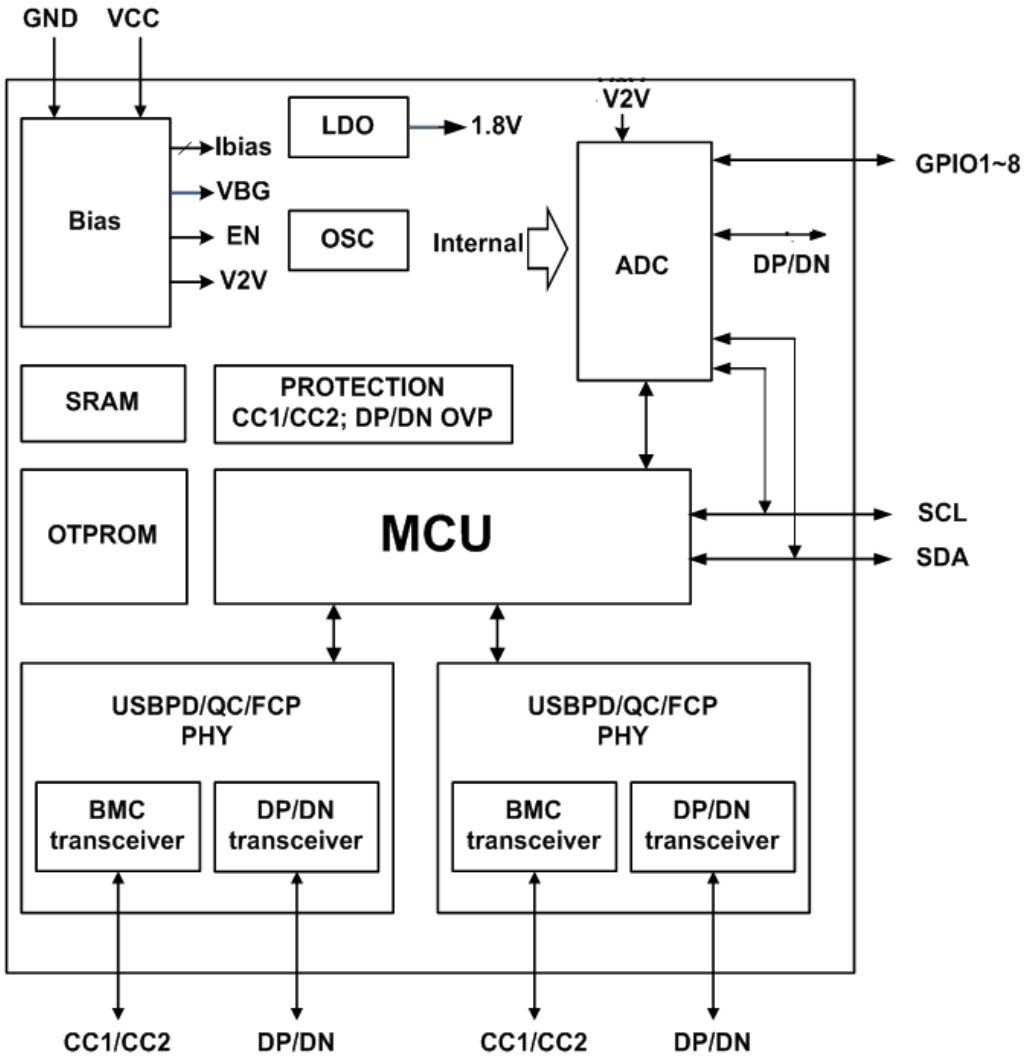


Figure 5. The functional block diagram of the AP43776Q

Functional Overview

Function Description

The AP43776Q is a highly integrated, dual-channel, USB Type-C PD3.1/ PPS/ QC5 protocol decoder, and has passed the certification of USB-IF PD3.1/PPS and Qualcomm™ QC5.0. To ensure two independent PD3.1 PPS protocol decoding operations are in full compliance with critical USB Power Delivery specification rev 3.1, the AP43776Q implements a combination of hardware and MCU firmware to leverage quick response times from the hardware and maintain software flexibility. To reduce noise interference during chip application, I2C communication is used between the PD controller and DC/DC converter.

USB Type-C CC Logic & PD 3.1 Engine

The AP43776Q supports the latest USB Power Delivery Specification Revision 3.1, and is compliant to USB Type-C Cable and Connector Specification Revision 2.1. The device can support the full range of PPS APDO (augmented power data object) from 3.3V to 21V with 20mV/step voltage resolution and up to 6A current with 50mA/step resolution for power management.

The device has two independent protocol decoders and plays as two DFPs (providers only). To leverage quick response times from the hardware circuitry, it consists of USB Type-C baseband transceivers, physical-layer logic, and DP/DM transceivers for supporting QC and FCP protocols. All communications are half-duplex, and the Physical Layer provides collision avoidance to minimize communication errors during handshake. These transceivers perform the BMC and the 4b/5b encoding and decoding functions as well as the analog front end.

To perform the CC detection logic, the current sources and switches are integrated to perform the R_P resistors, as required by USB Type-C specifications to implement connection detection, plug orientation detection, and to establish USB DFP role. Also, it can be programmed to indicate the complete range of current capacity on VBUS.

The built-in VCONN power switch is provided to the cable e-Marker over the CC pin that is determined not to be connected to the CC wire as soon as a cable is plugged in. The maximum output power of VCONN is 150mW.

CC Pin and V_{CONN} Switch Operating Mechanism

For the USB Type-C solution, two pins on the connector (CC1 and CC2) are used to establish and manage the Source-to-Sink connection, as shown in Figure 6. The CC1/CC2 voltage will change due to the resistor loading effect of the source Rp/current source and sink Rd during cable insertion. The AP43776Q then detects the voltage range and decides if the cable is attached, detached, or if an e-Marker is embedded.

Once the cable is connected, both parties will negotiate which side will act as a Source or Sink by periodically changing the impedance on the CC pin. The Source side will assign a pullup resistor/current source on its CC pin, and the Sink side will connect a pulldown resistor on the CC pin. The AP43776Q in this application will play as a Source to offer power to the Sink device, so a pullup resistor/current source is assigned on the CC pin. After the Source-to-Sink connection is built up, the V_{CONN} switch is also turned on by the Source to feed power to the cable through unconnected CC pin. At the same time, the USB Type-C plug orientation can be detected by monitoring the voltage on the CC pins (CC1 or CC2), and then the data path from Source to Sink is accomplished.

After the attachment, the Source can supply 5V of power to the VBUS by turning on the VBUS switch. Its current capability is assigned by the pullup resistor/current source on its CC pin.

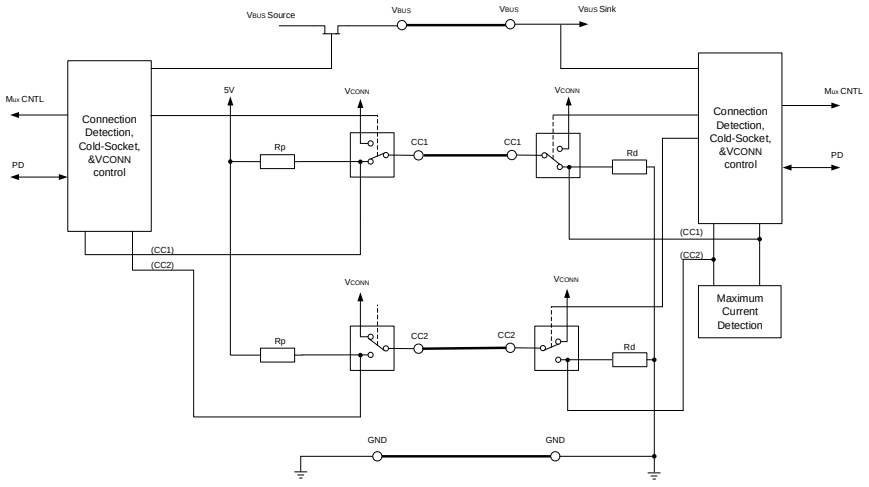


Figure 6. The USB Type-C CC Logic and V_{CONN} Switch

Functional Overview (continued)

USB Power Delivery (PD) and Physical layer

The AP43776Q supports PD communication over USB Type-C CC channel for advanced power delivery negotiation. Embedded are a USB PD physical layer that consists of a transmitter and receiver pair for Biphase Marked Coding (BMC) packet communication.

The transmitter functions include receiving packet data from the protocol layer, calculating a CRC and appending, BMC encoding, packetizing, and transmitting on the CC channel. The receiver functions perform clock recovering from pre-amble, packet start detecting, BMC decoding, packet data recovering, CRC validating, packet delivering to the protocol layer, or dropping.

The AP437776Q is compliant with USB Power Delivery (PD) specification Rev3.1, supporting the full range of Programmable Power Supply (PPS) up to 21V.

USB BC 1.2 DCP (Dedicated Charging Port) Mode and Quick-Charging Legacy

The AP43776Q integrates the USB dedicated charging port auto-detect function to recognize most mainstream portable devices. It supports charging schemes such as BC1.2 DCP mode, Apple mode, Chinese Telecommunications Industry Standard YD/T 1591-2009, FCP Class A, and Qualcomm Quick Charging HVDCP mode (QC2.0/3.0/4/4+/5).

DisplayPort Alternate Mode Support

The AP43776Q supports DisplayPort Alternate Mode on the USB Type-C standard, with DP mode Discovery, Enter, Exit included. The USB Type-C data stream can be correctly routed to the DP/HDMI receiver by decoding out the control signals from the CC handshaking, then delivering the mux switches through the I2C interface. Also provided are the DP configuration, status update, and source/sink connection detection.

USB BC1.2 CDP Mode

The AP43776Q also supports BC 1.2 CDP (Charging Downstream Port) Mode. It can be enabled by I2C communication. When CDP is enabled, QC/Apple and DCP modes on the DP and DM will be turned off.

Bias and Power

The AP43776Q operates from a single external supply source, VCC. VCC is used for analog circuitry and goes through internal regulators to generate all of the voltage and current references for chip operation, without the need for external capacitor decoupling. The AP43776Q has two different power modes: normal and sleep. During normal operation, the AP43771 consumes less than 3mA. During sleep mode, its current can be reduced to around 0.5mA automatically.

I2C Interface

For USB Type-C PD charging system, the I2C interface pins (SCK, SDA) are used to communicate between the PD decoder and DC/DC controller/converter to replace analog signal feedback with much higher noise immunity. The AP43776Q is in charge of the CC1/CC2 or DP/DN protocol handshake with the attached device, and deliver the voltage and current request to DC/DC controller/converter through I2C bus.

The AP43776Q, working as an I2C master device, keeps track of charging capability of each USB Type-C port through I2C interface pins at the same time. Based on the user-specified and desired smart power-sharing options for the two charging ports, the AP43776Q decides the final charging profiles for each port.

MCU and OTP/MTP ROM

The AP43776Q has an MCU subsystem, which integrates an 8-bit 8051 processor, SRAM, and OTP ROM. The MCU subsystem is optimized for user configurability of different topologies, support of different protocols, and low-power consumption at a low cost. With the embedded hardware PHY transceivers offloading MCU processing, the AP43776Q can handle two channels of PD handshakes efficiently through an MCU simultaneously and be compliant with critical USB Power Delivery specifications.

An OTP ROM is provided to store PD, QC, and FCP protocol firmware, and an MTP ROM is provided for user-configuration table. Either in-system programming or offline socket programming are provided for the OTP ROM and MTP ROM.

Functional Overview (continued)

ADC

The AP43776Q contains a 10-bit SAR (successive approximation register) ADC and multi-channel multiplexer for analog to digital conversions. All GPIO inputs can be connected to the internal analog multiplex buses through a switch. With the ADC voltage reference, VREF (set at 2V), any input voltage (Vin) on the GPIO can be digitized into a 10-bit digital code proportional to Vin/VREF. The sampling rate of ADC is 100KHz, but the firmware re-samples the ADC output by 1ms/time. A period of longer de-glitch time is used to qualify the ADC output code. Meanwhile, ADC is used to detect and monitor analog signals on the non-GPIO pins such as CC1/CC2/VCONN and DP/DN, and then enables the associated OVP protections.

GPIO Support

There are many GPIO pins that can be used to support customization features, such as low-voltage battery, power de-rating, thermal power de-rating, LED light indication, fault status, and so on. The GPIO pin can also be used for UART communication to support four USB Type-C ports, and some GPIOs support current sources for external NTC temperature detection.

Seen below, figure 7 is the equivalent structure of the GPIO pin. Q1~Q4 can be flexibly enabled/disabled by the firmware for input or output application scenarios. GPIO 3/4 have a controlled 100μA current source, which can be connected to the pin output for temperature sensing with an output NTC.

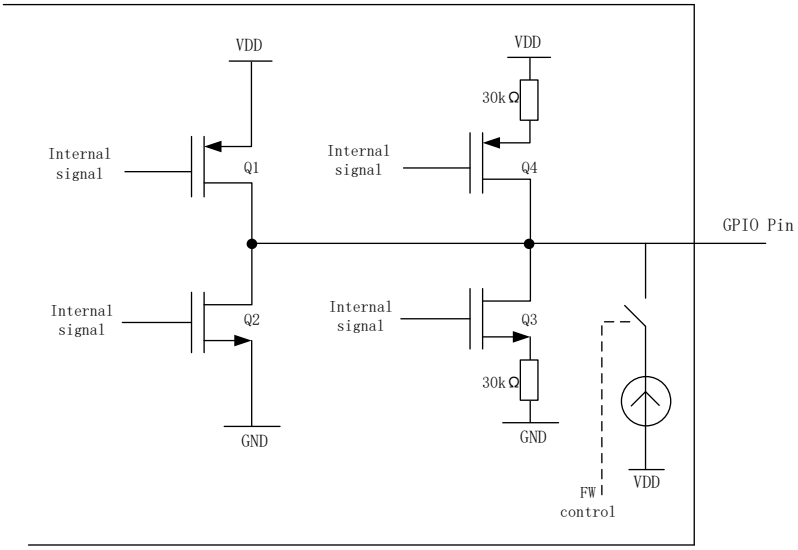


Figure 7. The structure of GPIO pin in AP43776Q

Below, table 1 summarizes the GPIO configuration for different applications. The maximum output voltage of the GPIO pin is 5V; we suggest to pull high to 5V for the voltage source if necessary.

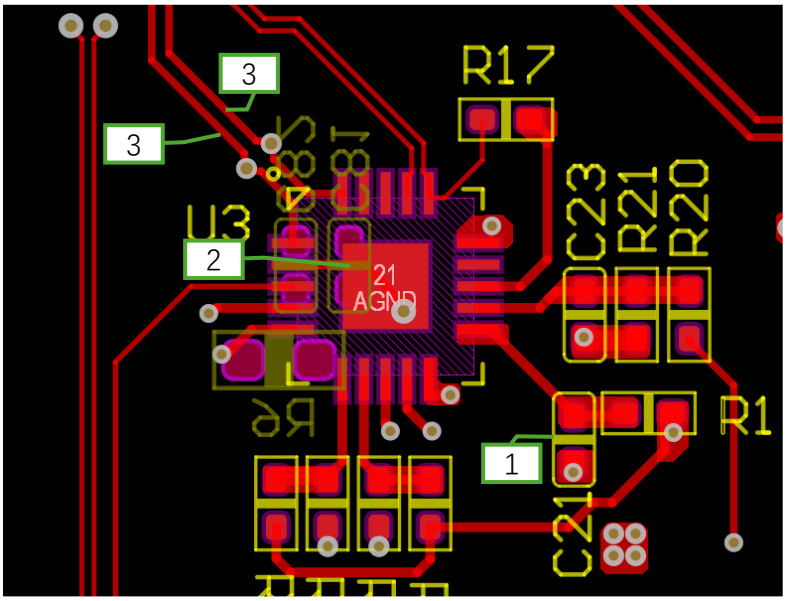
PIN	GPIO configuration for output	GPIO configuration for input	GPIO configuration for temperature sensing	Maximum Output
GPIO1	Q3/Q4 disabled internally, No need pull high and pull low externally	Q1/Q2 disabled , Default 30kΩ pull high internally , suggest 3kΩ pull low externally	-	5V
GPIO2	Q3/Q4 disabled internally, No need pull high and pull low externally	Q1/Q2 disabled , Default 30kΩ pull high internally , suggest 3kΩ pull low externally	-	
GPIO3	Q3/Q4 disabled internally, No need pull high and pull low externally	Q1/Q2 disabled , Default 30kΩ pull low internally , suggest 3kΩ pull high externally	Q1/Q2/Q3/Q4 disabled , internal 100uA current source connected on pinout, suggest 0~20kΩ NTC pull low externally	
GPIO4	Q3/Q4 disabled internally, No need pull high and pull low externally	Q1/Q2 disabled , Default 30kΩ pull low internally , suggest 3kΩ pull high externally	Q1/Q2/Q3/Q4 disabled , internal 100uA current source connected on pinout, suggest 0~20kΩ NTC pull low externally	
GPIO5	Q3/Q4 disabled internally, No need pull high and pull low externally	Q1/Q2 disabled , Default 30kΩ pull low internally , suggest 3kΩ pull high externally	-	
GPIO6	Q3/Q4 disabled internally, No need pull high and pull low externally	Q1/Q2 disabled , Default 30kΩ pull low internally , suggest 3kΩ pull high externally	-	
GPIO7	Q3/Q4 disabled internally, No need pull high and pull low externally	Q1/Q2 disabled , Default 30kΩ pull low internally , suggest 3kΩ pull high externally	-	
GPIO8	Q3/Q4 disabled internally, No need pull high and pull low externally	Q1/Q2 disabled , Default 30kΩ pull low internally , suggest 3kΩ pull high externally	-	

Table 1. GPIO configuration summary

PCB Layout Guideline

A suitable PCB layout is critical for stable operation and improved ESD performance. Please follow the guidelines as seen below:

1. Place the Vcc/V5V decoupling capacitor as close to the pins as possible.
2. The exposed pad of the IC must be connected to GND, which improves noise immunity.
3. Use traces to connect CC1/CC2 pins to the USB Type-C receptacle as short as possible.



Absolute Maximum Ratings (Note 4)

Symbol	Parameter	Rating	Unit
V_{CC}	Input Voltage at V_{CC} Pin	6.0	V
V_{CC1A}, V_{CC2A}, V_{CC1B}, V_{CC2B}	Input Voltage at CC1_A,CC2_A,CC1_B,CC2_B Pins	24	V
V_{DPA}, V_{DNA}, V_{DPB}, V_{DNB}, SDA, SCL and $GPIO_X$	Input Voltage at DPA, DNA, DPB, DNB, SDA, SCL, and GPIOx Pins	6.0	V
T_J	Operating Junction Temperature	-40 to +150	°C
T_{STG}	Storage Temperature	-65 to +150	°C
T_{LEAD}	Lead Temperature (Soldering, 10s)	+300	°C
θ_{JA}	Thermal Resistance (Junction to Ambient) (Note 5)	122	°C/W
θ_{JC}	Thermal Resistance (Junction to Case) (Note 5)	27	°C/W
ESD	ESD (Human Body Model) Voltage on D+, D- Pins	±6	kV
	ESD (Human Body Model) Voltage on other Pins	±4	kV
	ESD (Charged Device Model)	±1000	V

Notes: 4. Stresses greater than those listed under *Absolute Maximum Ratings* can cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to *Absolute Maximum Ratings* for extended periods can affect device reliability.

5. Test condition: Device mounted on FR-4 substrate PC board, 2oz copper, with the minimum footprint.

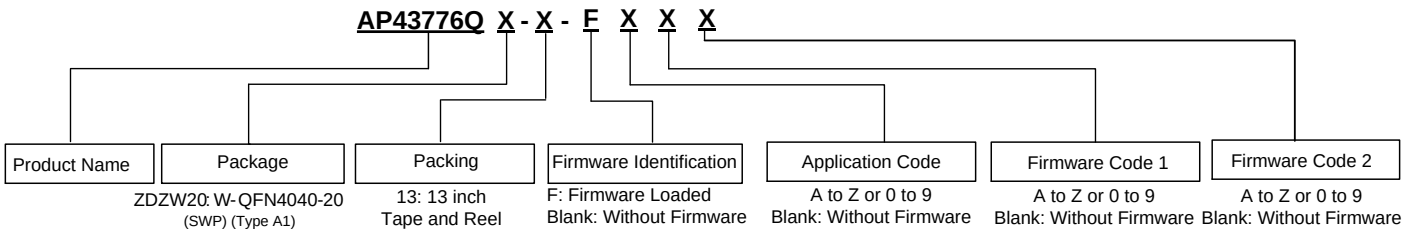
Recommended Operating Conditions

Symbol	Parameter	Min	Max	Unit
V_{CC}	Power Supply Voltage	3	5.5	V
T_{OP}	Operating Temperature Range	-40	+125	°C

Electrical Characteristics (-40°C < T_A< +125°C , V_{CC} = 5V, unless otherwise specified.)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
VCC PIN & INTERNAL BIAS SECTION						
V_{CC_OP}	VCC Operation Range	—	3	—	5.5	V
V_{CC_POR}	VCC Power-on Reset Voltage	—	2.0	—	3.1	V
$V_{CC\_POR\ HYS}$	VCC Power-on Hysteresis	—	—	0.1	—	V
I_{SM}	Sleep Mode Current	V_{CC} = 5V @ sleep mode	150	—	1200	μA
I_{CC_OP}	Operating Supply Current	—	1.1	—	3.0	mA
I_{S_SCL}	Sink Current of SCL for impedance check	V_{SCL} = 1V	760	840	920	μA
V_{2V}	Internal Reference Voltage	2.046±5%	1.944	2.046	2.148	V
CLK_{12M}	Internal Clock Frequency	12MHz±10%	10.8	12	13.2	MHz
CC1/CC2 PIN SECTION						
V_{OH_open}	Pull High Voltage of CCx	—	3.4	3.6	3.8	V
I_{rp_330}	Source Current of CCx	R_D = 5.1KΩ	305	330	355	μA
V_{SW_TxDC}	Voltage Swing of CCx for BMC Tx	R_D = 5.1KΩ	1.05	1.125	1.2	V
V_{SW_TxDCL}	Low Voltage Swing of CCx for BMC Tx	R_D = 5.1KΩ	0	--	75	mV
R_{VCONN}	Rds_on of internal Vconn switch			15		Ω
DN/DP PIN SECTION						
V_{DP_APP}	DP Apple mode output voltage	—	2.52	2.8	3.08	V
V_{DN_APP}	DN Apple mode output voltage	—	2.52	2.8	3.08	V
D_{P_DWM20K}	DP 20K pull down resistor	—	18	20	22	kΩ
D_{N_DWM20K}	DN 20K pull down resistor	—	18	20	22	kΩ
$D_{P\_DWM900K}$	DP 900K pull down resistor	—	600	—	1400	kΩ
$D_{N\_DWM900K}$	DN 900K pull down resistor	—	600	—	1400	kΩ
R_{DPDN_short}	DPDN short resistor	—	5	20	40	Ω
R_{DN_IMP}	Impedance check of DN for attach function	—	100	—	350	Ω
DIGITAL I/O PIN SECTION (DP/DN/GPIO1~GPIO8)						
V_{OH}	Logic Output High Level Voltage	Source Current 4mA	V_{CC}-0.2	—	—	V
V_{OL}	Logic Output Low Level Voltage	Sink Current 4mA	—	—	200	mV
I_{S_OTP}	Source Current for OTP Pins (GPIO3 and GPIO4)	—	126	140	154	μA
ADC SECTION						
V_{ADC_REF}	ADC Reference Voltage	—	—	2.046	—	V
V_{OFFSET}	ADC Offset Voltage	—	—	±4.0	—	mV
PROTECTION SECTION						
V_{DP_OVP}	VABCV$_{DP_OVP}$	V_{DP_OVP}	4.1	4.35	4.6	V
V_{DN_OVP}	V_{DN_OVP}	V_{DN_OVP}	4.1	4.35	4.6	V
I_{VCONN_OCP}	VCONN Overcurrent Protection	—	32	48	56	mA

Ordering Information

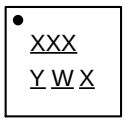


Orderable Part Number	Package (Note 6)	Marking ID	Packing		
			Quantity	Carrier	Part Number Suffix
AP43776QZDZW20-13	W-QFN4040-20 (SWP) (Type A1)	B4Q	3,000	13'' Tape and Reel	-13

Note: 6. For packaging details, go to our website at https://www.diodes.com/design/support/packaging/diodes-packaging/.

Marking Information

(Top View)

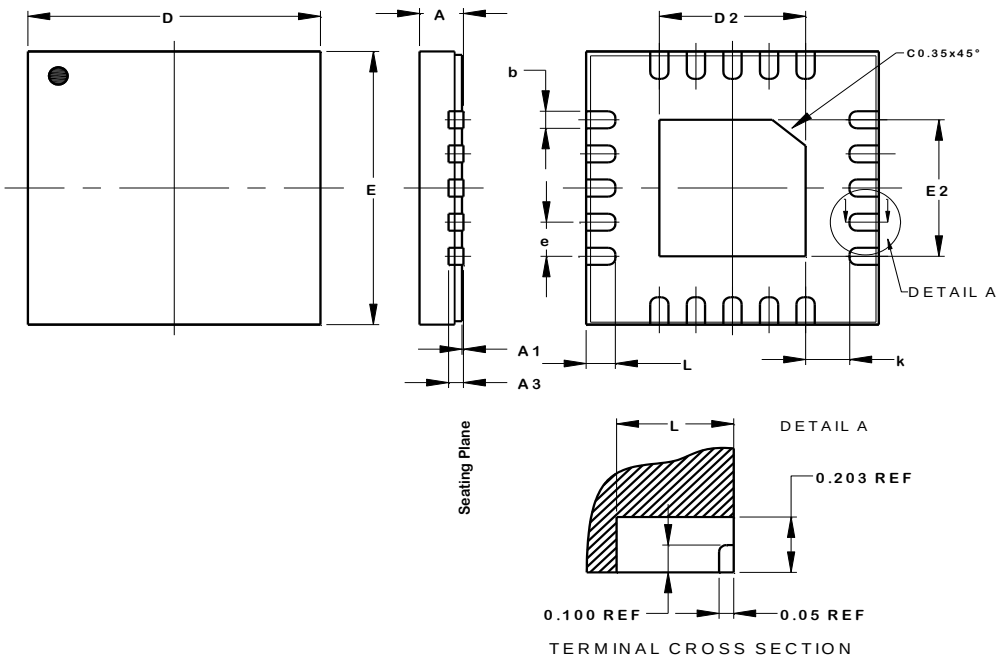


XX : Identification Code
Y : Year : 0~9
W : Week : A~Z : 1~26 week; a~z : 27~52 week; z represents 52 and 53 week
X : Internal Code

Package Outline Dimensions

Please see http://www.diodes.com/package-outlines.html for the latest version.

W-QFN4040-20 (SWP) (Type A1)



W-QFN4040-20 (SWP) (Type A1)			
Dim	Min	Max	Typ
A	0.70	0.80	0.75
A1	0.00	0.05	0.02
A3	0.203 REF		
b	0.20	0.30	0.25
D	4.00 BSC		
D2	1.95	2.05	2.00
E	4.00 BSC		
E2	1.95	2.05	2.00
e	0.50 BSC		
k	0.20	--	--
L	0.30	0.50	0.40
All Dimensions in mm			

Suggested Pad Layout

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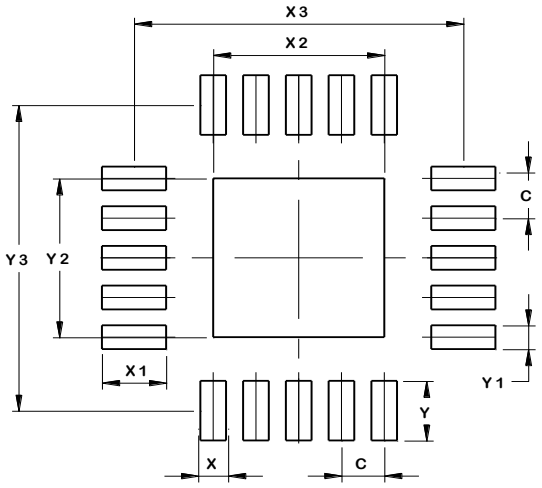
W-QFN4040-20 (SWP) (Type A1)



Dimensions	Value (in mm)
C	0.500
X	0.300
X1	0.750
X2	2.000
X3	3.850
Y	0.750
Y1	0.300
Y2	2.000
Y3	3.850

Mechanical Data

- Moisture Sensitivity: Level 1 per JESD22-A113
- Terminals: Finish – Matte Tin Plated Leads, Solderable per JESD22-B102 (e3)
- Weight: 0.0408 grams (Approximate)

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