USB PD CONTROLLER SUPPORTING DISPLAYPORT OVER TYPE-C ALTERNATE MODE

Description

The AP43781 is a highly integrated USB Type-C® power delivery controller targeted for monitor or TV power board with USB Type-C ports. It supports USB power delivery specification Rev3.1 SPR (Standard Power Range) with full range of programmable power supply (PPS).

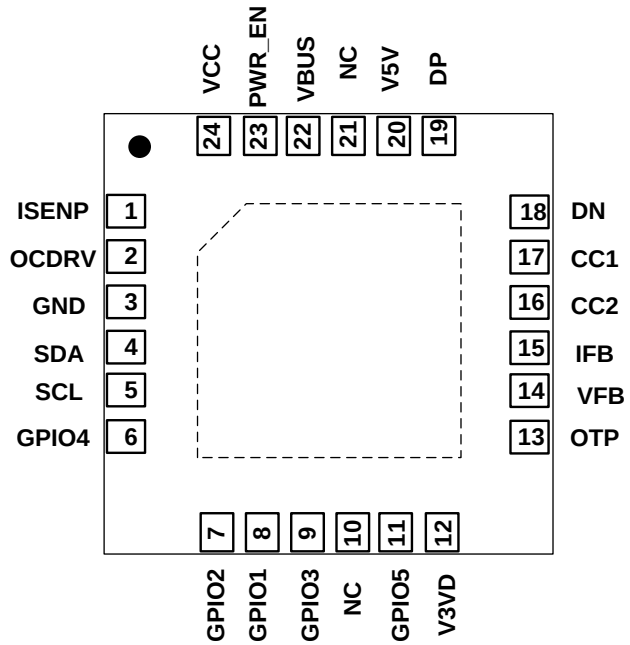
The AP43781 can support PPS APDO (Augmented Power Data Object) with resolution of 20mV/step in voltage and 50mA/step in current. In addition, cable-loss compensation and e-Marker detection are provided.

After the power negotiation is established, AP43781 can support DisplayPort™ by decoding out the CC signal and then deliver the routing control and signaling information to the high-speed switches and the re-driver/re-timer ICs through I2C interface, where the I2C bus can be assigned as master or slave, and GPIO pins can be programmed for different applications.

The AP43781 can offer comprehensive safety protection schemes, including overvoltage protection (OVP), undervoltage protection (UVP), overcurrent protection (OCP), short-circuit protection (SCP) and/or overtemperature protection (OTP).

A one-time programmable ROM is provided for main firmware, and a multi-time programmable ROM is provided for user configuration data.

Pin Assignments



W-QFN4040-24 (Type A1)

Features

- Compatible with USB PD Rev3.1 SPR
- Support Full Range of PPS 3.3V to 21V with Resolution of 20mV/Step in Voltage and 50mA/Step in Current.
- Support Type-C Alternative Mode for DisplayPort
- Built-in Regulator for CV and CC Control
- Support OVP/UVP/OCP/SCP/OTP with Auto Restart
- Support Power Saving Mode
- Driver for Output Enable nMOS Switch
- Support E-Marker Cable Detection
- Support I2C Interface with Master and Slave Flexibility
- Operating Voltage Range: 3.3V to 24V
- OTP (One-Time Programmable) for Main Firmware
- MTP (Multi-Time Programmable) for System Configuration
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**
- **For automotive applications requiring specific change control (i.e. parts qualified to AEC-Q100/101/104/200, PPAP capable, and manufactured in IATF 16949 certified facilities), please contact us or your local Diodes representative. https://www.diodes.com/quality/product-definitions/**

Applications

- Monitors with Type-C ports
- TV power boards with Type-C ports

Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

Typical Applications Circuit

The AP43781 not only supports USB PD power profile negotiation with the sink controller, but also provides the data link capability to the sink device. Figure 1 illustrates how the AP43781 of the CLM (Type-C-Link-to-Monitor) module is used to play as a PD power source controller with support for DisplayPort application.

When the Type-C attachment is completed between an active CLM module and the NB host, the power profile negotiation is started through the CC commands. After the negotiation is completed, the AP43781 will enable the buck-boost controller to provide the matched power to the NB host.

At the same time, the AP43781 plays as a data down-facing port, and enters the alternative mode support by decoding out the VDM (Vendor Defined Message) CC commands delivered from NB host side. The decoded information is then sent out through the I2C interface to the high-speed switches (i.e. PI3USB31531) and signaling chips (i.e. PI3DPX1207C), so that the data stream can be delivered from host side to the DisplayPort at the right routing path and with correct signaling accordingly.

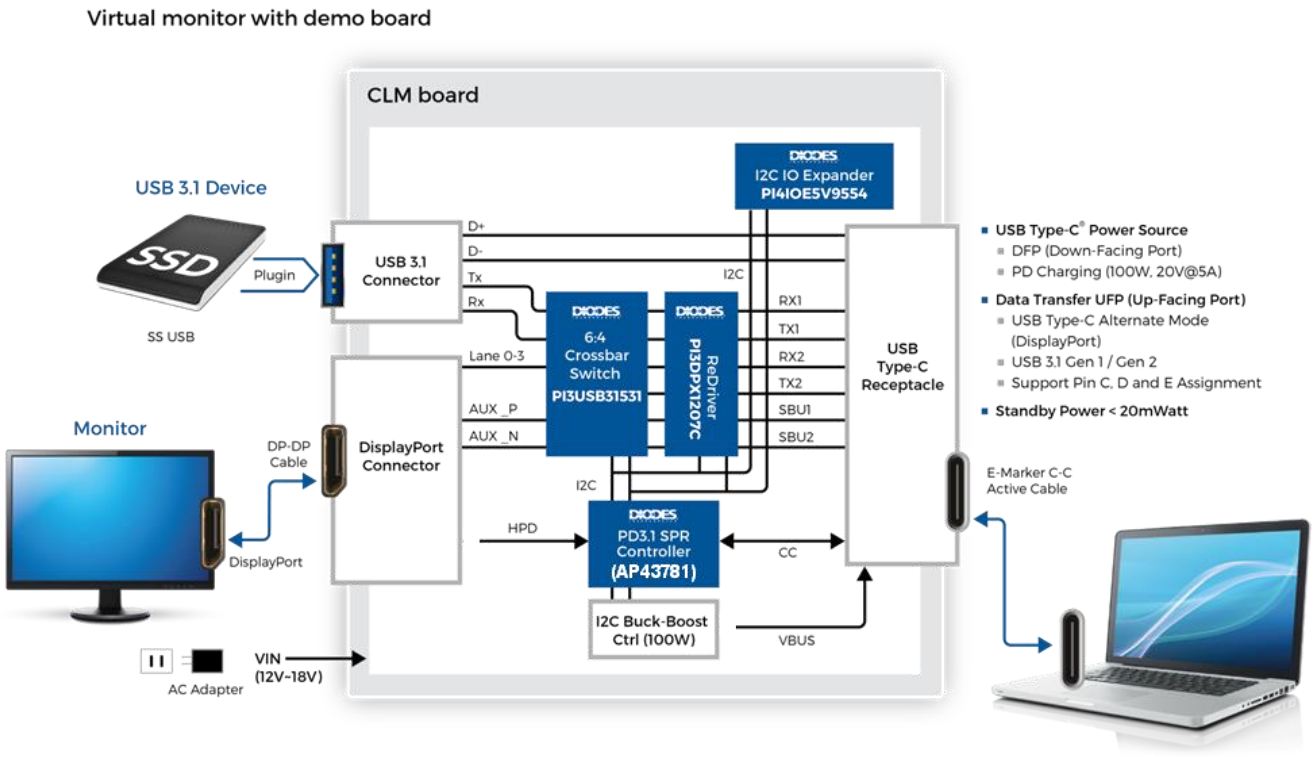


Figure 1. The AP43781 Supports DP Alternative Mode for Data Link During the Power Sourcing

Pin Descriptions

Pin Number	Pin Name	Function
1	ISENP	Input Current Sense Positive Node
2	OCDRV	CC/CV Output. Open-Drain Output for Optocoupler.
3	GND	Ground
4	SDA	GPIO/I2C Data
5	SCL	GPIO/I2C Clock
6	GPIO4	General-Purpose Input or Output
7	GPIO2	General-Purpose Input or Output
8	GPIO1	General-Purpose Input or Output
9	GPIO3	General-Purpose Input or Output
10	NC	No Connection
11	GPIO5	General-Purpose Input or Output
12	V3VD	LDO-3V Output
13	OTP	Source Current to External NTC Sensor for OTP (Overtemperature Protection). Current amplitude is programmable.
14	VFB	CV Input. Negative Node of CV OPAMP for Optocoupler.
15	IFB	CC Input. Negative Node of CC OPAMP for Optocoupler.
16	CC2	Type-C_CC2
17	CC1	Type-C_CC1
18	DN	Type-C_DN
19	DP	Type-C_DP
20	V5V	LDO-5V Output, Connected to a Decoupling Capacitor.
21	NC	No Connection
22	VBUS	Output Terminal for Discharge Path
23	PWR_EN	External nMOS Gate Driver. To control external MOS switch, 1: To enable VBUS voltage. 0: Disconnect VBUS.
24	VCC	The Power Supply of the IC, Connected to a Ceramic Capacitor.

Table 1. The AP43781 Pinout Description

Functional Block Diagram

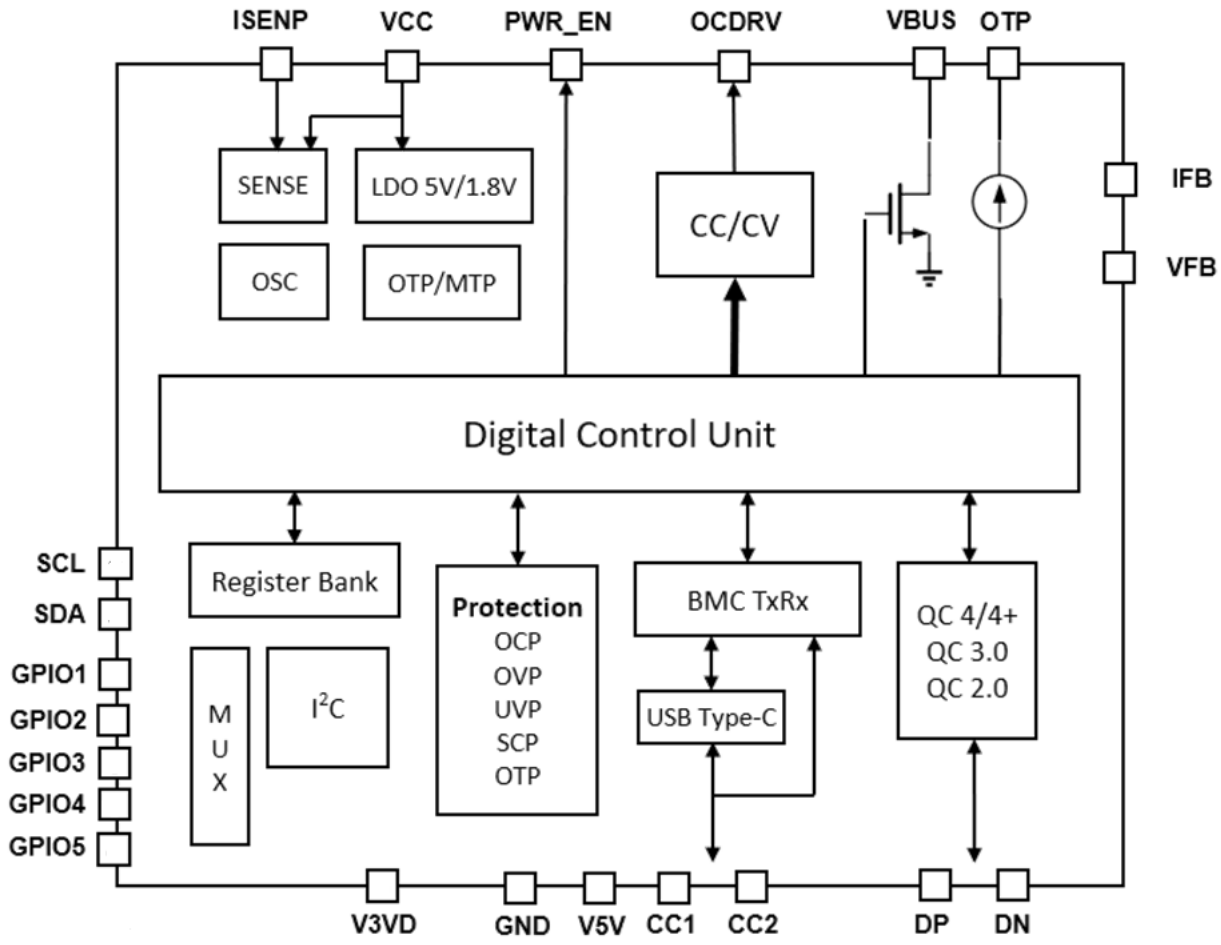


Figure 2. The AP43781 Block Diagram

Absolute Maximum Ratings (Note 4)

Symbol	Parameter	Rating		Unit
V_{VCC}	Input Voltage at VCC Pin	-0.3 to 24		V
V_{VFB}, V_{IFB}, V_{OTP}	Input Voltage at VFB, IFB, OTP Pins	-0.3 to 7		V
V_{VBUS}, V_{PWR_EN}, V_{ISENP}, V_{OCDRV}	Input Voltage at VBUS, PWR_EN, ISENP, OCDRV Pins	-0.3 to 24		V
—	Voltage from PWR_EN to VCC Pin	-16 to 7		V
V_{V5V}	Input Voltage at V5V Pin	-0.3 to 7		V
V_{CC1}, V_{CC2}	Input Voltage at CC1, CC2 Pins	-0.3 to 7		V
V_{DP}, V_{DN}	Input Voltage at DP, DN Pins	-0.3 to 7		V
V_{GPIO1} - V_{GPIO5}, V_{SDA}, V_{SCL}	Input Voltage at GPIO1-5, SDA, SCL Pins (Note 5)	-0.3 to 5		V
T_J	Operating Junction Temperature	-40 to +150		°C
T_{STG}	Storage Temperature	-65 to +150		°C
T_{LEAD}	Lead Temperature (Soldering, 10s)	+300		°C
θ_{JA}	Thermal Resistance (Junction to Ambient) (Note 6)	W-QFN4040-24 (Type A1)	28	°C/W
θ_{JC}	Thermal Resistance (Junction to Case) (Note 6)	W-QFN4040-24 (Type A1)	16	°C/W
—	ESD (Human Body Model) Voltage on DP, DN Pins	6		kV
—	ESD (Human Body Model) Voltage on VBUS, ISENP, PWR_EN, VCC, OCDRV, OTP, V5V, IFB, VFB, CC1, CC2 Pins	2		kV
—	ESD (Charged Device Model)	750		V

Notes: 4. Stresses greater than those listed under *Absolute Maximum Ratings* can cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to *Absolute Maximum Ratings* for extended periods can affect device reliability.
5. When GPIO1-5, SDA, and SCL pins are pulled high to a voltage source, it is strongly recommended to series a resistor with minimum 10k value.
6. Test condition: device mounted on FR-4 substrate PC board, 2oz copper, with the minimum footprint.

Recommended Operating Conditions

Symbol	Parameter	Min	Max	Unit
V_{VCC}	Power Supply Voltage	3.3	24	V
T_{OP}	Operating Temperature Range	-40	+85	°C

Electrical Characteristics (@T_A = +25°C, unless otherwise specified.)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
VCC PIN SECTION						
V_{ST}	Startup Voltage	—	2.5	2.8	3.2	V
V_{UVLO}	Minimum Operating Voltage	—	2.4	2.7	3	V
V_{VCC_HYS}	V_{VCC} Hysteresis (V_{ST}-V_{UVLO})	—	0.05	—	—	V
$I_{VCC\_DEEP\ SLEEP}$	V_{IN} Current in Deep Sleep Mode	CC1/2 Detach after 3s V_{VCC} = 5V	—	550	900	μA
I_{VCC_OPR}	Operating Supply Current	V_{VCC} = 5V	—	3.3	6	mA
VOLTAGE CONTROL LOOP SECTION						
V_{REF_CV5}	Reference Voltage for 5V CV Control	—	4.85	5	5.15	V
V_{REF_CV9}	Reference Voltage for 9V CV Control	—	8.73	9	9.27	V
V_{REF_CV12}	Reference Voltage for 12V CV Control	—	11.64	12	12.36	V
V_{CABLE}	Cable Compensation (Note 7)	—	22	32	42	mV/A
I_{OS}	Maximum OCDRV Pin Sink Current	V_{OUT} = 5V	10	16	30	mA
PROTECTION FUNCTION SECTION						
V_{OVP5V}	OVP_5V Enable Voltage (Note 8)	—	5.6	6	6.8	V
V_{OVP9V}	OVP_9V Enable Voltage (Note 8)	—	9.9	10.8	12.1	V
V_{OVP12V}	OVP_12V Enable Voltage (Note 8)	—	13.2	14.4	16.2	V
$t_{DEBOUNCE\_OVP}$	OVP Debounce Time (Note 9)	—	—	90	—	ms
V_{UVP5V}	UVP_5V Enable Voltage	—	3.3	3.7	4.4	V
V_{UVP9V}	UVP_9V Enable Voltage	—	5.9	6.8	7.7	V
V_{UVP12V}	UVP_12V Enable Voltage	—	7.9	9.1	10	V
I_{OVD}	Overvoltage Discharge Current	V_{VCC} = 5V	150	200	250	mA
t_{OCP}	OCP Deglitch Time (Note 10)	—	—	30	—	ms
$t_{RESTART\_INTERVAL\_SCP}$	Restart Interval Time under SCP (Note 10)	—	—	0.8	—	s
T_{OTP}	Internal OTP Temperature (Note 10)	—	—	+140	—	°C
$I_{OTP\_EXTERNAL}$	External OTP Current	—	90	100	110	μA
T_{HYS}	OTP Recovery Hysteresis Temperature (Note 10)	—	—	+25	—	°C
t_{SLEEP}	Enter Sleep Mode Time after Cable Detached (Note 10)	—	—	3	—	s
t_{OV_DELAY}	Delay from OVP Threshold Trip to nMOS Gate Turn-Off (Note 10)	—	—	—	50	μs
t_{UV_DELAY}	Delay from UVP Threshold Trip to nMOS Gate Turn-Off (Note 10)	—	—	30	—	ms
CC1/CC2, DP/DN PIN SECTION						
V_{L_RD3A}	Low Voltage Threshold Used to Distinguish R_D Attached or Detached for 3A Delivery	—	—	1.35	—	V
V_{H_RD3A}	High Voltage Threshold Used to Distinguish R_D Attached or Detached for 3A Delivery	—	—	2.0	—	V
I_{RD3A}	CC1/CC2 Current Source for 3A Advertisement	V_{VCC} = 5V	304	330	356	μA
V_{OVP_DN}	DN Line Overvoltage Protection Threshold	—	4.1	4.5	4.8	V
V_{OVP_DP}	DP Line Overvoltage Protection Threshold	—	4.1	4.5	4.8	V

Notes: 7. Cable compensation voltage can be adjusted by setting from 0 to $V_{CABLE * N}$ (N: 0 to 7).
8. 120% OVP setting & 76% UVP setting.
9. OVP blanking time during V_O transition from high output voltage to low output voltage, such as 9V to 5V, or 12V to 5V.
10. Guaranteed by design.

Performance Characteristics

System Power-On Sequence

Once external power is supplied to the VCC pin, the AP43781 will wake up. All analog control blocks will get ready, and then the digital block and MCU engine will start initialization flow. After the power-on initialization, the system closed loop is established by the AP43781 and the power module is ready for the Type-C PD negotiation process.

CC Logic and V_{CONN} Switch

For the USB Type-C solution, two pins on the connector, CC1 and CC2, are used to establish and manage the Source-to-Sink connection, as shown in Figure 3. The CC1/CC2 voltage will be changed due to the resistor loading effect of source Rp / current source and sink Rd during the cable insertion. The AP43781 can then detect the voltage range and decide if the cable is attached, detached, or e-Marker embedded.

Once the cable is connected, both parties will negotiate which side will act as a Source or Sink by periodically changing the impedance on CC pin. The Source side will assign a pullup resistor / current source on its CC pin, and the Sink side will connect a pulldown resistor on CC pin. The AP43781 in this application will play as a Source to offer power to the Sink device, so a pullup resistor / current source is assigned on the CC pin. After the Source to Sink connection is built up, the V_{CONN} switch is turned on by Source to feed power to the cable through unconnected CC pin as well. At the same time, the Type-C plug orientation can be detected by monitoring the voltage on CC pins (CC1 or CC2), and then the data path from Source to Sink is accomplished.

After the attachment, the VBUS can be supplied 5V power from Source by turning on the VBUS switch, and its current capability is assigned by the pullup resistor / current source on its CC pin.

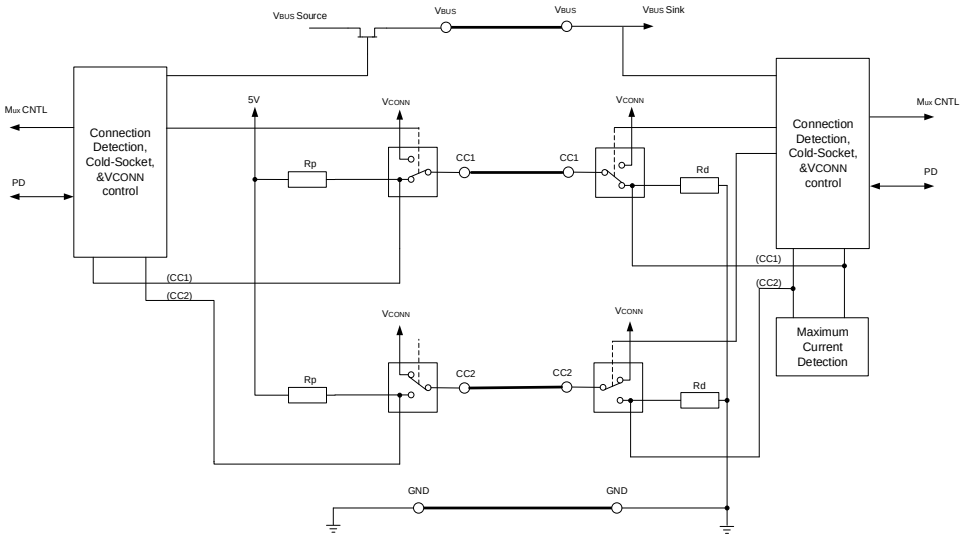


Figure 3. The USB Type-C CC Logic and V_{CONN} Switch

USB Power Delivery (PD) and Phy

The AP43781 supports PD communication over USB Type-C CC channel for advanced power delivery negotiation. A USB PD physical layer that consists of pair of transmitter and receiver for Biphase Marked Coding (BMC) packet communication are embedded.

The transmitter functions include receiving packet data from the protocol layer, calculating a CRC and appending, BMC encoding, packetizing and transmitting on the CC channel. The receiver functions perform clock recovering from preamble, packet start detecting, BMC decoding, packet data recovering, CRC validating, packet delivering to the protocol layer or dropping.

The AP43781 is compliant with the USB Power Delivery (PD) specification Rev3.1 supporting full range of Programmable Power Supply (PPS) up to 21V.

Performance Characteristics (continued)

Voltage Transition

When the sink and source make an acceptable power request deal, the AP43781 will provide the VBUS with the requested voltage and current capability through the VFB control feedback or I2C communication to the DC/DC controller. During the voltage transition, the feedback system stability of AP43781 and DC/DC controller should be carefully designed to guarantee monotonic voltage transition and avoid violating USB PD electrical specification.

DisplayPort Alternate Mode Support

After the PDO negotiation is completed, the AP43781 plays as a data Upstream Facing Port (UFP), and enter the alternative mode support by decoding out the VDM (Vendor Defined Message) commands delivered by the host side. The AP43781 supports DisplayPort Alternate Mode on USB Type-C standard with Discover Identify, Discover SVIDs, Discover Modes, Enter Mode, DP Status, DP Configure, and Exit Mode. The decoded information is then sent out to the high-speed switches (i.e. PI3USB31531) and signaling chips (i.e. PI3DPX1207C) through the I2C interface, so that the data stream can be delivered from host side to the DisplayPort at the right routing path and correct signaling accordingly.

CV/CC Control Loop

The AP43771V uses Constant Voltage (CV) and Constant Current (CC) functions to control the output voltage and current as shown in Figure 4, where both loops are connected at OCDRV pin, and the feedback signal is photo-coupled from the PD controller to the primary power stage.

The CV loop regulates the output to be the expected voltage by sensing VCC through resistor divider to VFB and comparing it with a predetermined voltage set by a DAC converter. The signal difference drives OCDRV to control a photo coupler to the power stage, and then a negative feedback loop is accomplished to regulate VCC to the expected voltage. Here the DAC is used to set the expected VCC output voltage.

The CC loop controls the output to be the expected constant current by sensing the I*Rsense drop on voltage output and comparing IFB with a predetermined voltage set by a DAC converter. The signal difference drives OCDRV to control a photo coupler to the power stage, and then a negative feedback loop is completed to adjust the I*Rsense drop to be equal to the DAC setting. Thereby the corresponding constant current is obtained.

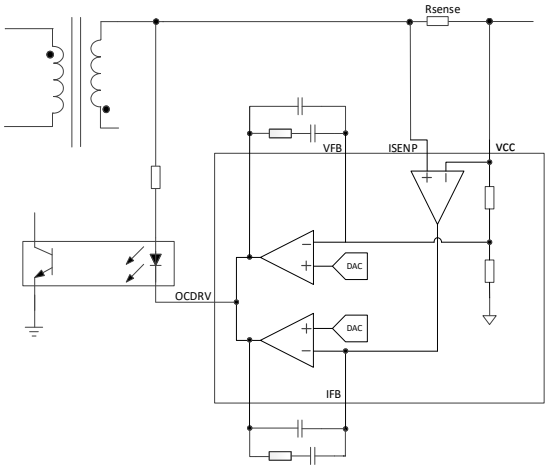


Figure 4. The CC/CV Control Loop in AP43781

Protection

The AP43781 provides OVP/UVP/OCP/SCP/OTP functions and supports Constant Current (CC) function. All the protection thresholds depend on the requested power profile and provide the most reliable protection scheme.

The AP43781 provides OVP feature by turning off the power switch when V_{BUS} is higher than OVP enable voltage. Meanwhile, it provides an internal discharge path to reduce the overvoltage duration and terminates discharge current as soon as V_{BUS} reaches the target voltage. To prevent the VBUS pin from working abnormally, the AP43781 provides UVP function whenever V_{BUS} drops to UVP enable voltage.

To ensure the safe operation of USB PD, the AP43781 provides programmable OCP function to make sure output current will not be higher than the allowed maximum current. Once OCP conditions happen, the AP43781 will shut down the USB PD system and send “Hard Reset” to the host side.

Performance Characteristics (continued)

MCU and OTP/MTP ROM

The AP43781 has an MCU subsystem, which integrates an 8-bit 8051 processor, SRAM, and OTP ROM. The MCU subsystem is optimized for user configurability of different topologies, supporting different protocols, and low-power consumption at a low cost. With the embedded hardware PHY transceivers offloading MCU processing, the AP43781 can handle PD handshakes efficiently, and be compliant with critical USB Power Delivery specifications.

An OTP ROM is provided to store PD, QC, and FCP protocol firmware, and an MTP ROM is provided for user configuration table. Either in-system programming or offline socket programming are provided for the OTP ROM and MTP ROM.

I2C Interface

The I2C interface pins (SCK, SDA), as shown in below Table 2, are used to communicate between the PD decoder and DC/DC controller/converter to replace analog signal feedback of VFB with much higher noise immunity. I2C commands are supported by firmware so that it can monitors and changes status of other I2C devices

Pin No.	Pin Name	Pin Function
4	SDA	I2C Data
5	SCL	I2C Clock

Table 2. I2C Interface of the AP43781 Supports Both Master and Slave Modes

The AP43871 can play as an I2C master or slave device. The I2C read and write operations are supported as below.

All transactions begin with a START (S) and be terminated by a STOP (P). A START condition is defined whenever a HIGH to LOW transition on the SDA while SCL is HIGH. A STOP condition is defined whenever a LOW to HIGH transition on the SDA while SCL is HIGH. The START and STOP conditions are always generated by the master.

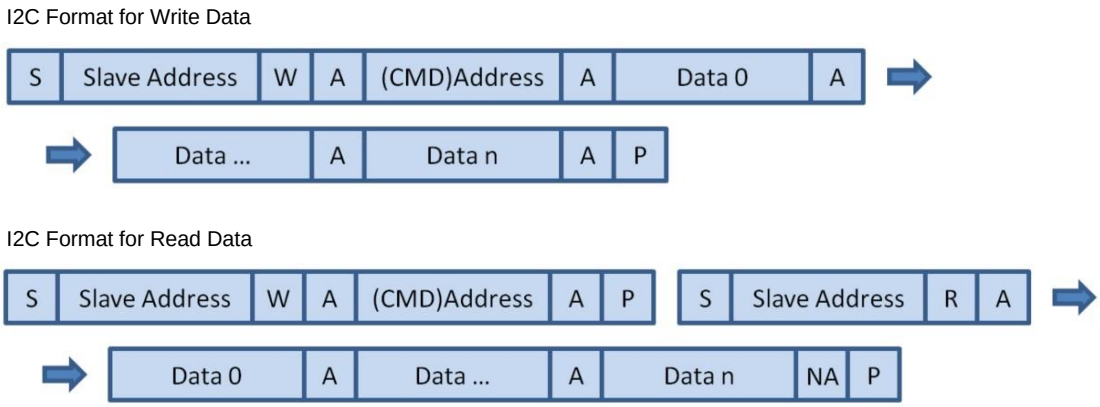


Figure 5. The I2C Command Format in AP43781

Performance Characteristics (continued)

GPIO Support

There are many GPIO pins that can be used to support customization features, LED light indication, fault status, and so on. The GPIO pin can also be used for UART communication to master MCU, and some GPIOs support current sources for external NTC temperature detection.

Below Figure 6 is the equivalent structure of GPIO pin. Q1 to Q4 can be enabled/disabled flexibly by firmware for input or output application scenario. GPIO 3/4 have a controlled 100μA current source which can be connected to pin output for temperature sensing with an output NTC.

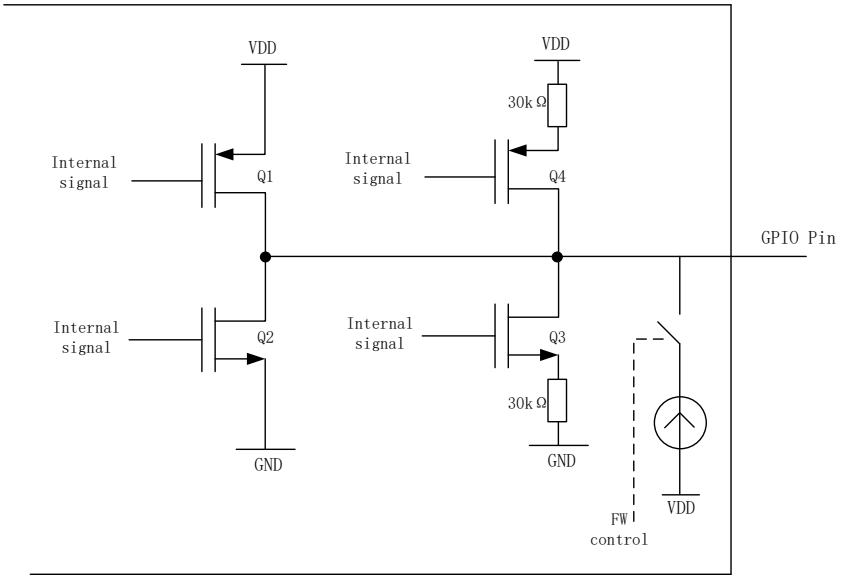


Figure 6. The Structure of GPIO Pin in AP43781

Below Table 3 summarized the GPIO configuration for different applications. The maximum output voltage of GPIO pin is 5V, suggest to full high to 3.3V voltage source if necessary.

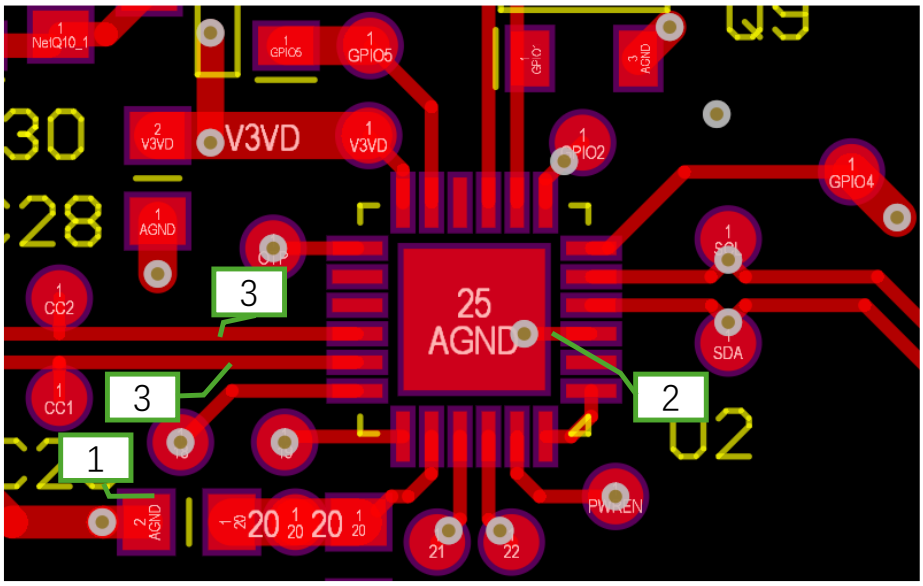
PIN	GPIO configuration for output	GPIO configuration for input	GPIO configuration for temperature sensing	Maximum Output
GPIO1	Q3/Q4 disabled internally, No need pull high and pull low externally	Q1/Q2 disabled , Default 30kΩ pull high internally , suggest 3kΩ pull low externally	-	3.3V
GPIO2	Q3/Q4 disabled internally, No need pull high and pull low externally	Q1/Q2 disabled , Default 30kΩ pull high internally , suggest 3kΩ pull low externally	-	
GPIO3	Q3/Q4 disabled internally, No need pull high and pull low externally	Q1/Q2 disabled , Default 30kΩ pull low internally , suggest 3kΩ pull high externally	-	
GPIO4	Q3/Q4 disabled internally, No need pull high and pull low externally	Q1/Q2 disabled , Default 30kΩ pull low internally , suggest 3kΩ pull high externally	-	
GPIO5	Q3/Q4 disabled internally, No need pull high and pull low externally	Q1/Q2 disabled , Default 30kΩ pull low internally , suggest 3kΩ pull high externally	-	
OTP pin	-	-	Internal 100uA current source connected on pinout, suggest 0~20kΩ NTC pull low externally	

Table 3. Summary of GPIO Configuration

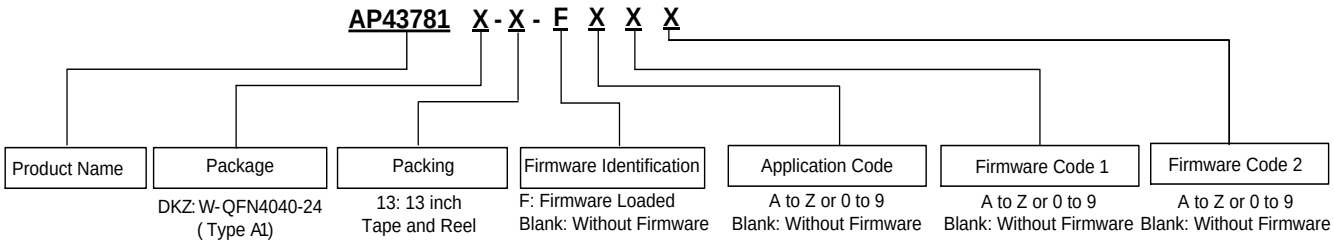
PCB Layout Guideline

Suitable PCB layout is critical for stable operation and better ESD performance. Follow some guidelines as below:

1. Place the V5V decoupling capacitor as close to the pins as possible.
2. The exposed pad of the IC must be connected to GND. It is better for noise immunity.
3. Use traces to connect CC1/CC2 pins to the USB Type-C receptacle as short as possible.



Ordering Information

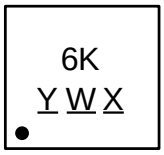


Orderable Part Number	Package	Identification Code	Packing	
			Qty.	Carrier
AP43781DKZ-13-FXXX	W-QFN4040-24 (Type A1)	6K	3000	13” Tape and Reel

Marking Information

W-QFN4040-24 (Type A1)

(Top View)

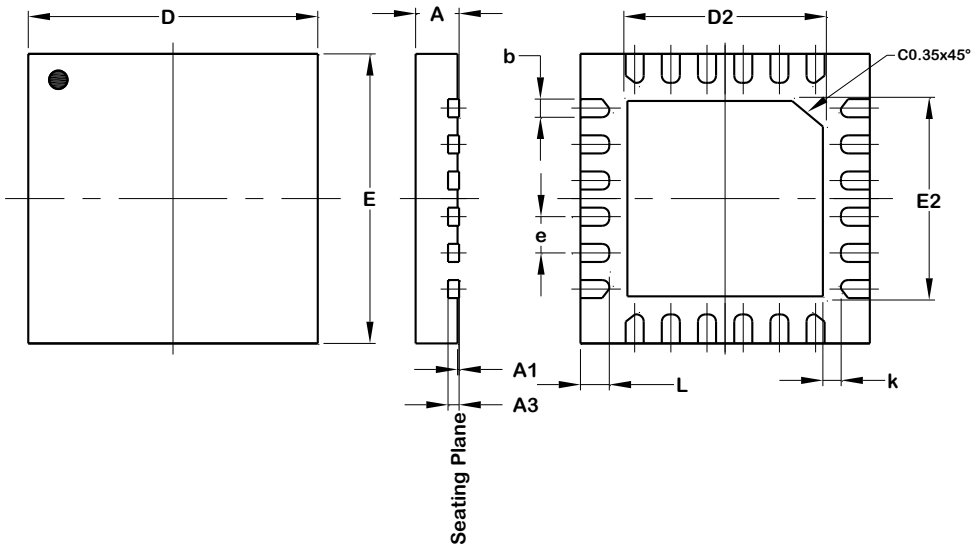


6K : Identification Code
Y : Year : 0 to 9 (ex: 4 = 2024)
W : Week : A to Z : week 1 to 26;
a to z : week 27 to 52; z represents
week 52 and 53
X : Internal Code

Package Outline Dimensions

Please see http://www.diodes.com/package-outlines.html for the latest version.

W-QFN4040-24 (Type A1)

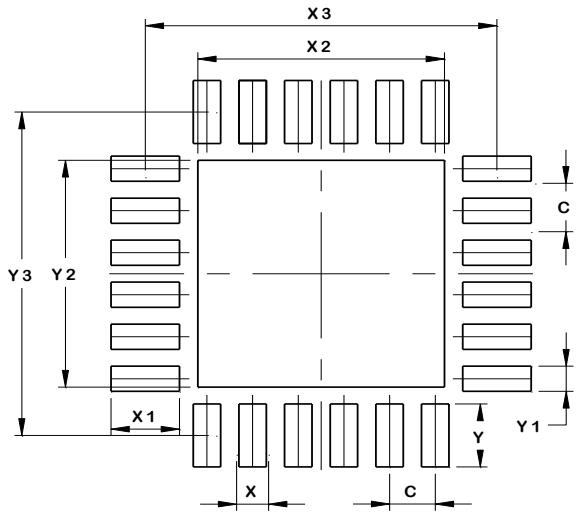


W-QFN4040-24 (Type A1)			
Dim	**Min**	**Max**	**Typ**
A	0.70	0.80	0.75
A1	0.00	0.05	0.02
A3	0.203 REF		
b	0.18	0.30	0.25
D	4.00 BSC		
D2	2.65	2.75	2.70
E	4.00 BSC		
E2	2.65	2.75	2.70
e	0.50 BSC		
k	0.20	--	--
L	0.35	0.45	0.40
All Dimensions in mm			

Suggested Pad Layout

Please see http://www.diodes.com/package-outlines.html for the latest version.

W-QFN4040-24 (Type A1)



Dimensions	Value (in mm)
C	0.500
X	0.300
X1	0.750
X2	2.700
X3	3.850
Y	0.750
Y1	0.300
Y2	2.700
Y3	3.850

Mechanical Data

- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals: Finish – Matte Tin Plated Leads, Solderable per J-STD-202 e3
- Weight: 0.041 grams (Approximate)

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