AUTOMOTIVE COMPLIANT 500mA HIGH-PSRR LOW-NOISE LDO WITH POWER-GOOD INDICATOR

Description

The AP7347EQ is a low-dropout regulator with high output-voltage accuracy, low $R_{DS(ON)}$, high PSRR, low output noise, and low quiescent current. This regulator is based on a CMOS process.

The AP7347EQ includes a voltage reference, error amplifier, current-limit circuit, and an enable input to turn it on and off. With the integrated resistor network, fixed output-voltage version and adjustable output-voltage version can be delivered. The AP7347EQ has power-good indicator.

With its low power consumption and line- and load-transient response, the AP7347EQ is well-suited for noise-sensitive automotive equipment.

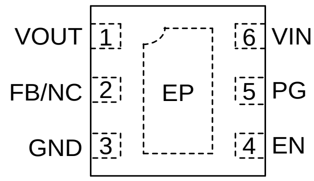
The AP7347EQ is packaged in the U-DFN2020-6 (SWP) (Type UXC) and V-DFN3030-8/SWP (Type UX) packages.

Features

- Low V_{IN} and Wide V_{IN} Range: 1.7V to 5.5V
- Guarantee Output Current: 500mA
- V_{OUT} Accuracy ±1%
- Ripple Rejection 75dB at 1kHz
- Low Output Noise, 60µVrms from 10Hz to 100kHz
- Quiescent Current as Low as 75µA
- Output Voltage Range
  - Fixed: 1.0V to 5.0V
  - Adjustable: 1.0V to 5.0V
- Power-Good (PG) Output for Supply Monitoring and for Sequencing of Other Supplies
- Active Output Discharge
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**
- **The AP7347EQ is suitable for automotive applications requiring specific change control; this part is AEC-Q100 qualified, PPAP capable, and manufactured in IATF 16949 certified facilities.**
  https://www.diodes.com/quality/product-definitions/

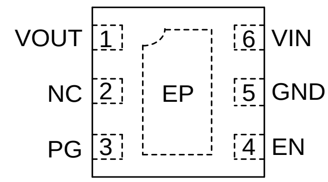
Pin Assignments

(Top View)



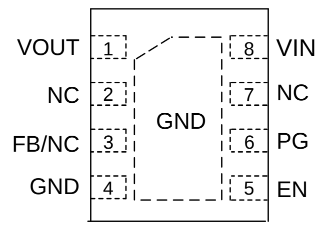
U-DFN2020-6 (SWP) (Type UXC)
(Package Code: FDCW)

(Top View)



U-DFN2020-6 (SWP) (Type UXC)
(Package Code: FDCWR)

(Top View)



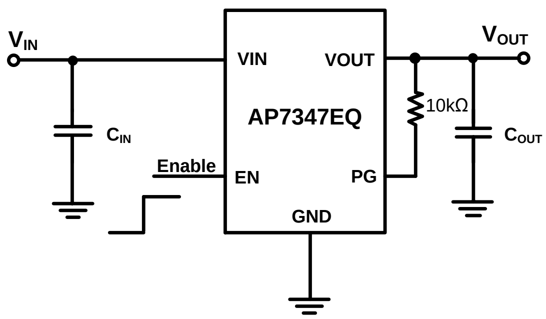
V-DFN3030-8/SWP (Type UX)

Applications

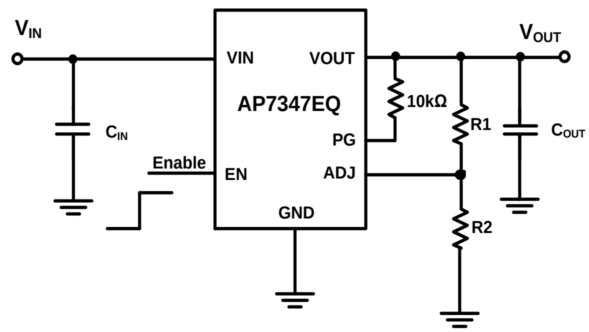
- Infotainment power supplies
- Automotive RF supplies
- Cameras
- Automotive POL in ADAS
- Automotive wireless communication systems

Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

Typical Applications Circuit



AP7347EQ Fixed Version

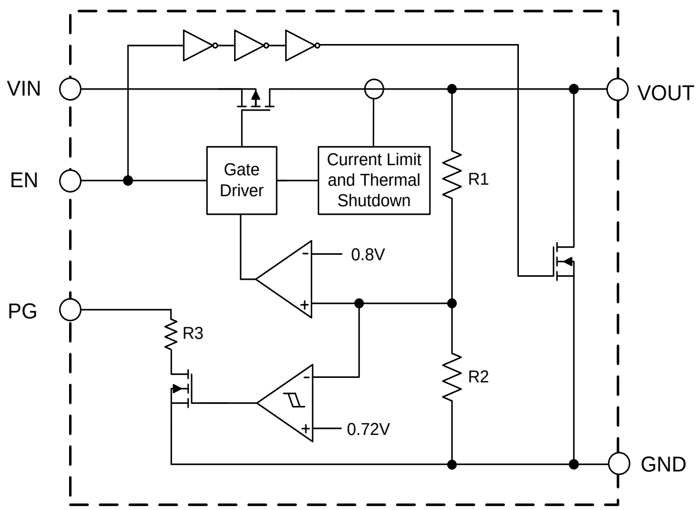


AP7347EQ Adjustable Version

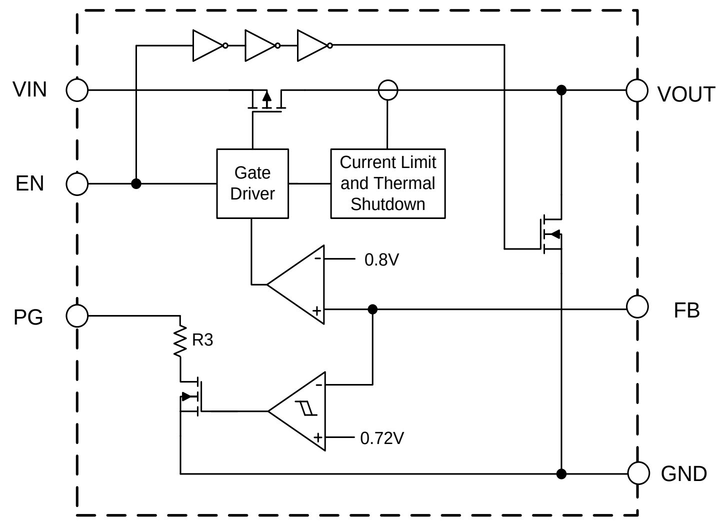
Pin Descriptions

Pin Number			Pin Name	Function
U-DFN2020-6 (SWP) (Type UXC) (Package Code: FDCW)	**UDFN2020-6 (SWP) (Type UXC) (Package Code: FDCWR)**	**V-DFN3030-8/SWP (Type UX)**		
1	1	1	VOUT	Power Output Pin
2	—	3	FB/NC	Adjustable voltage A resistor divider from this pin to the OUT pin and ground sets the output voltage. No Connect Not connected internally; recommended to connect to GND to maximize PCB copper for thermal dissipation.
3	5	4	GND	Ground
4	4	5	EN	Enable Pin This pin should be driven either high or low and must not be floating. Driving this pin high enables the regulator, while pulling it low puts the regulator into shutdown mode.
5	3	6	PG	Power-good pin, open-drain output. When the VOUT is below the PG threshold, the PG pin is driven low; when the VOUT exceeds the threshold, the PG pin goes into a high-impedance state. To use the PG pin, use a 10kΩ to 1MΩ pullup resistor to pull it up to a supply, which can be higher than the input voltage.
6	6	8	VIN	Power Input Pin
—	2	2, 7	NC	No Connect Not connected internally; recommended to connect to GND to maximize PCB copper for thermal dissipation.
EP	EP	EP	Expose Pad	In PCB layout, prefer to use large copper area to cover this pad for better thermal dissipation, then connect this area to GND or leave it open. However, do not use it as GND electrode function alone.

Functional Block Diagram



AP7347EQ Fixed Version



AP7347EQ Adjustable Version

Absolute Maximum Ratings (Note 4) (@T_A = +25°C, unless otherwise specified.)

Symbol	Parameter		Ratings	Unit
ESD HBM	Human Body Mode ESD Protection		2	kV
ESD CDM	Charged Device Model		1	kV
V_{IN}	Input Voltage		6.0	V
V_{EN}	Input Voltage for EN Pin		6.0	V
V_{OUT}	Output Voltage		-0.3 to V_{IN} + 0.3	V
I_{OUT}	Output Current		500	mA
P_D	Power Dissipation	U-DFN2020-6 (SWP) (Type UXC)	1.025	W
		V-DFN3030-8/SWP (Type UX)	1.331	
T_A	Operating Ambient Temperature		-40 to +125	°C
T_J	Operating Junction Temperature		-40 to +150	°C
T_{STG}	Storage Temperature		-55 to +150	°C

Notes: 4. a). Stresses beyond those listed under *Absolute Maximum Ratings* can cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to absolute-maximum-rated conditions for extended period can affect device reliability.

b). Ratings apply to ambient temperature at +25°C. The JEDEC STD.51 High-K board design used to derive this data was a 3inch × 3inch multilayer board with 1oz. internal power and ground planes and 2oz. copper traces on the top and bottom of the board.

Recommended Operating Conditions (@T_A = +25°C, unless otherwise specified.)

Symbol	Parameter	Min	Max	Unit
V_{IN}	Input Voltage	1.7	5.5	V
V_{OUT}	Output Voltage	1.0	5.0	V
I_{OUT}	Output Current	0	500	mA
T_J	Operating Junction Temperature	-40	+125	°C

Electrical Characteristics (@T_J = -40°C to +125°C, V_{IN} = V_{OUT} + 1.0V or V_{IN} = V_{OUT} + 0.5 (if V_{OUT} > 4.5V), C_{IN} = C_{OUT} = 1.0µF, I_{OUT} = 1.0mA, unless otherwise specified.)

Parameter	Condition		Min	Typ	Max	Unit
Input Voltage	T_J = -40°C to +125°C		1.7	—	5.5	V
Feedback Voltage	T_J = +25°C		0.792	0.8	0.808	V
	T_J = -40°C to +125°C		0.788	0.8	0.812	
FB Leakage Current	V_{FB} = 0.8V		—	0.1	1	µA
Output-Voltage Accuracy (Note 5)	$V_{OUT}(T)$ ≥ 1.5V, T_J = +25°C		$V_{OUT}(T)$* 0.99	$V_{OUT}(T)$	$V_{OUT}(T)$* 1.01	V
	$V_{OUT}(T)$ ≥ 1.5V, T_J = -40°C to +125°C		$V_{OUT}(T)$* 0.985	$V_{OUT}(T)$	$V_{OUT}(T)$* 1.015	
	$V_{OUT}(T)$ < 1.5V, T_J = +25°C		$V_{OUT}(T)$* 0.99	$V_{OUT}(T)$	$V_{OUT}(T)$* 1.01	
	$V_{OUT}(T)$ < 1.5V, T_J = -40°C to +125°C		$V_{OUT}(T)$- 20mV	$V_{OUT}(T)$	$V_{OUT}(T)$+ 20mV	
Line Regulation ($dV_{OUT}/dV_{IN}/V_{OUT}$)	V_{IN} = ($V_{OUT-Nom}$ + 1.0V) to 5.5V, I_{OUT} = 1.0mA, V_{IN} = 5.3 to 5.5V (if V_{OUT} = 5.5V)		—	0.02	0.1	%/V
Load Regulation	V_{IN} = $V_{OUT-Nom}$ + 1.0V, or V_{IN} = 2.0V (if V_{OUT} ≤ 1V), I_{OUT} = 1mA to 500mA		—	22.5	45	mV
Quiescent Current (Note 6)	I_{OUT} = 0		—	75	140	µA
$I_{STANDBY}$	V_{EN} = 0 (Disabled)		—	0.01	1.0	µA
Output Current	V_{IN} > V_{OUT} + max Dropout, and V_{IN} > 2.0V		500	—	—	mA
Foldback Short Current (Note 7)	V_{OUT} Short to Ground		—	180	400	mA
PSRR (Note 8)	V_{IN} = (V_{OUT} + 1V) V_{DC} + 0.2Vp-pAC, V_{OUT} = 1.0V, I_{OUT} = 50mA	f = 1kHz	—	75	—	dB
Output Noise Voltage (Note 8) (Note 9)	BW = 10Hz to 100kHz, V_{OUT} = 1.0V, I_{OUT} = 50mA		—	60	—	µVrms
Dropout Voltage (Note 10)	I_{OUT} = 500mA	1.0V ≤ V_{OUT} < 1.2V	—	0.75	0.95	V
		1.2V ≤ V_{OUT} < 1.4V	—	0.65	0.80	
		1.4V ≤ V_{OUT} < 1.7V	—	0.55	0.66	
		1.7V ≤ V_{OUT} < 2.1V	—	0.45	0.55	
		2.1V ≤ V_{OUT} < 2.5V	—	0.36	0.42	
		2.5V ≤ V_{OUT} < 3.0V	—	0.31	0.36	
		3.0V ≤ V_{OUT} < 4.0V	—	0.27	0.32	
		4.0V ≤ V_{OUT} < 5.0V	—	0.14	0.32	
Output-Voltage Temperature Coefficient	I_{OUT} = 50mA, T_J = -40°C to +125°C		—	±80	—	ppm/°C

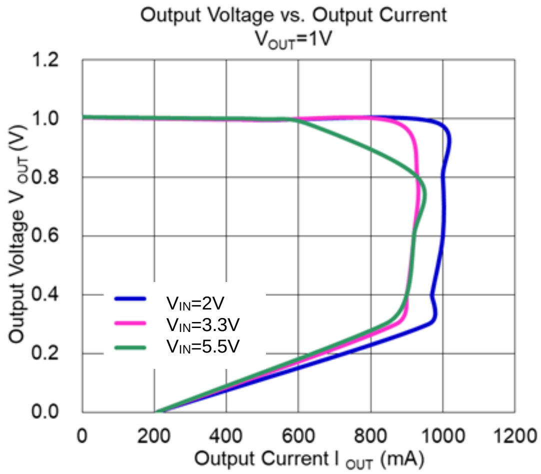
Notes:
5. Potential multiple grades based on following output-voltage accuracy.
6. Quiescent current is defined here is the difference in current between the input and the output.
7. Short-circuit current is measured with V_{OUT} pulled to GND.
8. This specification is guaranteed by design.
9. To make sure lowest environment noise minimizes the influence on noise measurement.
10. Dropout voltage is the voltage difference between the input and the output at which the output voltage drops 2% below its nominal value.

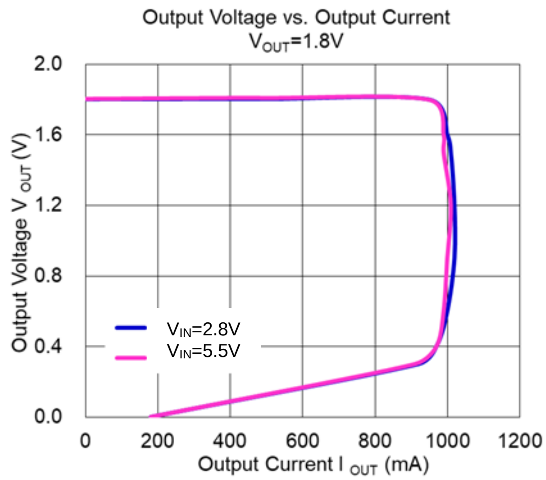
Electrical Characteristics (continued) (@T_J = -40°C to +125°C, V_{IN} = V_{OUT} + 1.0V or V_{IN} = V_{OUT} + 0.5 (if V_{OUT} > 4.5V), C_{IN} = C_{OUT} = 1.0µF, I_{OUT} = 1.0mA, unless otherwise specified.)

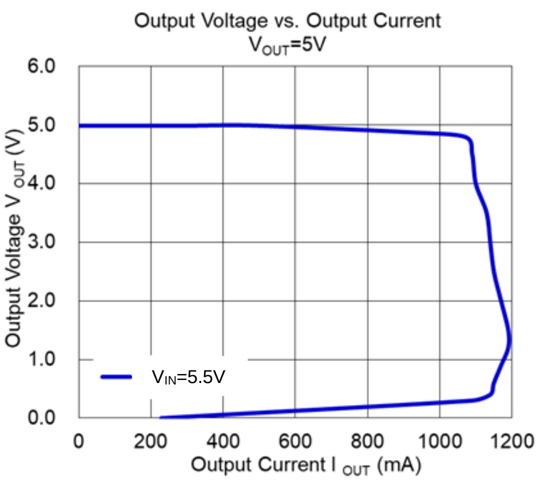
Parameter	Condition	Min	Typ	Max	Unit
EN Input Low Voltage	—	0	—	0.5	V
EN Input High Voltage	—	1.25	—	5.5	V
EN Input Leakage	V_{EN} = 0, V_{IN} = 5.0V or V_{EN} = 5.0V, V_{IN} = 0	-1	—	+1	µA
PG High Threshold_PG_{HTH}	V_{OUT} Increasing	85	—	95	% V_{OUT}
PG Low Threshold_PG_{LTH}	V_{OUT} Decreasing	83	—	93	% V_{OUT}
PG Pin Low-Level Output Voltage	V_{IN} ≥ 1.8V, I_{SINK} = 1mA	—	—	300	mV
	V_{IN} ≥ 2.75V, I_{SINK} = 2mA	—	—	300	
PG Pin Leakage Current (Note 11)	V_{OUT} > PG_{HTH}; V_{PG} = 5.5V	—	—	300	nA
PG Delay Time Rising (Note 11)	Time from PG_{HTH} to 20% of PG	—	100	—	µs
PG Deglitch Time	Time from PG_{HTH} to 80% of PG	—	5	—	µs
On Resistance of N-Channel for Auto-Discharge (Note 10)	V_{IN} = 4.0V, V_{EN} = 0 (Disabled)	—	30	100	Ω
Thermal Shutdown Threshold (TSHDN)	—	—	+170	—	°C
Thermal Shutdown Hysteresis (THYS)	—	—	+20	—	°C
Thermal Resistance Junction to Ambient (θ_{JA}) (Note 4)	U-DFN2020-6 (SWP) (Type UXC)	—	97.5	—	°C/W
	V-DFN3030-8/SWP (Type UX)	—	75.1	—	
Thermal Resistance Junction to Case (θ_{JC}) (Note 4)	U-DFN2020-6 (SWP) (Type UXC)	—	17.5	—	°C/W
	V-DFN3030-8/SWP (Type UX)	—	14.87	—	

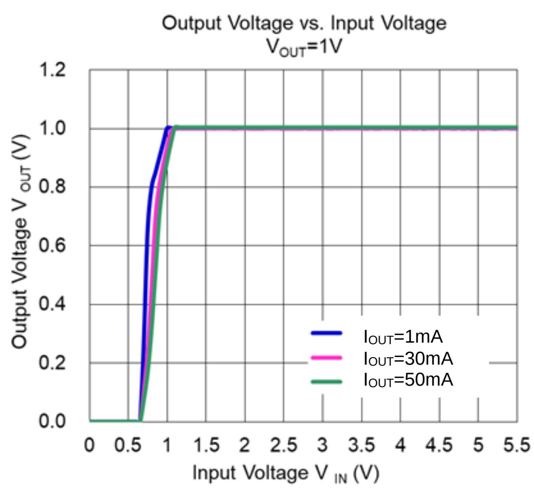
Notes: 4. a). Stresses beyond those listed under *Absolute Maximum Ratings* can cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to absolute-maximum-rated conditions for extended period can affect device reliability.
b). Ratings apply to ambient temperature at +25°C. The JEDEC STD.51 High-K board design used to derive this data was a 3 inch × 3 inch multilayer board with 1oz. internal power and ground planes and 2oz. copper traces on the top and bottom of the board.
10. Dropout voltage is the voltage difference between the input and the output at which the output voltage drops 2% below its nominal value.
11. The PG pullup resistance is 10kΩ.

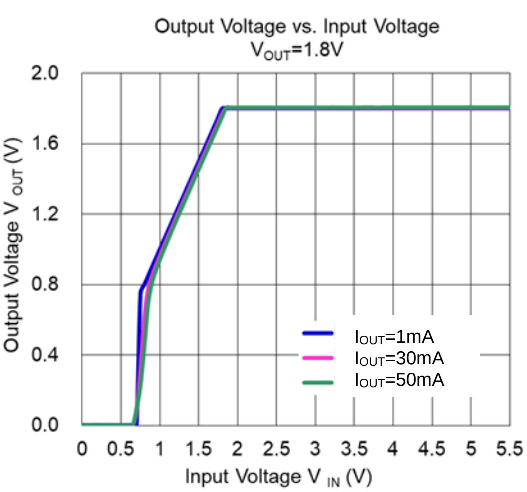
Typical Performance Characteristics

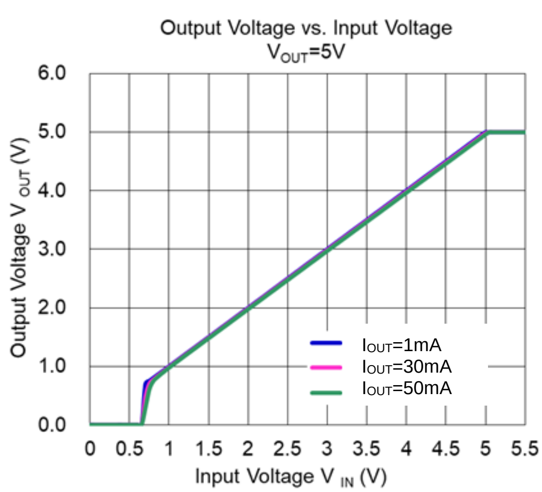




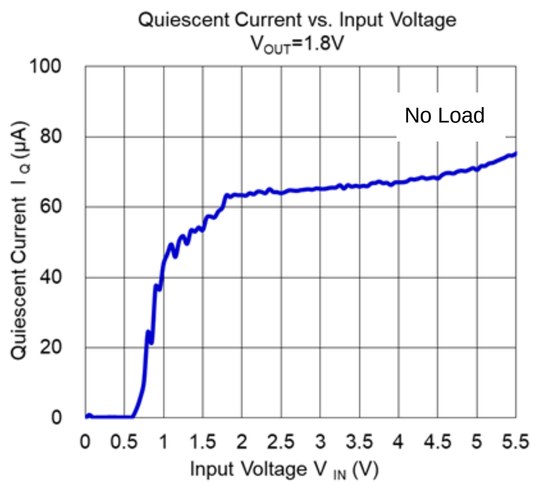


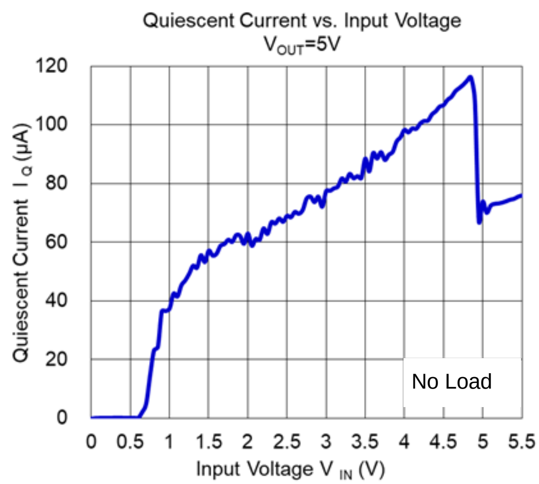


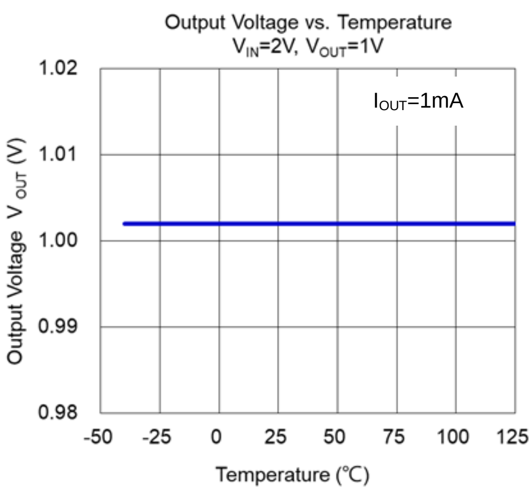


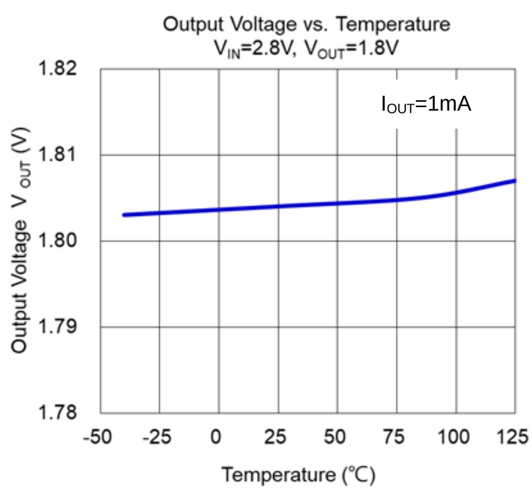


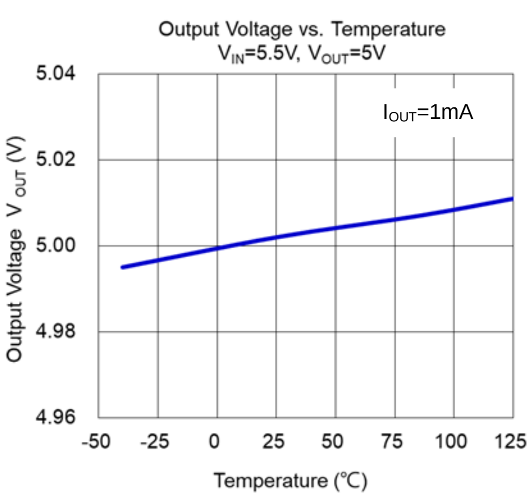
Typical Performance Characteristics (continued)

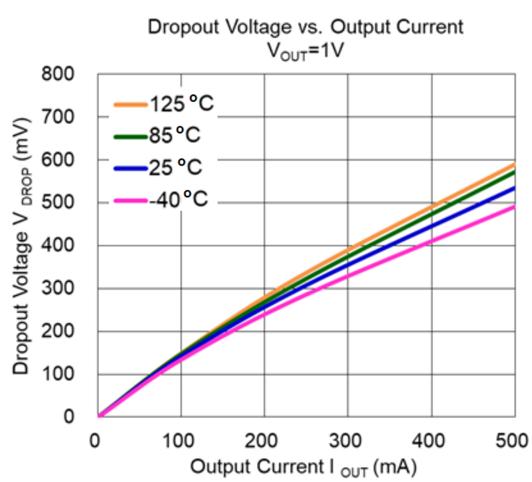




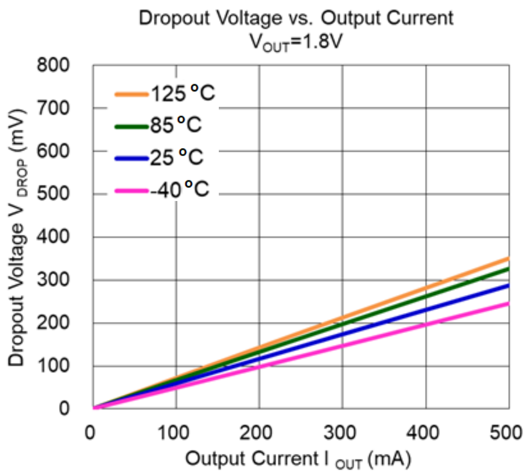


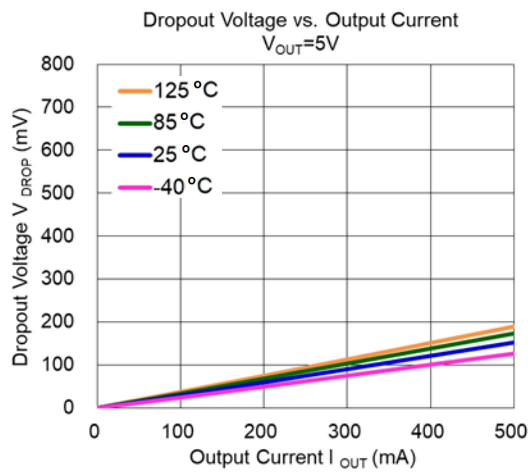


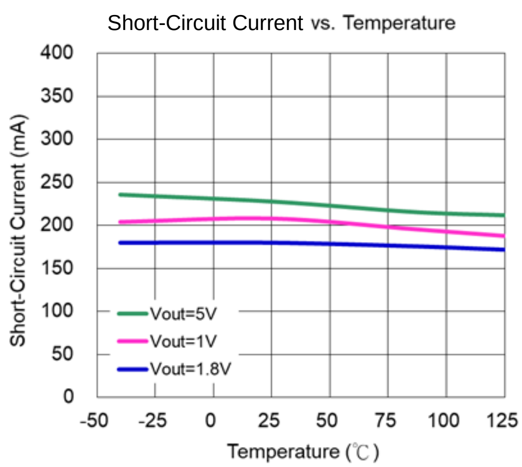


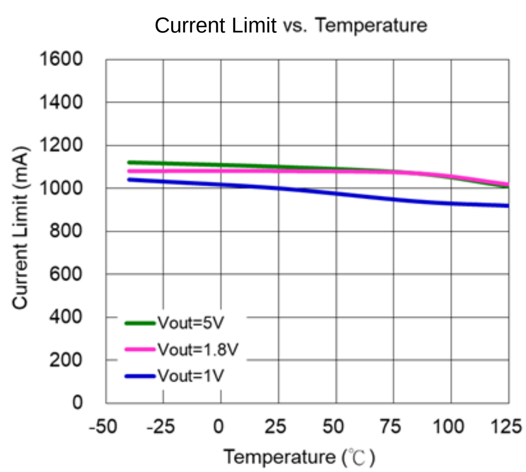


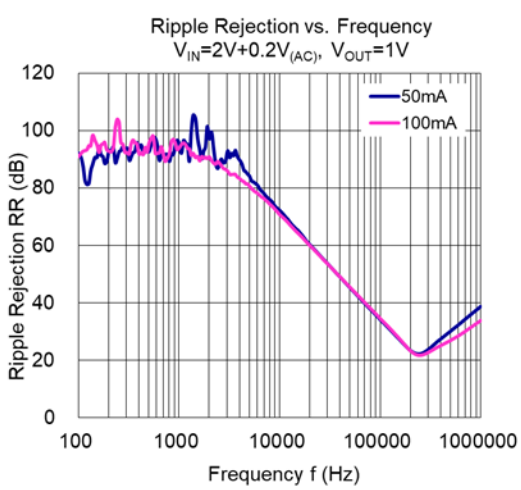
Typical Performance Characteristics (continued)

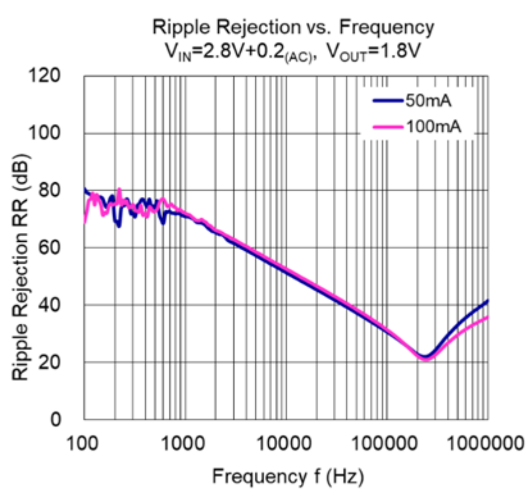




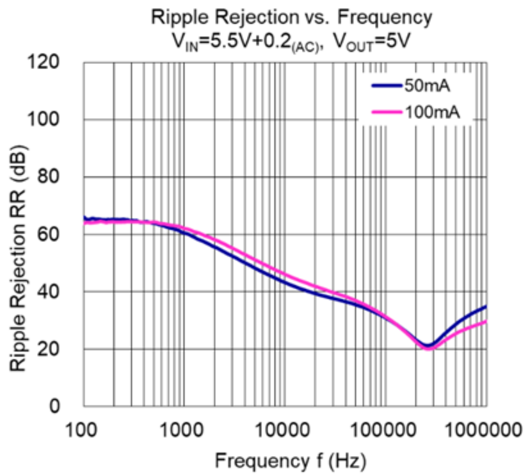


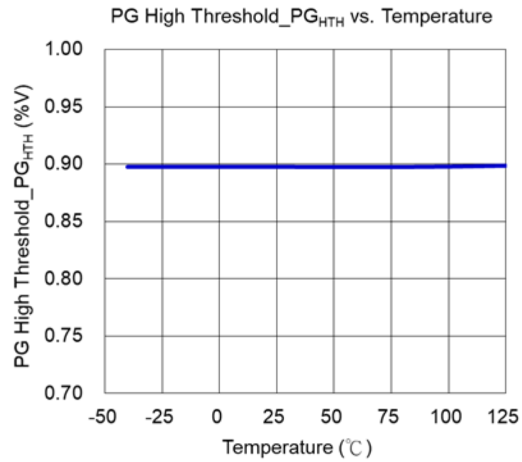


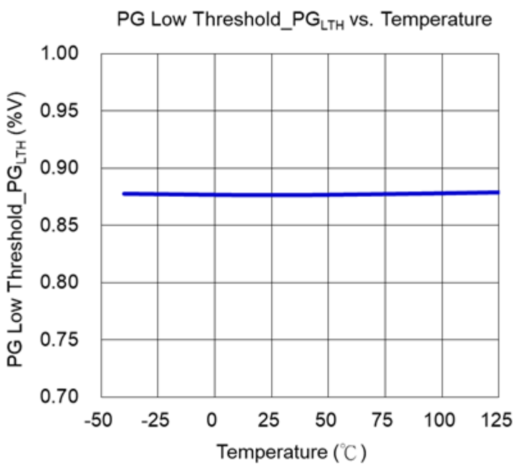


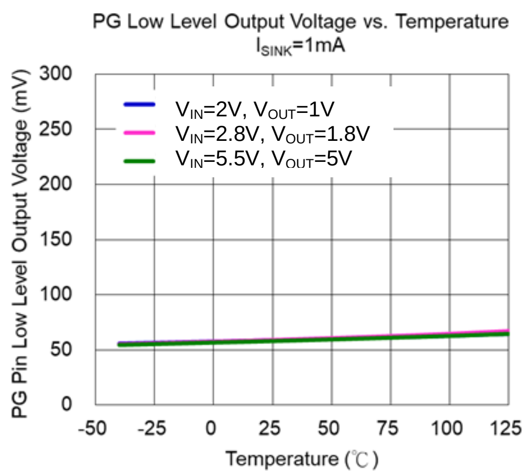


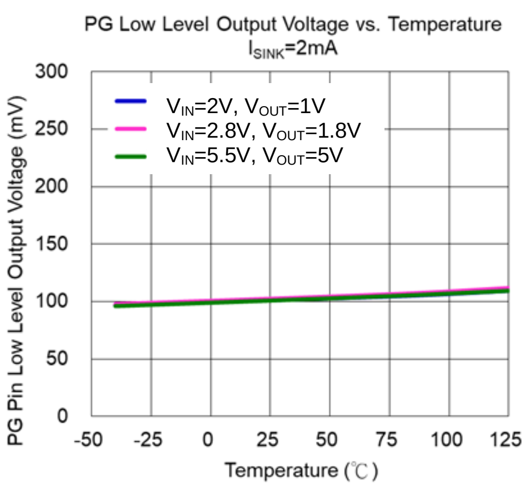
Typical Performance Characteristics (continued)

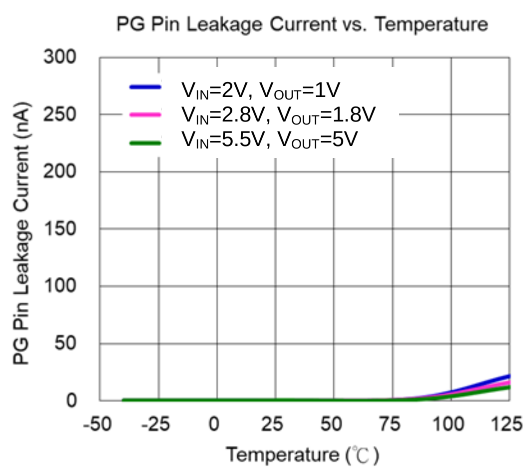




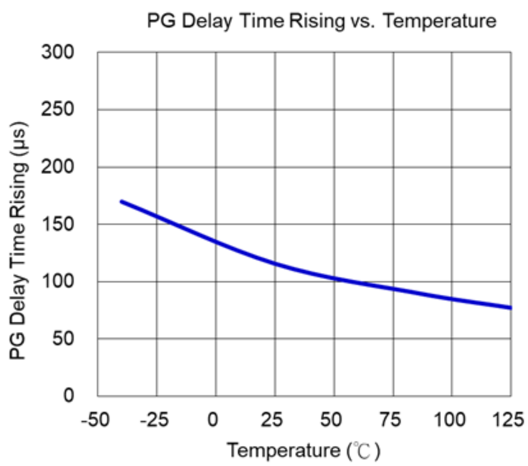


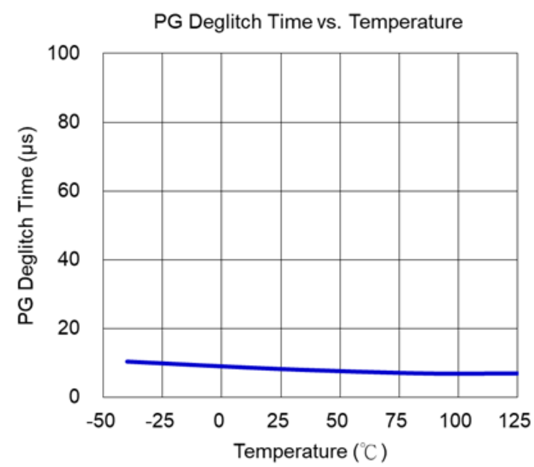




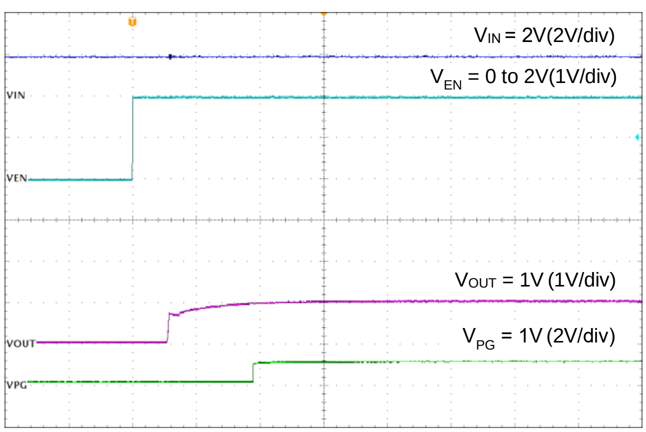


Typical Performance Characteristics (continued)



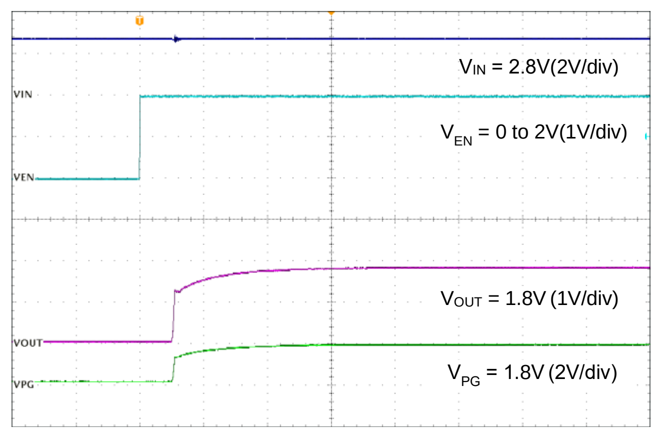


Enable Turn-On Response



Time (400µs/div)

Enable Turn-On Response



Time (400µs/div)

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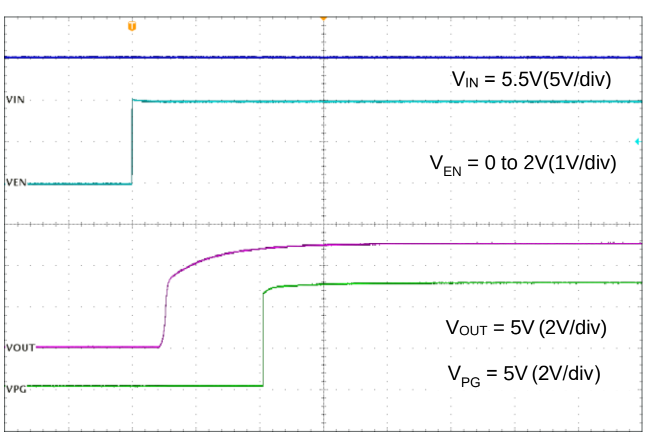
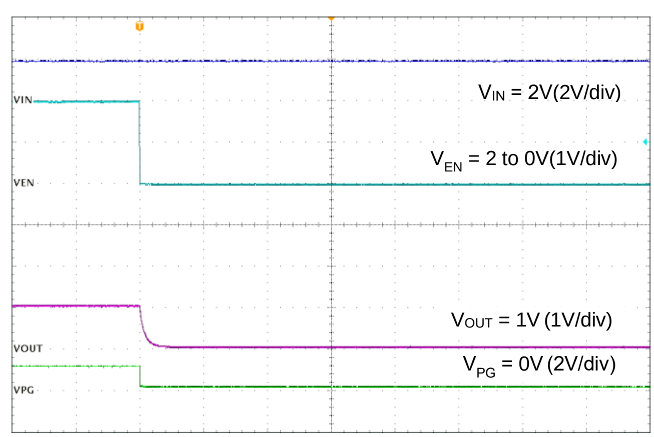


Time (400µs/div)

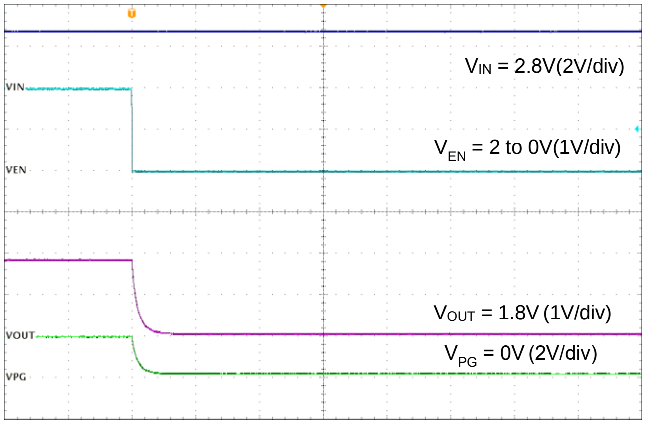
Enable Turn-Off Response



Time (400µs/div)

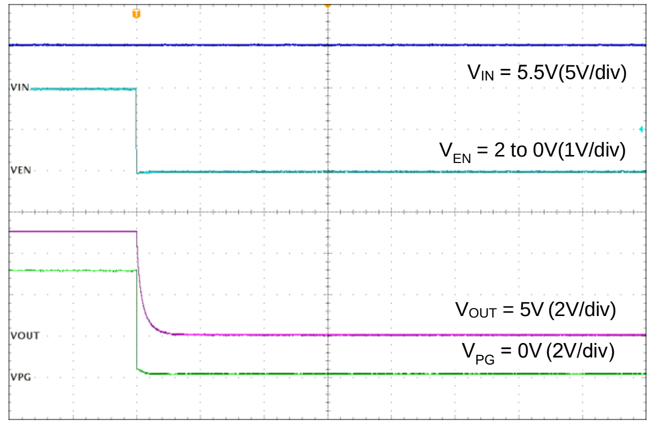
Typical Performance Characteristics (continued)

Enable Turn-Off Response



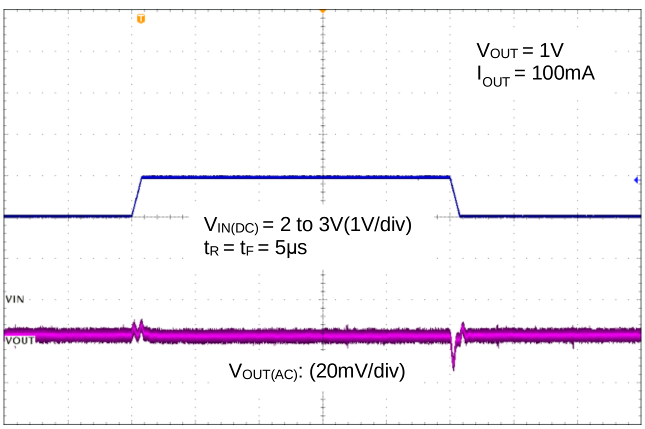
Time (400µs/div)

Enable Turn-Off Response



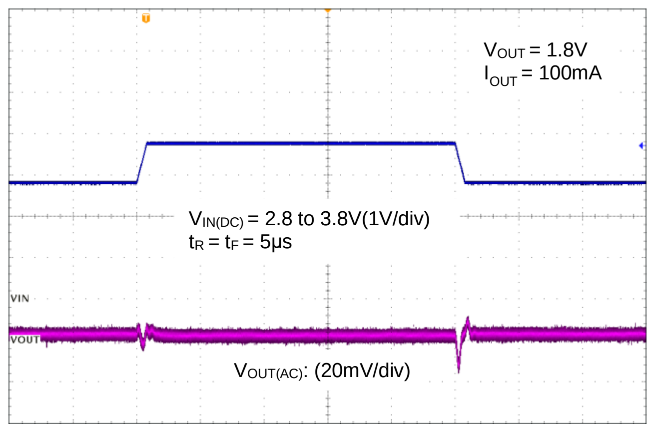
Time (400µs/div)

Line-Transient Response



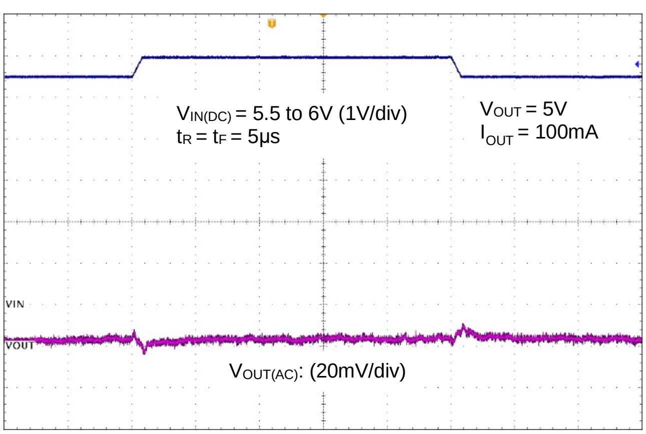
Time (40µs/div)

Line-Transient Response



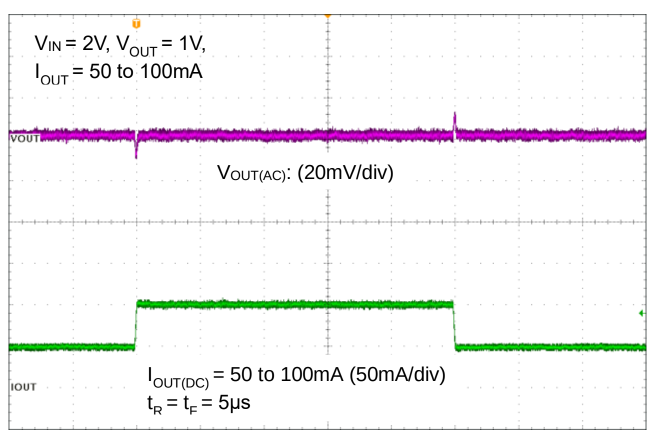
Time (40µs/div)

Line-Transient Response



Time (40µs/div)

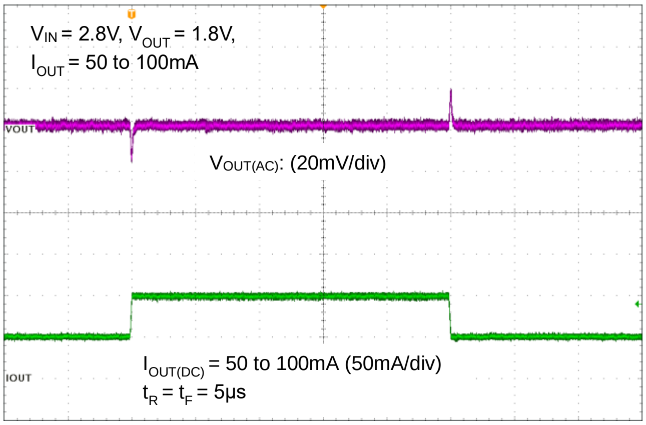
Load-Transient Response



Time (200µs/div)

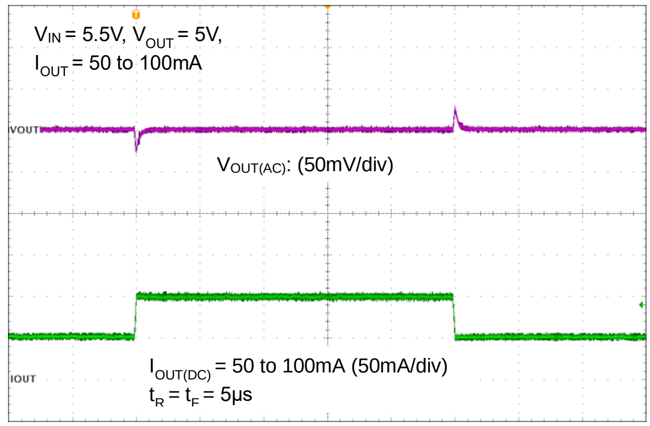
Typical Performance Characteristics (continued)

Load-Transient Response



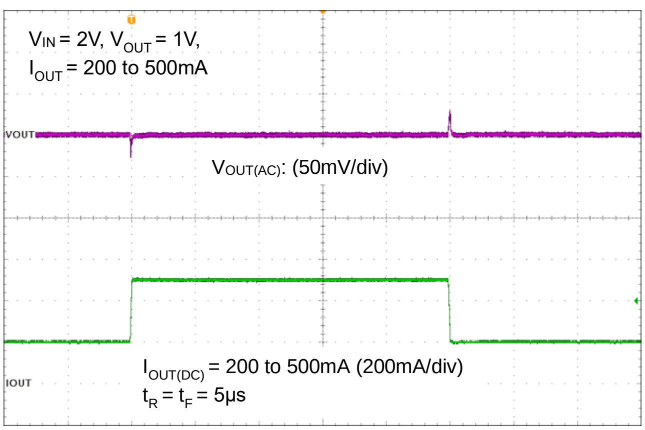
Time (200µs/div)

Load-Transient Response



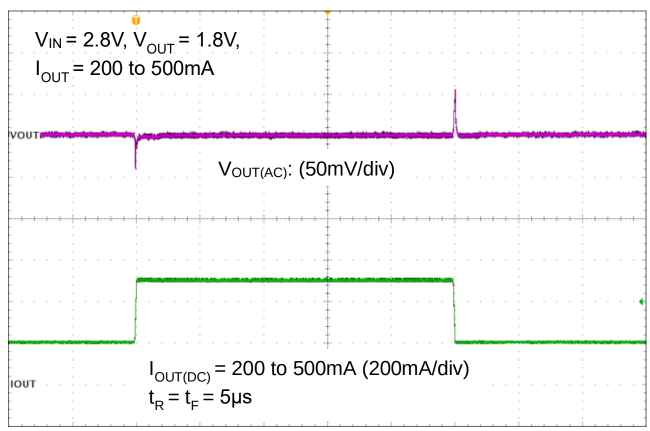
Time (200µs/div)

Load-Transient Response



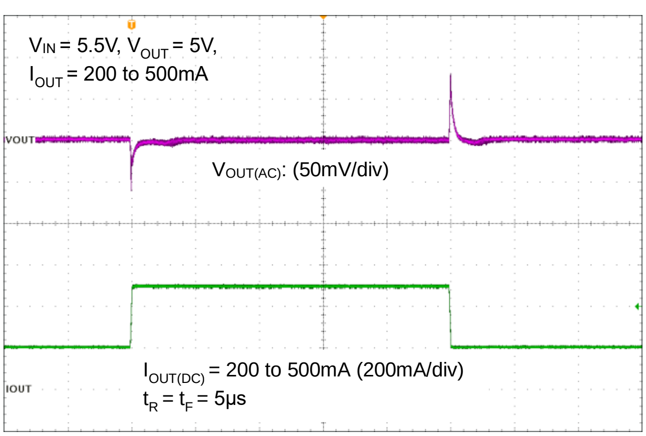
Time (200µs/div)

Load-Transient Response



Time (200µs/div)

Load-Transient Response



Time (200µs/div)

Application Information

Output Capacitor

An output capacitor (C_{OUT}) is needed to improve transient response and maintain stability. The AP7347EQ is stable with very small ceramic output capacitors. The ESR (equivalent series resistance) and capacitance drives the selection. If the application has large load variations, it is recommended to utilize low-ESR bulk capacitors. It is also recommended to place ceramic capacitors as close as possible to the load and the ground pin. Care should be taken to reduce the impedance in the layout.

Input Capacitor

To prevent the input voltage from dropping during load steps, it is recommended to utilize an input capacitor (C_{IN}). A minimum 1µF ceramic capacitor is recommended between the VIN and GND pins to decouple input power supply glitch. This input capacitor must be located as close as possible to the device to assure input stability and reduce noise. For PCB layout, a wide copper trace is required for both V_{IN} and GND pins.

Short-Circuit Protection

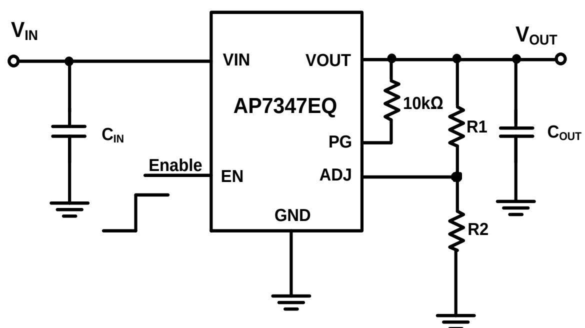
When the V_{OUT} pin short-circuits to GND, short-circuit protection will be triggered and clamp the output current to approximately 180mA. This feature protects the regulator from overcurrent and damage due to overheating.

Layout Considerations

For good ground loop and stability, the input and output capacitors should be located close to the input, output, and ground pins of the device. The regulator ground pin should be connected to the external circuit ground to reduce voltage drop caused by trace impedance. Ground plane is generally used to reduce trace impedance. Wide trace should be used for large current paths from V_{IN} to V_{OUT}, and load circuit.

Adjustable Operation

The AP7347EQ provides output voltage from 1V to 5V through external resistor divider as shown below:



AP7347EQ Adjustable Version

The output voltage is calculated by:

$$V_{OUT} = \left(1 + \frac{R_1}{R_2}\right)$$

Where V_{REF} = 0.8V (the internal reference voltage).
Rearranging the equation will give the following that is used for adjusting the output to a particular voltage:

$$R_1 = R_2\left(\frac{V_{OUT}}{V_{REF}} - 1\right)$$

To maintain the stability of the internal reference voltage, R2 needs to be kept smaller than 80kΩ.

ON/OFF Input Operation

The AP747EQ is turned on by setting the EN pin high, and is turned off by pulling it low. If this feature is not used, the EN pin should be tied to IN pin to keep the regulator output on at all time. To ensure proper operation, the signal source used to drive the EN pin must be able to swing above and below the specified turn-on/off voltage thresholds listed in the *Electrical Characteristics* section under V_{IL} and V_{IH}.

Current-Limit Protection

When output current at OUT pin is higher than current-limit threshold, the current-limit protection will be triggered and clamp the output current to prevent overcurrent and to protect the regulator from damage due to overheating.

Application Information (continued)

Power-Good

The power-good (PG) pin is an open-drain output. When the $V_{OUT} \geq PG_{HTH}$, the PG output is high-impedance; if the V_{OUT} drops below PG_{LTH}, or the device is disabled, the PG pin is pulled low by an internal MOSFET.

Thermal Shutdown Protection

Thermal protection disables the output when the junction temperature rises to approximately +170°C, allowing the device to cool down. When the junction temperature reduces to approximately +150°C, the output circuitry is enabled again. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This cycling limits the heat dissipation of the regulator, protecting it from damage due to overheating.

Power Dissipation

The device power dissipation and proper sizing of the thermal plane that is connected to the thermal pad is critical to avoid thermal shutdown and ensure reliable operation. Power dissipation of the device depends on input voltage and load conditions and can be calculated by:

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT}$$

The maximum power dissipation, handled by the device, depends on the maximum junction to ambient thermal resistance, maximum ambient temperature, and maximum device junction temperature, which can be calculated by the equation in the following:

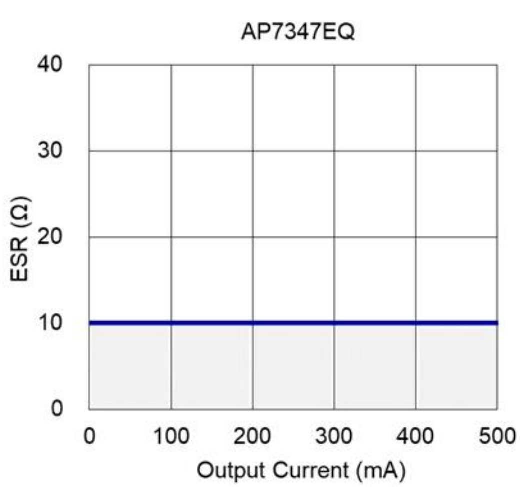
$$P_D(max@T_A) = \frac{(+150℃ - T_A)}{R_{\theta JA}}$$

ESR vs. Output Current

Ceramic type output capacitor is recommended for this series; however, the other output capacitors with low ESR also can be used. One 1μF output capacitor is suggested, the AP7347EQ series LDO would have stable output capacitance range from 4.7μF to 100μF. The relations between I_{OUT} (output current) and ESR of an output capacitor are shown below. The stable region for the safety operating temperature (-40°C to +125°C) is marked as the gray area in the graph.

Measurement conditions: Frequency Band: 10Hz to 2MHz, Temperature: -40°C to +125°C.

ESR vs. Output Current



Ordering Information

AP7347EQ - XXX XXXXX - XX

Output Voltage

Blank : ADJ
10 : 1.0V
105 : 1.05V
11 : 1.1V
115 : 1.15V
12 : 1.2V
15 : 1.5V
17 : 1.7V
18 : 1.8V
22 : 2.2V
25 : 2.5V
28 : 2.8V
29 : 2.9V
30 : 3.0V
33 : 3.3V
50 : 5.0V

Package

FDCW: U-DFN2020-6 (SWP) (Type UXC)
FDCWR: U-DFN2020-6 (SWP) (Type UXC)
FGECW: V-DFN3030-8/SWP (Type UX)

Packing

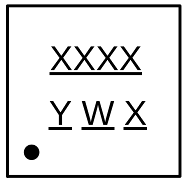
7R/13A: 7"/13" Tape & Reel

Orderable Part Number	Package Code	Package	Packing	
			Qty.	Carrier
AP7347EQ-FDCW-7R	FDCW	U-DFN2020-6 (SWP) (Type UXC)	3000	7" Tape & Reel
AP7347EQ-XXXFDCW-7R	FDCW	U-DFN2020-6 (SWP) (Type UXC)	3000	7" Tape & Reel
AP7347EQ-XXXFDCWR-7R	FDCWR	U-DFN2020-6 (SWP) (Type UXC)	3000	7" Tape & Reel
AP7347EQ-FGECW-13A	FGECW	V-DFN3030-8/SWP (Type UX)	3000	13" Tape & Reel
AP7347EQ-XXXFGECW-13A	FGECW	V-DFN3030-8/SWP (Type UX)	3000	13" Tape & Reel

Marking Information

(1) U-DFN2020-6 (SWP) (Type UXC)

(Top View)



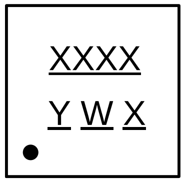
XXXX : Identification Code
Y : Year : 0~9
W : Week : A~Z : 1~26 week;
a~z : 27~52 week; z represents
52 and 53 week
X : Internal Code

Orderable Part Number	Package	Identification Code
AP7347EQ-FDCW-7R	U-DFN2020-6 (SWP) (Type UXC)	E2AQ
AP7347EQ-10FDCW-7R	U-DFN2020-6 (SWP) (Type UXC)	E2BQ
AP7347EQ-105FDCW-7R	U-DFN2020-6 (SWP) (Type UXC)	E2CQ
AP7347EQ-11FDCW-7R	U-DFN2020-6 (SWP) (Type UXC)	E2DQ
AP7347EQ-115FDCW-7R	U-DFN2020-6 (SWP) (Type UXC)	E2EQ
AP7347EQ-12FDCW-7R	U-DFN2020-6 (SWP) (Type UXC)	E2FQ
AP7347EQ-15FDCW-7R	U-DFN2020-6 (SWP) (Type UXC)	E2GQ
AP7347EQ-17FDCW-7R	U-DFN2020-6 (SWP) (Type UXC)	E2HQ
AP7347EQ-18FDCW-7R	U-DFN2020-6 (SWP) (Type UXC)	E2JQ
AP7347EQ-22FDCW-7R	U-DFN2020-6 (SWP) (Type UXC)	E2KQ
AP7347EQ-25FDCW-7R	U-DFN2020-6 (SWP) (Type UXC)	E2MQ
AP7347EQ-28FDCW-7R	U-DFN2020-6 (SWP) (Type UXC)	E2NQ
AP7347EQ-29FDCW-7R	U-DFN2020-6 (SWP) (Type UXC)	E2PQ
AP7347EQ-30FDCW-7R	U-DFN2020-6 (SWP) (Type UXC)	E2RQ
AP7347EQ-33FDCW-7R	U-DFN2020-6 (SWP) (Type UXC)	E2SQ
AP7347EQ-50FDCW-7R	U-DFN2020-6 (SWP) (Type UXC)	E2TQ
AP7347EQ-10FDCWR-7R	U-DFN2020-6 (SWP) (Type UXC)	E3BQ
AP7347EQ-105FDCWR-7R	U-DFN2020-6 (SWP) (Type UXC)	E3CQ
AP7347EQ-11FDCWR-7R	U-DFN2020-6 (SWP) (Type UXC)	E3DQ
AP7347EQ-115FDCWR-7R	U-DFN2020-6 (SWP) (Type UXC)	E3EQ
AP7347EQ-12FDCWR-7R	U-DFN2020-6 (SWP) (Type UXC)	E3FQ
AP7347EQ-15FDCWR-7R	U-DFN2020-6 (SWP) (Type UXC)	E3GQ
AP7347EQ-17FDCWR-7R	U-DFN2020-6 (SWP) (Type UXC)	E3HQ
AP7347EQ-18FDCWR-7R	U-DFN2020-6 (SWP) (Type UXC)	E3JQ
AP7347EQ-22FDCWR-7R	U-DFN2020-6 (SWP) (Type UXC)	E3KQ
AP7347EQ-25FDCWR-7R	U-DFN2020-6 (SWP) (Type UXC)	E3MQ
AP7347EQ-28FDCWR-7R	U-DFN2020-6 (SWP) (Type UXC)	E3NQ
AP7347EQ-29FDCWR-7R	U-DFN2020-6 (SWP) (Type UXC)	E3PQ
AP7347EQ-30FDCWR-7R	U-DFN2020-6 (SWP) (Type UXC)	E3RQ
AP7347EQ-33FDCWR-7R	U-DFN2020-6 (SWP) (Type UXC)	E3SQ
AP7347EQ-50FDCWR-7R	U-DFN2020-6 (SWP) (Type UXC)	E3TQ

Marking Information (continued)

(2) V-DFN3030-8/SWP (Type UX)

(Top View)



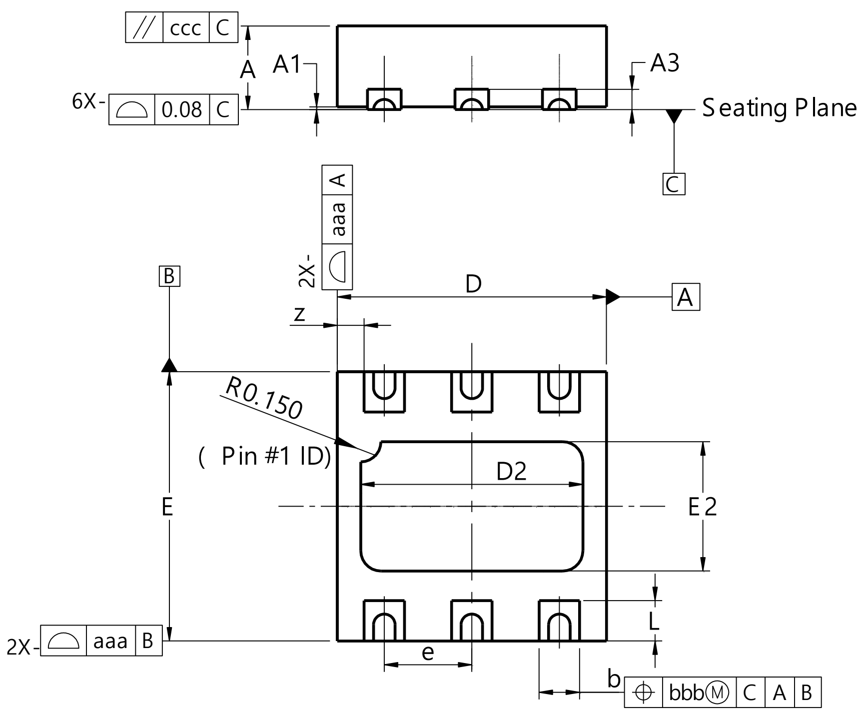
XXXX : Identification Code
Y : Year : 0~9
W : Week : A~Z : 1~26 week;
a~z : 27~52 week; z represents
52 and 53 week
X : Internal Code

Orderable Part Number	Package	Identification Code
AP7347EQ-FGECW-13A	V-DFN3030-8/SWP (Type UX)	E4AQ
AP7347EQ-10FGECW-13A	V-DFN3030-8/SWP (Type UX)	E4BQ
AP7347EQ-105FGECW-13A	V-DFN3030-8/SWP (Type UX)	E4CQ
AP7347EQ-11FGECW-13A	V-DFN3030-8/SWP (Type UX)	E4DQ
AP7347EQ-115FGECW-13A	V-DFN3030-8/SWP (Type UX)	E4EQ
AP7347EQ-12FGECW-13A	V-DFN3030-8/SWP (Type UX)	E4FQ
AP7347EQ-15FGECW-13A	V-DFN3030-8/SWP (Type UX)	E4GQ
AP7347EQ-17FGECW-13A	V-DFN3030-8/SWP (Type UX)	E4HQ
AP7347EQ-18FGECW-13A	V-DFN3030-8/SWP (Type UX)	E4JQ
AP7347EQ-22FGECW-13A	V-DFN3030-8/SWP (Type UX)	E4KQ
AP7347EQ-25FGECW-13A	V-DFN3030-8/SWP (Type UX)	E4MQ
AP7347EQ-28FGECW-13A	V-DFN3030-8/SWP (Type UX)	E4NQ
AP7347EQ-29FGECW-13A	V-DFN3030-8/SWP (Type UX)	E4PQ
AP7347EQ-30FGECW-13A	V-DFN3030-8/SWP (Type UX)	E4RQ
AP7347EQ-33FGECW-13A	V-DFN3030-8/SWP (Type UX)	E4SQ
AP7347EQ-50FGECW-13A	V-DFN3030-8/SWP (Type UX)	E4TQ

Package Outline Dimensions

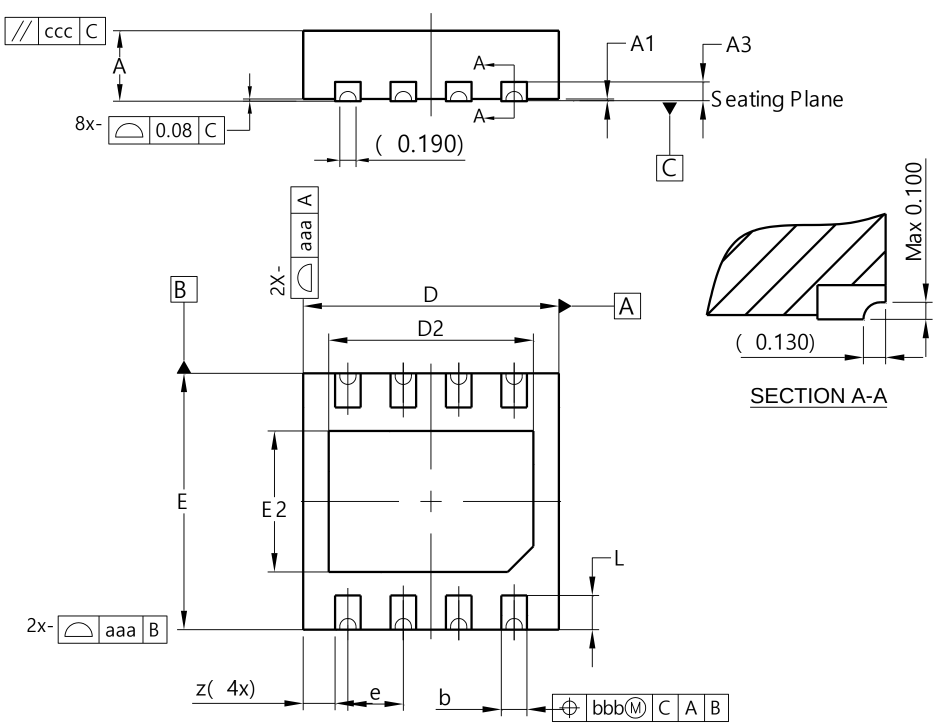
Please see http://www.diodes.com/package-outlines.html for the latest version.

(1) U-DFN2020-6 (SWP) (Type UXC)



U-DFN2020-6 (SWP) (Type UXC)			
Dim	**Min**	**Max**	**Typ**
A	0.57	0.63	0.60
A1	0.00	0.05	0.02
A3	—	—	0.13
b	0.25	0.35	0.30
D	1.95	2.075	2.00
D2	1.55	1.75	1.65
E	1.95	2.075	2.00
E2	0.86	1.06	0.96
e	—	—	0.65
L	0.25	0.35	0.30
z	—	—	0.20
aaa	0.25		
bbb	0.10		
ccc	0.10		
All Dimensions in mm			

(2) V-DFN3030-8/SWP (Type UX)

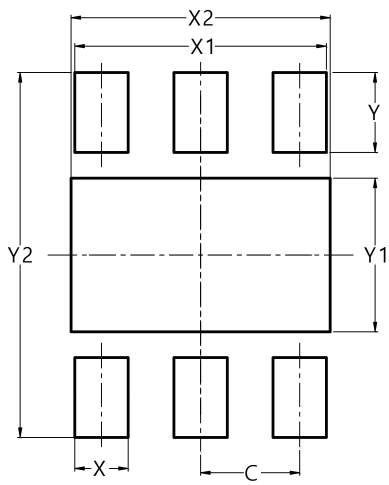


V-DFN3030-8/SWP (Type UX)			
Dim	**Min**	**Max**	**Typ**
A	0.75	0.85	0.80
A1	0.00	0.05	0.02
A3	--	--	0.20
b	0.25	0.35	0.30
D	2.90	3.10	3.00
D2	2.30	2.50	2.40
e	0.65 BSC		
E	2.90	3.10	3.00
E2	1.55	1.75	1.65
L	0.30	0.50	0.40
z	--	--	0.37
aaa	0.25		
bbb	0.10		
ccc	0.10		
All Dimensions in mm			

Suggested Pad Layout

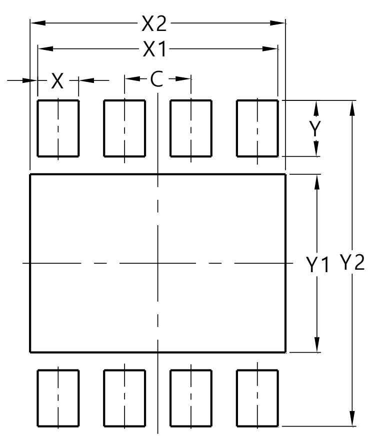
Please see http://www.diodes.com/package-outlines.html for the latest version.

(1) U-DFN2020-6 (SWP) (Type UXC)



Dimensions	Value (in mm)
C	0.650
X	0.350
X1	1.650
X2	1.700
Y	0.525
Y1	1.010
Y2	2.400

(2) V-DFN3030-8/SWP (Type UX)



Dimensions	Value (in mm)
C	0.650
X	0.400
X1	2.350
X2	2.500
Y	0.550
Y1	1.750
Y2	3.200

Mechanical Data

U-DFN2020-6 (SWP) (Type UXC)

- Moisture Sensitivity: Level 1 Per J-STD-020
- Terminals: Finish – NiPdAu over Copper Leads, Solderable per MIL-STD-202, Method 208 (e4)
- Weight: 0.007 grams (Approximate)

V-DFN3030-8/SWP (Type UX)

- Moisture Sensitivity: Level 1 Per J-STD-020
- Terminals: Finish – NiPdAu over Copper Leads, Solderable per MIL-STD-202, Method 208 (e4)
- Weight: 0.019 grams (Approximate)

IMPORTANT NOTICE

www.diodes.com