SAS DISABLE +5V eFUSE WITH INTEGRATED ISOFET

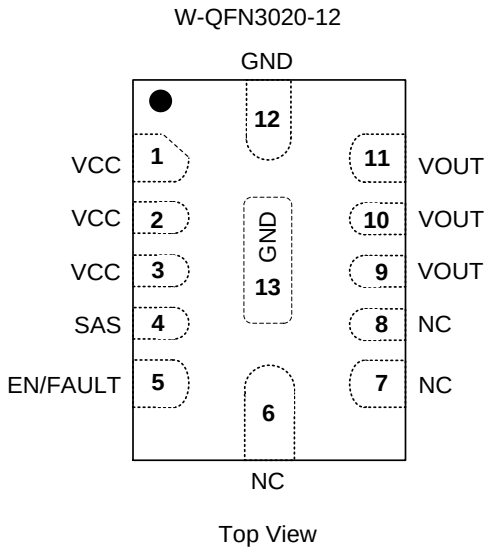
Description

The eFuse is a 5V protection device with a bidirectional switch that incorporates input slew rate control to reduce input surge current and reverse current detection to prevent discharge to VCC from VOUT. The eFuse protection features include undervoltage lockout, a fixed 2.5A current limit, trimmed fast response overvoltage protection and thermal shutdown. The EN/FAULT line is a tri-state bidirectional interface that can be used to disable the output by pulling the line low through an external open-drain device. If a thermal fault occurs, the voltage on the pin will go to an intermediate voltage indicating a fault and it can be connected to another device to cause simultaneous shutdown. The SAS pin is an ESD protected interface that allows direct external control of the eFuse. Driving the SAS pin high pulls the enable line low causing the eFuse to shut down and enter a low quiescent current state.

The integrated ISOFET latches off when the reverse current is detected. This can be reset only by triggering the undervoltage lockout, by EN/FAULT pin or when voltage on the output pin (V_{OUT}) falls below the supply pin voltage (V_{CC}) in the AP91350H.

The AP91350H is available in a standard Green W-QFN3020-12 package and is RoHS compliant.

Pin Assignments



Top View

Features

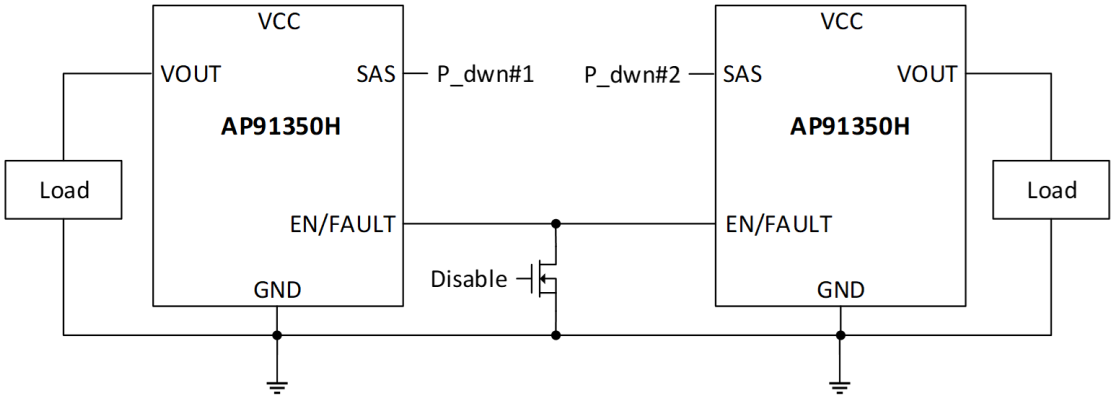
- SAS Disable
  - 2.1V Signal Disables the eFuse
  - ESD Compliant to 2kV HBM and 1kV CDM
- Integrated ISOFET That Latches Off When Reverse Current is Detected. Latch Off is Reset by
  - V_{OUT} Falling Below V_{CC}
  - UVLO Trigger
  - EN/FAULT Pin
- Input Tolerant of Continuous +12V
- 50mΩ Typical Total On-Resistance
- Fixed 2.5A Overcurrent Protection (OCP)
- Overvoltage Protection (OVP)
- Fixed 13ms +/- 20% Slew Rate Control (SRC)
- Overtemperature Protection (OTP)
- Undervoltage Lockout (UVLO)
- Thermally Efficient Low Profile Package, W-QFN3020-12
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**
- **For automotive applications requiring specific change control (i.e. parts qualified to AEC-Q100/101/104/200, PPAP capable, and manufactured in IATF 16949 certified facilities), please contact us or your local Diodes representative. https://www.diodes.com/quality/product-definitions/**

Applications

- HHD drives
- SSD drives
- Mother board power management
- Printer load power management
- Fan drives

Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

Typical Applications Circuit

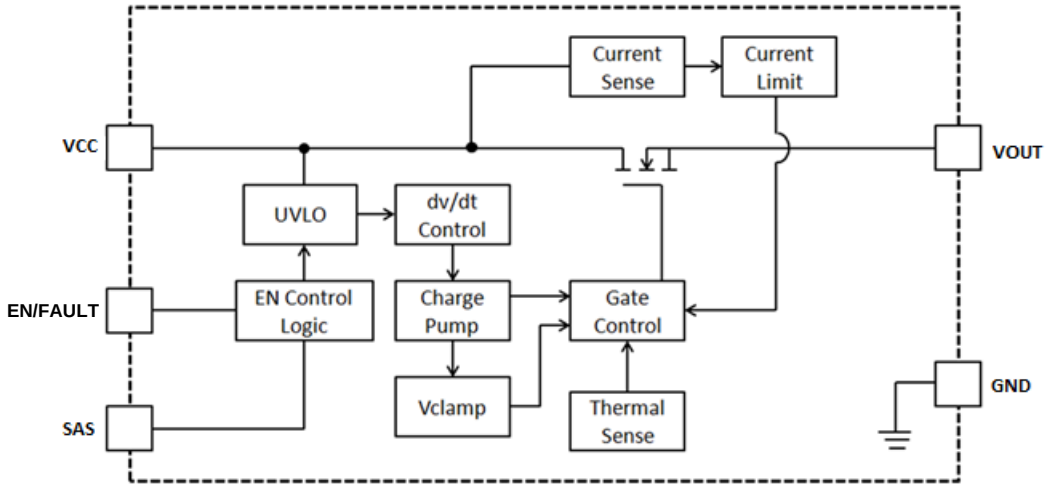


Pin Descriptions

Pin Number	Pin Name	Description
1, 2, 3	VCC	Supply input, a minimum 10µF (Note 4) capacitor is needed to supply internal charge pump. The capacitor return should be connected directly to the GND pin.
4	SAS	SAS disable. When this pin is pulled high to a voltage greater than 2.1V, the eFuse is turned off.
5	EN/FAULT	The EN/FAULT pin is a tri-state, bidirectional interface. It can be used to enable or disable the output of the device by pulling it to ground using an open-drain device. If a thermal fault occurs, the voltage on this pin will go to an intermediate state to signal a monitoring circuit that the device is in thermal shutdown. It can also be connected to another device in this family to cause a simultaneous shutdown during thermal events.
6, 7, 8	NC	Do not connect on PCB, internally connected for production purpose.
9, 10, 11	VOUT	Output: eFuse controlled output; a 20µF capacitor is needed for overvoltage protection stability. The capacitor return should be connected directly to the GND pin.
12	GND	Ground
13	GND	Ground exposed pad

Note: 4. Minimum input capacitance is 10µF. Please refer to the *Input Capacitor Selection* in *Application Note* section.

Functional Block Diagram



Absolute Maximum Ratings (Note 5) (@ T_A = +25°C, unless otherwise specified.)

Symbol	Parameter		Ratings	Unit
VCC	Input Voltage	Steady State	-0.3 to 16	V
		Transient (100ms)	-0.3 to 21	
EN/FAULT	Enable Voltage		-0.3 to 6	V
SAS	SAS Disable Voltage		-0.3 to 3.6	V
VOUT	VOUT Voltage		-0.3 to 7.0	V
ESD HBM	Human Body ESD Protection JESD22-A114		2000	V
ESD CDM	Charged Device Model ESD Protection JESD22-C101		1000	V
$T_{J(Max)}$	Maximum Junction Temperature		+150	°C
T_{ST}	Storage Temperature		-65 to +150	°C
P_D	Power Dissipation (T_A = +25°C)	W-QFN3020-12	1.3	W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (0.5 square inch)	W-QFN3020-12 (Note 6)	40	°C/W

Notes:
5. Stresses greater than those listed under *Absolute Maximum Ratings* can cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to *Absolute Maximum Ratings* for extended periods can affect device reliability.
6. For a device surface mounted on 25mm by 25mm by 1.6mm FR-4 PCB with high coverage of single sided 2oz copper, in still air conditions; the device is measured when operating in a steady state condition.

Recommended Operating Conditions (All specifications are for -10°C < T_A < +85°C, V_{CC} = 5V, unless otherwise noted.)

Symbol	Parameter	Min	Typ	Max	Unit
VCC	Input Voltage Range	3.6	—	12	V
T_A	Operating Ambient Temperature	-40	—	+85	°C

Electrical Characteristics (Note 7) (All specifications are for -10°C < T_A < +85°C, V_{CC} = 5V, unless otherwise noted.)

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
Supply Current						
I_Q	VCC Supply Current	EN = High, SAS = 0, I_{LOAD} = 0A	—	—	300	μA
		Fault Latch off	—	100	—	μA
		EN = Low	—	—	100	μA
Power FET						
$R_{DS(ON)}$	On-Resistance	T_A = +25°C	—	50	65	mΩ
		T_J = +80°C	—	95	—	mΩ
t_{ON-DLY}	Turn-On Delay	Enable I_D = 100mA, 1A Resistive Load	—	500	—	μs
I_{DC}	Continuous Current	T_A = +25°C, 0.5 Square inch Copper	—	2	—	A
I_{OFF}	Off-State Leakage	V_{CC} = 12V, EN = Low	—	—	1	μA
Slew Rate Control						
SRC	Slew Rate Control	EN to V_{OUT} = 4.7V (Note 8)	10.4	13.0	15.6	ms
Current Protection						
I_{LIM}	Current Limit	—	2.5	3.0	—	A
I_{SHORT}	Short-Circuit Current	—	—	3.0	—	A
t_{ILIM}	Current Limit Response	—	5.5	—	40	μs
Reverse Current Limit/Undervoltage Protection						
$I_{QREVERSE}$	Fast Reverse Current Limit	(Note 9)	0.9	—	1.7	A
$t_{QREVERSE}$	Fast Reverse Current Limit Response Time	V_{CC} dv/dt = -5V/1ms	5	—	10	μs
UVLO	Undervoltage Lockout	UVLO Rising	3.8	4.0	4.2	V
UVLO-hys	Undervoltage Hysteresis	—	—	0.3	—	V
—	Undervoltage Response	—	—	2.0	—	μs
Overvoltage Protection						
OVP	Overvoltage Clamping	—	5.5	6	6.25	V
t_{OVP}	Overvoltage Response	C_{OUT} = 20μF, dv/dt (V_{CC}) = 0.5V/μs V_{OUT} < 6.5V	—	20	40	μs
Thermal Protection						
TH_{SD}	Shutdown Temperature	—	+130	+150	+200	°C
Enable/Fault						
V_L	Logic Level Low	Output Disabled (Note 8)	0.35	—	0.8	V
V_M	Logic Level Mid	Thermal Fault, Output Disabled (Note 8)	0.9	—	1.95	V
V_H	Logic Level High	Output Enabled	2.1	—	3.3	V
V_{MAX}	Maximum High State	—	3.4	—	5.2	V
I_L	Logic Low Sink Current	EN = 0V	—	-12	-20	μA
I_H	Logic Level High	EN = 3.3V	—	—	1	μA
FAN	Fan Out	—	—	—	3	Units

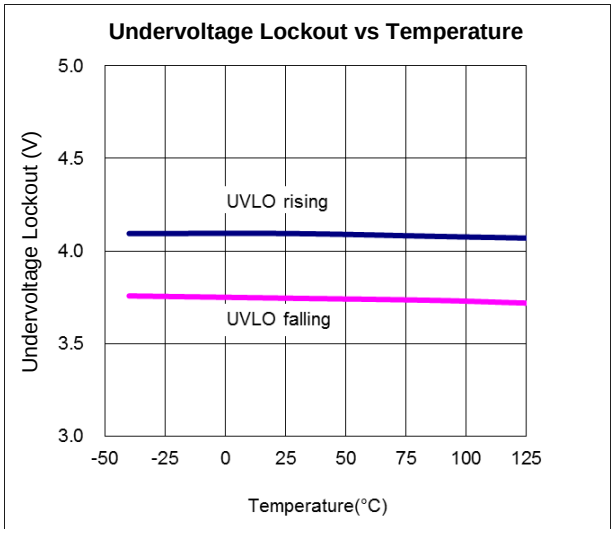
Notes:
7. Typical data is measured at T_A = +25°C, V_{CC} = 5V. The maximum and minimum parameters values over operating temperature range are not tested in production, they are guaranteed by design, characterization and process control.
8. The slew rate control is held in reset until the input voltage is greater than the UVLO rising threshold and Enable = High. The slew rate control is reset when input voltage drops below UVLO falling threshold, Enable changes from High to Mid or Low, SA = High or reverse current detection.
9. Reverse current detection will latch off the ISOFET switch; In AP91350H, this condition can be reset by undervoltage lockout, by EN/FAULT and SAS pins, or when V_{OUT} falls below the supply pin voltage (V_{CC}) by 100mV typical at T_A = +25°C, V_{CC} = 5V.

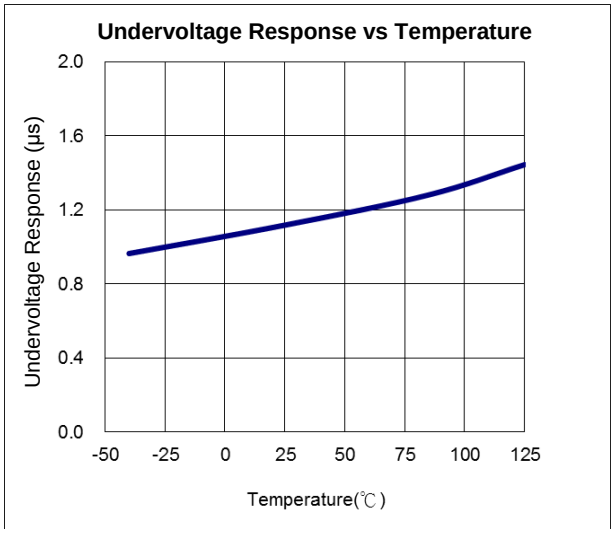
Electrical Characteristics (continued) (Note 7) (All specifications are for -10°C < T_A < +85°C, V_{CC} = 5V, unless otherwise noted.)

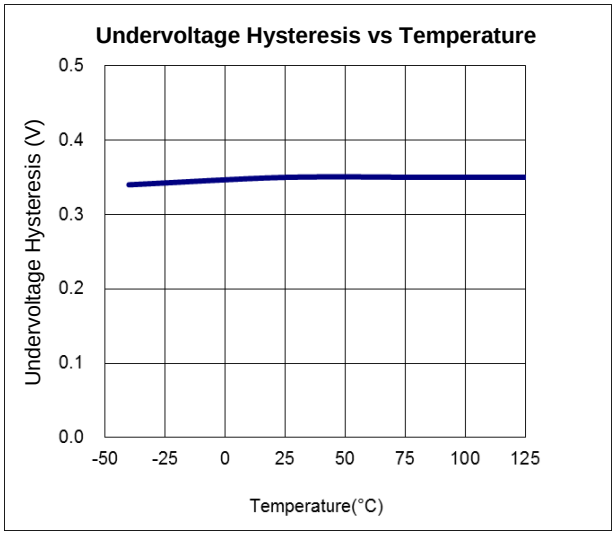
Symbol	Parameters	Conditions	Min	Typ	Max	Unit
SAS Disable						
SAS_L	Logic Level Low	Output Enabled	0.35	—	1.05	V
SAS_H	Logic Level High	Output Disabled	1.15	1.4	2.1	V
SAS_{Hmax}	Maximum Pin Voltage	—	—	—	3.3	V
$SAS\text{-}\Omega_{IN}$	Input Impedance	To GND	350	500	1000	kΩ
$SAS\text{-}T_{DLY}$	Deglitch Filter	—	2	—	50	µs
—	Human Body JESD22-A114	—	1	—	—	kV
—	Charged Device JESD22-C101	—	500	—	—	V

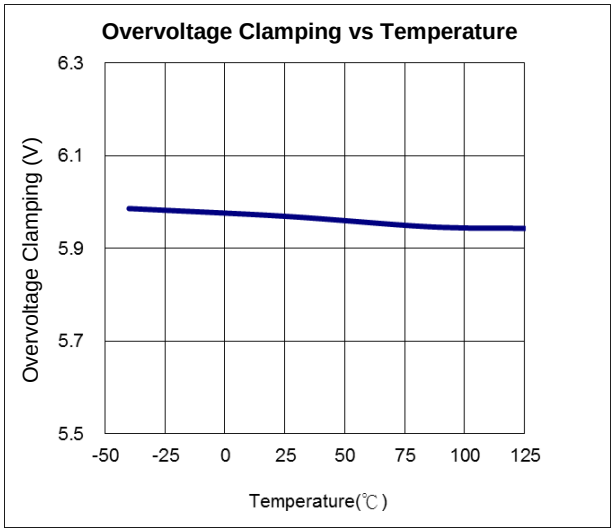
Note: 7. Typical data is measured at T_A = +25°C, V_{CC} = 5V. The maximum and minimum parameters values over operating temperature range are not tested in production, they are guaranteed by design, characterization and process control.

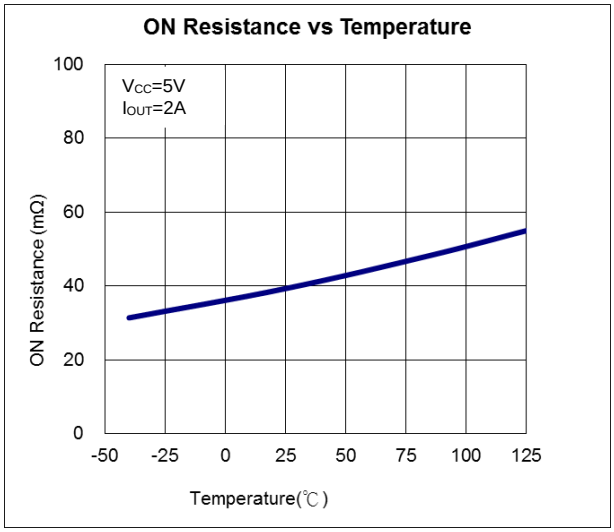
Performance Characteristic

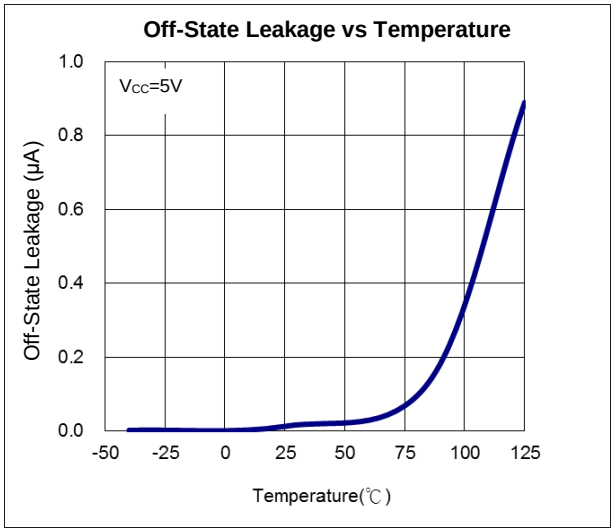




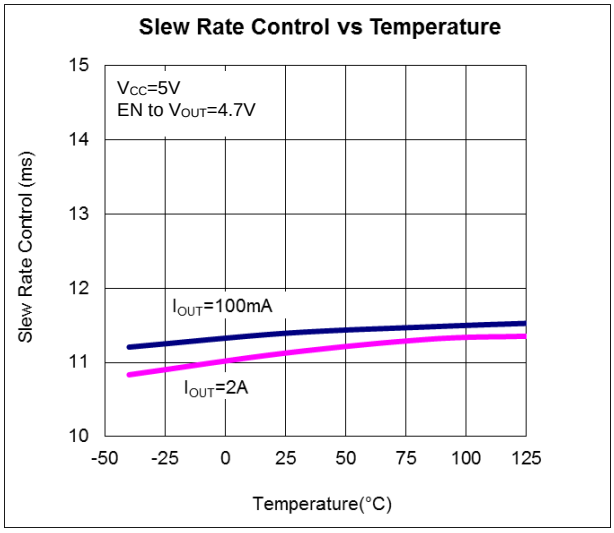


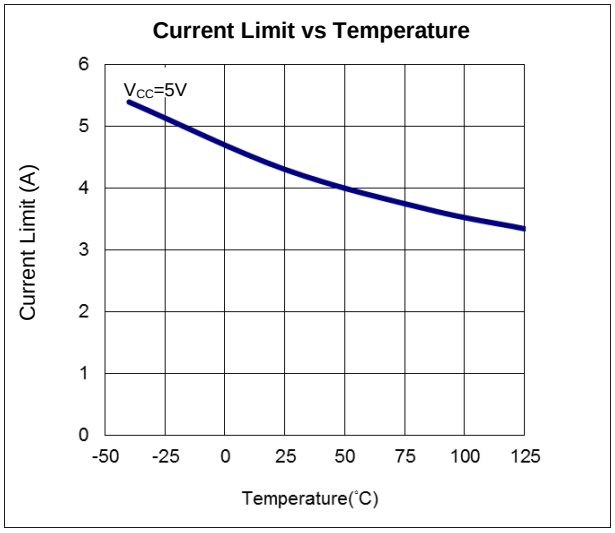


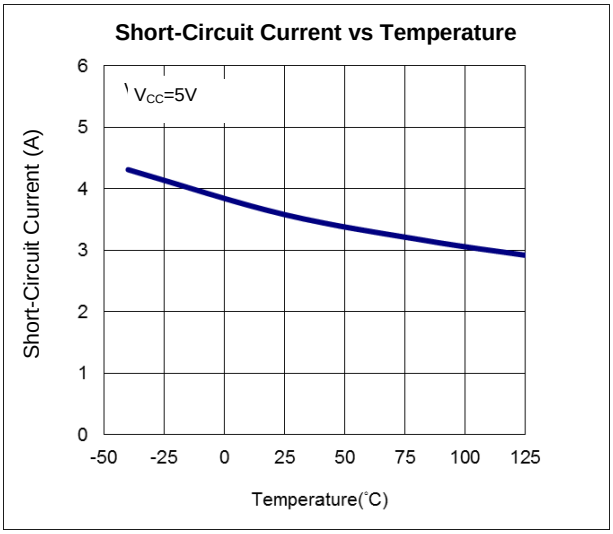


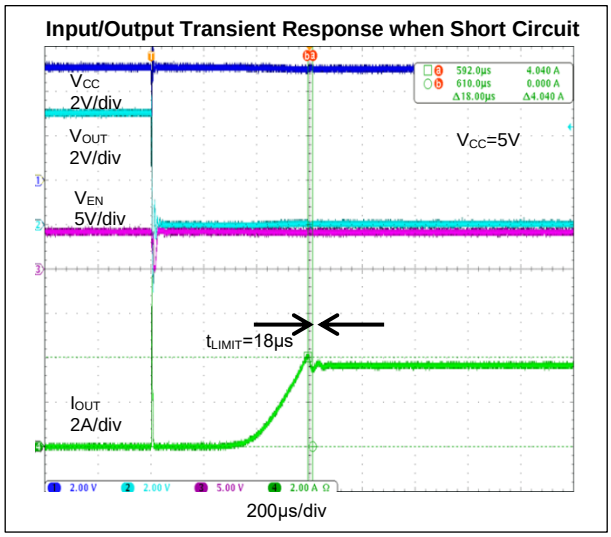


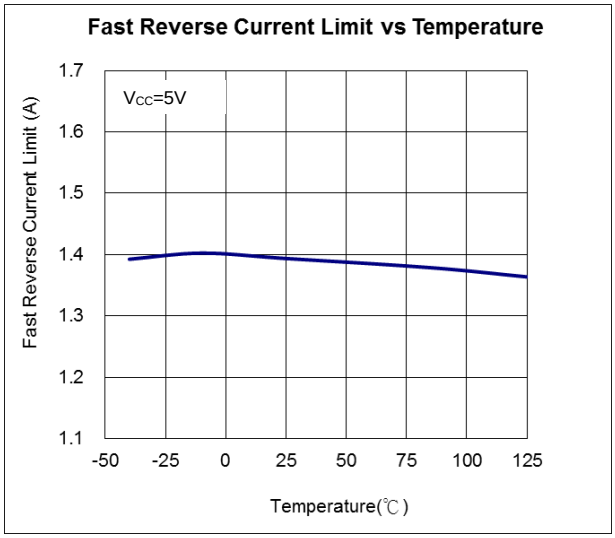
Performance Characteristic (continued)

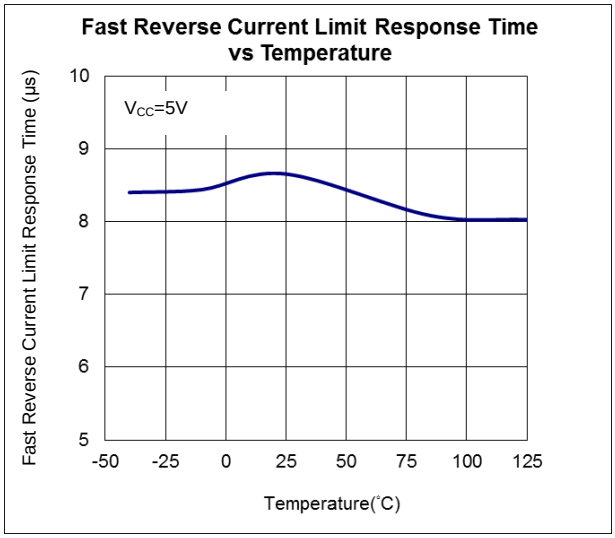












Application Note

Theory of Operation

The AP91350H is a self-protected, resettable electronic fuse. It monitors the input and output voltage, the output current and the die temperature. When the AP91350H is powered up, it will ramp up the output voltage based on the fixed slew rate (see *Electrical Characteristics* above) and current will begin to flow. The Overcurrent Protection, Overvoltage Clamp, Undervoltage Lockout and Thermal Protection are internally set.

Also, integrated reverse blocking MOSFET would prevent back-drive from an active load inadvertently causing undetermined behavior in the application.

Overvoltage Clamping

The AP91350H monitors the input voltage and clamp output voltage once it exceeds 6.25V (max). This will allow for transient on the input for a short period of time. If the input voltage stays above 6.25V (max) for an extended period of time, the voltage drop across the FET with the load current will increase the die temperature and the thermal shutdown feature will protect the device and shut it down.

Undervoltage Lockout

The input voltage of AP91350H is monitored by a UVLO circuit (undervoltage lockout). If the input voltage drops below this threshold, the output transistor will be pulled into a high impedance state.

Input Capacitor Selection

The AP91350H is designed to feature multiple fault protections to protect application circuit and device itself. VCC input may have voltage transient upon immediate switch-off behavior by fault events like SCP (Short-Circuit Protection) and OTP (Overtemperature Protection), if excessive voltage transient on VCC is observed, increase capacitance on VCC up to 10µF is recommended.

Enable/Fault

The AP91350H has a tri-state EN/FAULT pin. It is used to turn on and off the device with high and low signals from a GPIO, but can also indicate a thermal fault. When the EN/FAULT pin is pulled low, the output is turned off; when the EN/FAULT pin is pulled high, the output is turned on. Also, the EN/FAULT pin would be internally pulled high after V_{CC} reaches UVLO. In the event of a thermal fault, the EN/FAULT pin will be pulled low to an intermediate voltage by an internal circuit. This can be used to chain up to 3 eFuses together, like AP91350H, NIS5132 (12V eFuse), or NIS5135 (5V eFuse), so during a thermal shutdown, the linked devices turn off as well.

Due to this fault indication capability, it should not be connected to any type of logic with an internal pullup device.

The AP91350H connected to a 2nd device will latch off until the EN/FAULT pin has been pulled to low and then allowed to go back up to a high signal, or SAS pin has been toggled from High to Low or if the power has been cycled. Once the part starts up again, it will go through the start-up ramp determined by the internal circuit, 13ms (typ).

Table 1. EN/FAULT Signal Levels & Device Status

Symbol	Description	Enable/Fault	eFuse State	Latching
UVLO	Under Voltage Lock Out	V_L	Off	No
SAS_H	SAS Disable = 1	V_L	Off	N/A
TH_{SD}	Thermal Shutdown	V_M	Off	Yes
$I_{REVERSE}$	Reverse Current Protection	V_M	Off	(Note 9)
SAS_O	SAS Disable = Open	V_H	On	N/A
SAS_L	SAS Disable = 0	V_H	On	N/A
—	V_{CC} > UVLO, No Fault	V_H	On	N/A

Note: 9. Reverse current detection will latch off the ISOFET switch; In AP91350H, this condition can be reset by undervoltage lockout, by EN/FAULT and SAS pins, or when V_{OUT} falls below the supply pin voltage (V_{CC}) by 100mV typical at T_A = +25°C, V_{CC} = 5V.

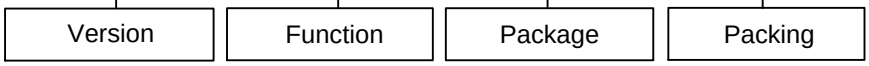
Thermal Protection

The AP91350H has an integrated temperature sensing circuit that protects the die in the event of overtemperature. The trip point has been intentionally set high at +150˚C (typ) to allow for increased trip times during high power transient events. The AP91350H will shut down current flow to the output when the die temperature reaches +150°C (typ). The AP91350H will restart after the Enable pin has been toggled or the input power has been cycled.

Even though the thermal trip point has been set high to allow for high current transients, the circuit design should accomplish best thermal performance with good thermal layout of the PCB. It is not recommended to operate AP91350H above +150°C over extended period of time.

Ordering Information

AP91350H XX X - XXX - XX



MN : Product Version

1: Thermal or Reverse Current Latching (Note 9)

DT8 : W-QFN3020-12

7R : Tape & Reel

Part Number	Part Number Suffix	Package Code	Package (Note 10)	Packing	
				Qty.	Carrier
AP91350HMN1-DT8-7R	-7R	DT8	W-QFN3020-12	3000	Tape & Reel

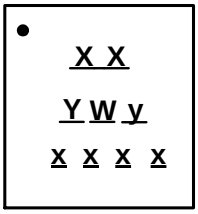
Notes: 9. Reverse current detection will latch off the ISOFET switch; In AP91350H, this condition can be reset by undervoltage lockout, by EN/FAULT and SAS pins, or when V_{OUT} falls below the supply pin voltage (V_{CC}) by 100mV typical at T_A = +25°C, V_{CC} = 5V.

10. Pad layout as shown in Diodes Incorporated's package outline PDFs, which can be found on our website at http://www.diodes.com/package-outlines.html.

Marking Information

W-QFN3020-12

(Top View)



XX : Identification Code

Y : Year : 0 to 9 (ex: 4 = 2024)

W : Week : A to Z : week 1 to 26; a to z : week 27 to 52; z represents week 52 and 53

y : Internal Code

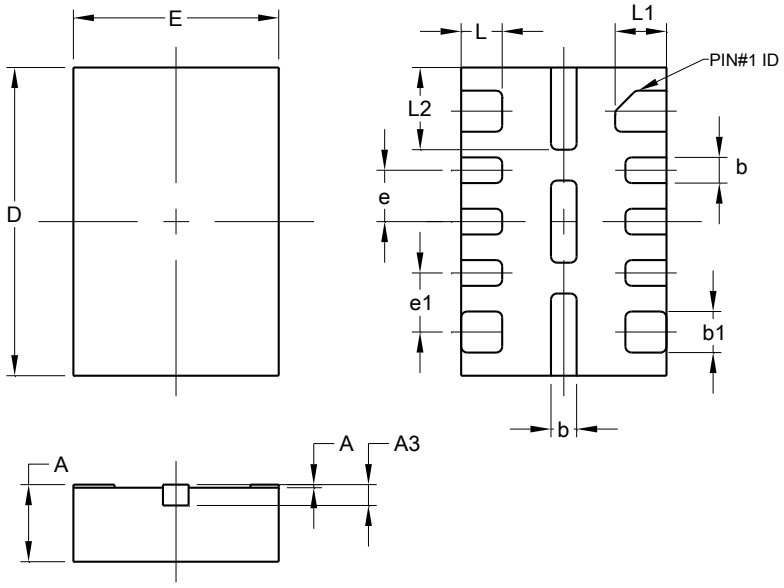
x : Internal Code

Part Number	Package	Identification Code
AP91350HMN1-DT8-7R	W-QFN3020-12	H9

Package Outline Dimensions

Please see http://www.diodes.com/package-outlines.html for the latest version.

W-QFN3020-12

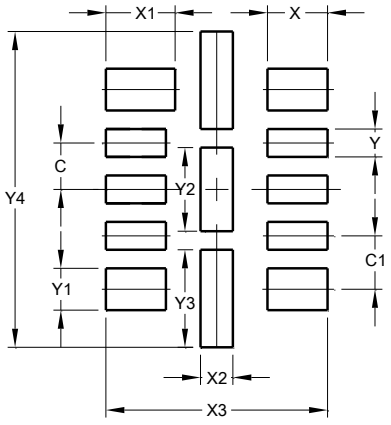


W-QFN3020-12			
Dim	**Min**	**Max**	**Typ**
A	0.700	0.800	-
A1	0	0.05	-
A3	0.203REF		
b	0.200	0.300	-
b1	0.350	0.450	-
D	1.900	2.100	2.000
E	2.900	3.100	3.000
e	-	-	0.500
e1	-	-	0.575
L	0.350	0.450	-
L1	0.450	0.550	-
L2	0.750	0.850	-
All Dimensions in mm			

Suggested Pad Layout

Please see http://www.diodes.com/package-outlines.html for the latest version.

W-QFN3020-12



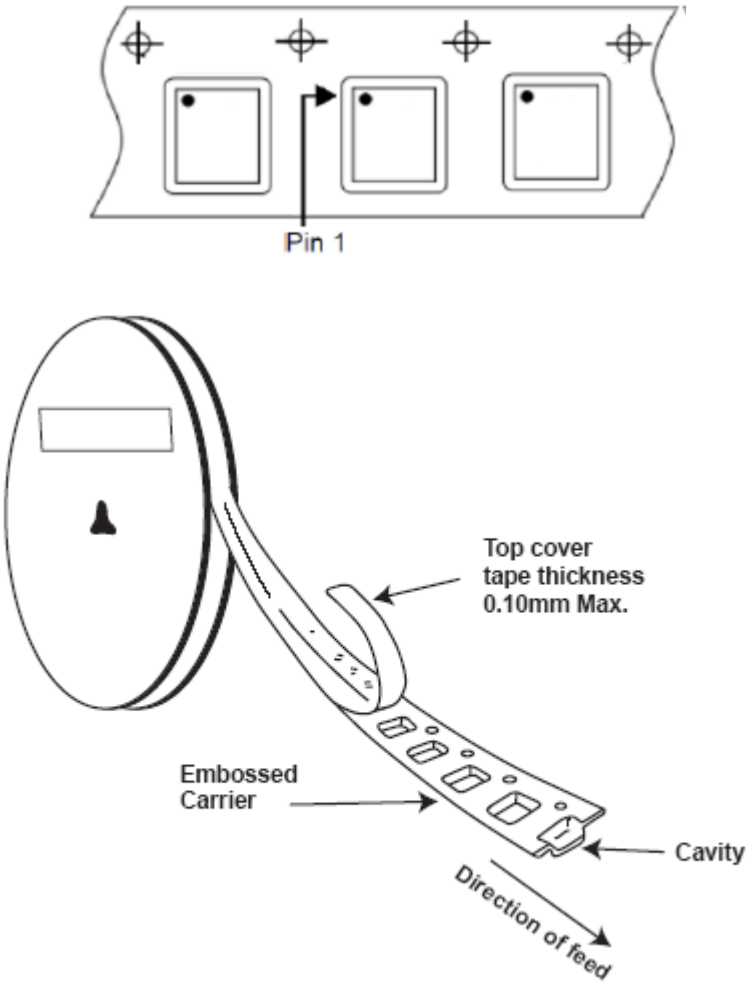
Dimensions	Value (in mm)
C	0.500
G	0.575
X	0.650
X1	0.750
X2	0.350
X3	2.400
Y	0.300
Y1	0.450
Y2	0.900
Y3	1.050
Y4	3.400

Mechanical Data

- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals: Finish-Matte Tin Plated Leads, Solderable per MIL-STD-202, Method 208 e3
- Weight: 0.012 grams (Approximate)

Taping Orientation

Package Type: W-QFN3020-12



Note: 11. The taping orientation of the other package type can be found on our website at https://www.diodes.com/assets/Packaging-Support-Docs/ap02007.pdf.

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