

## 4 CHANNEL LOW CAPACITANCE TVS DIODE ARRAY

### Product Summary

<b>V<sub>BR</sub> (Min)</b>	<b>I<sub>PP</sub> (Max)</b>	<b>C<sub>T</sub> (Typ)</b>
5V	3.5A	0.23pF

### Description

The D3V3XS4B10LP is a high-performance device suitable for protecting four high speed I/Os. These devices are assembled in U-DFN2510-10 package and have high ESD surge capability, low ESD clamping voltage and Ultra-low capacitance.

### Applications

Typically used at high-speed ports such as USB 3.0, USB 3.1, Serial ATA, Display port.

### Features

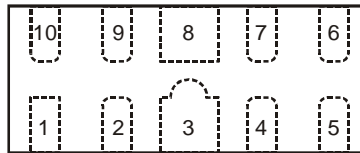
- Clamping Voltage: 11.2V at 16A TLP
- IEC 61000-4-2 (ESD): Air — ±8kV, Contact — ±8kV
- IEC 61000-4-5 (Lightning): 3.5A (8/20µs)
- 4 Channels of ESD Protection
- Ultra-low Channel Input Capacitance of 0.23pF Typical
- TLP Dynamic Resistance: 0.55Ω
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**

### Mechanical Data

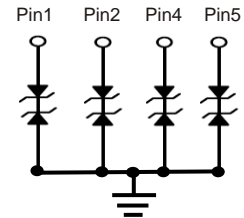
- Case: U-DFN2510-10
- Case Material: Molded Plastic, "Green" Molding Compound.  
UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals: NiPdAu over Copper Leadframe (Lead Free Plating).  
Solderable per MIL-STD-202, Method 208 (e4)
- Weight: 0.038 grams (Approximate)

Pin Number	Description
1, 2, 4, 5	I/O
6, 7, 9, 10	No Connection
3, 8	V <sub>SS</sub>

U-DFN2510-10



Pin Description (Top View)



Device Schematic

### Ordering Information (Note 4)

Part Number	Compliance	Marking	Reel Size (inches)	Tape Width (mm)	Quantity per Reel
D3V3XS4B10LP-7	Standard	MW7	7	8	3,000/Tape & Reel

- Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
  2. See <https://www.diodes.com/quality/lead-free/> for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
  3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
  4. For packaging details, go to our website at <https://www.diodes.com/design/support/packaging/diodes-packaging/>.

### Marking Information

U-DFN2510-10



MW7 = Product Type Marking Code  
 YM = Date Code Marking  
 Y = Year (ex: F = 2018)  
 M = Month (ex: 9 = September)

#### Date Code Key

Year	2018	2019	2020	2021	2022	2023
Code	F	G	H	I	J	K

Month	Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec
Code	1	2	3	4	5	6	7	8	9	O	N	D

**Maximum Ratings** (@T<sub>A</sub> = +25°C, unless otherwise specified.)

Characteristic	Symbol	Value	Unit	Conditions
Peak Pulse Current, per IEC 61000-4-5	I <sub>PP</sub>	3.5	A	I/O to V <sub>SS</sub> , 8/20μs
Peak Pulse Power, per IEC 61000-4-5	P <sub>PP</sub>	20	W	I/O to V <sub>SS</sub> , 8/20μs
ESD Protection – Contact Discharge, per IEC 61000-4-2	V <sub>ESD_Contact</sub>	±8	kV	I/O to V <sub>SS</sub>

**Thermal Characteristics**

Characteristic	Symbol	Value	Unit
Power Dissipation Typical (Note 5)	P <sub>D</sub>	350	mW
Thermal Resistance, Junction to Ambient Typical (Note 5)	R <sub>θJA</sub>	360	°C/W
Operating and Storage Temperature Range	T <sub>J</sub> , T <sub>STG</sub>	-55 to +150	°C

**Electrical Characteristics** (@T<sub>A</sub> = +25°C, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Conditions
Reverse Working Voltage	V <sub>RWM</sub>	—	—	3.3	V	—
Reverse Current	I <sub>R</sub>	—	—	1.0	μA	V <sub>R</sub> = 3.3V, I/O to V <sub>SS</sub>
Reverse Breakdown Voltage	V <sub>BR</sub>	5	—	9	V	I <sub>R</sub> = 1mA, I/O to V <sub>SS</sub>
Clamping Voltage (Note 6)	V <sub>C</sub>	—	11.2	—	V	TLP, 16A, t <sub>p</sub> = 100ns, I/O to V <sub>SS</sub>
Dynamic Reverse Resistance	R <sub>DIF</sub>	—	0.55	—	Ω	TLP, 10A, t <sub>p</sub> = 100ns, I/O to V <sub>SS</sub>
Channel Input Capacitance	C <sub>I/O</sub>	—	0.23	—	pF	V <sub>I/O</sub> = 0V, V <sub>SS</sub> = 0V, f = 1MHz

- Notes:
5. Device mounted on FR-4 PCB pad layout (2oz copper) as shown in Diodes Incorporated's package outline PDFs, which can be found on our website at <http://www.diodes.com/package-outlines.html>.
  6. Clamping voltage value is based on a TLP model. TLP conditions: Z<sub>0</sub> = 50Ω, t<sub>p</sub> = 100ns, t<sub>p</sub> = 1ns, averaging window; t<sub>1</sub> = 70ns to t<sub>2</sub> = 90ns.

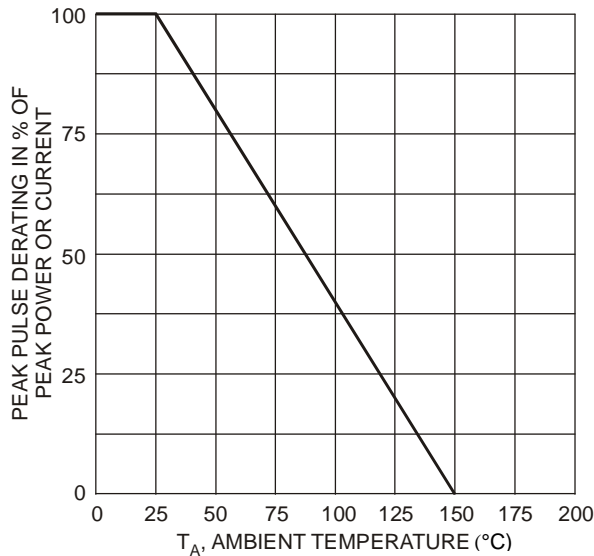


Figure 1 Pulse Derating Curve

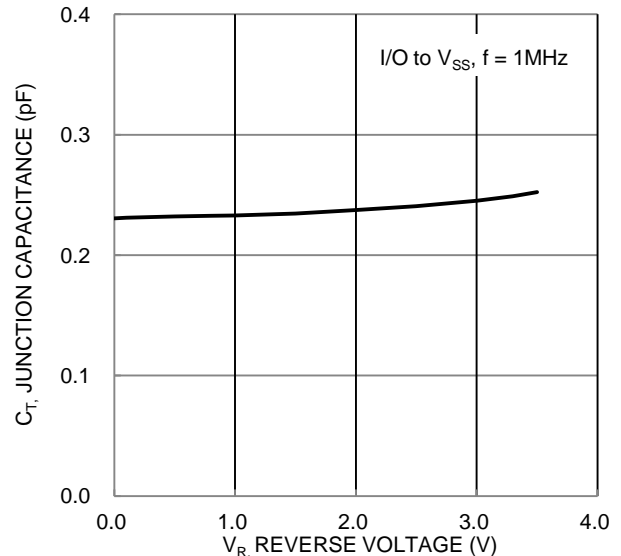
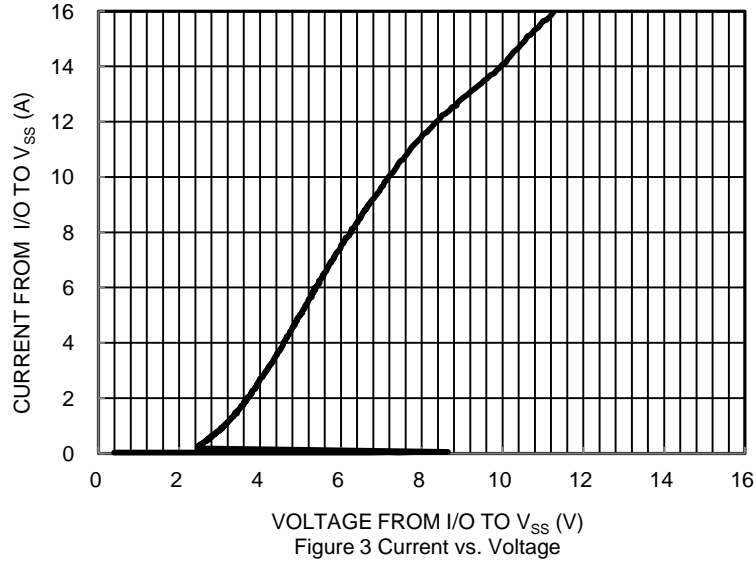


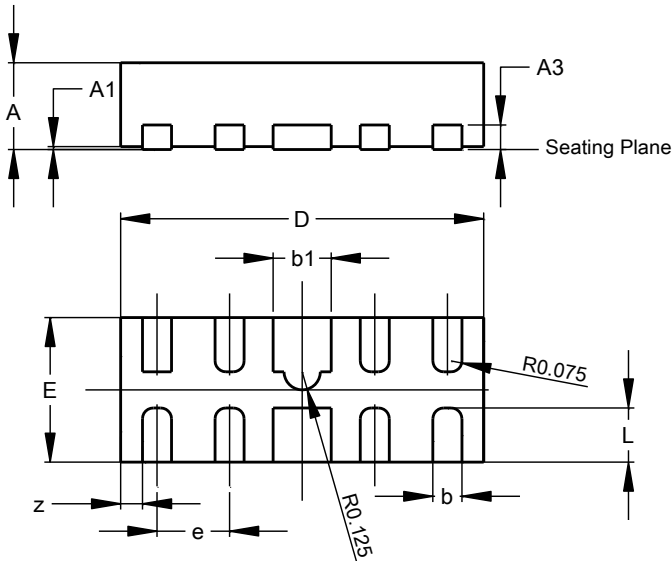
Figure 2 Typical Total Capacitance



**Package Outline Dimensions**

Please see <http://www.diodes.com/package-outlines.html> for the latest version.

**U-DFN2510-10**

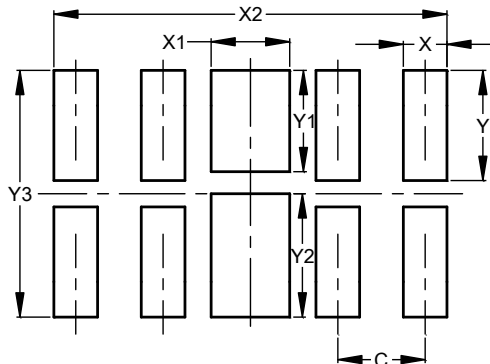


U-DFN2510-10			
Dim	Min	Max	Typ
A	0.545	0.605	0.575
A1	0.00	0.05	0.03
A3	-	-	0.13
b	0.15	0.25	0.20
b1	0.35	0.45	0.40
D	2.450	2.575	2.500
e	-	-	0.50
E	0.950	1.075	1.000
L	0.325	0.425	0.375
z	-	-	0.150
All Dimensions in mm			

**Suggested Pad Layout**

Please see <http://www.diodes.com/package-outlines.html> for the latest version.

**U-DFN2510-10**



Dimensions	Value (in mm)
C	0.500
X	0.250
X1	0.450
X2	2.250
Y	0.625
Y1	0.575
Y2	0.700
Y3	1.400

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