



ESD PROTECTION FOR ETHERNET INTERFACES

Product Summary

V _{RWM} Max	V _{hold} Min	I _R Max
24V	28V	100nA

Features and Benefits

- One Channel of ESD Protection
- Sidewall Plating for Easy Optical Inspection
- Low Profile and Ultra-small Form Factor Minimizes PCB Footprint
- Provides ESD Protection per IEC 61000-4-2 Standard: Air ±30kV. Contact ±30kV
- Low Channel Input Capacitance to Prevent Data Degradation
- Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)
- Halogen and Antimony Free. "Green" Device (Note 3)
- The DESD1ETH1GLPSQ is suitable for automotive applications requiring specific change control; this part is AEC-Q101 qualified, PPAP capable, and manufactured in IATF 16949 certified facilities.

https://www.diodes.com/quality/product-definitions/

Description and Applications

This DESD1ETH1GLPSQ is Fully OPEN Alliance 100BASE-T1 and 1000BASE-T1 compliant electrostatic discharge (ESD) protection and surge protection device packaged in a small footprint surface-mount package. The combination of small size and high ESD surge capability makes it ideal for use in automotive applications.

- Open alliance 100/1000BASE-T1 ethernets
- Low-voltage differential signaling (LVDS) automotives
- Automotive in-vehicle network lines

Mechanical Data

- Package: U-DFN1006-2 with Sidewall Plating
- Package Material: Molded Plastic, "Green" Molding Compound.
 UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals: 100% NiPdAu
 Solderable per MIL-STD-202, Method 208 (e4)
- Weight: 0.001 grams (Approximate)

U-DFN1006-2/SWP







Top View

Bottom View

Device Schematic

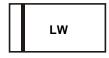
Ordering Information (Note 4)

Orderable Bort Number	Pookogo	Marking	Reel Size (inches)	Tape Width (mm)	Packing	
Orderable Part Number Package Marking Reel	Reel Size (Iliches)	rape widin (ililii)	Qty.	Carrier		
DESD1ETH1GLPSQ-7B	U-DFN1006-2/SWP	LW	7	8	10,000	Tape & Reel

Notes:

- 1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
- 2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
- 3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
- 4. For packaging details, go to our website at https://www.diodes.com/design/support/packaging/diodes-packaging/

Marking Information



LW = Product Type Marking Code Bar Denotes Pin 1



Maximum Ratings (@ $T_A = +25$ °C, unless otherwise specified.)

Characteristic	Symbol	Value	Unit	Conditions
Peak Pulse Current	IPP	2.3	Α	8/20µs, Per Figure 3
	VESD_Contact	±30	kV	IEC 61000-4-2; contact discharge
	VESD_Contact	±30	kV	ISO 10605; contact discharge; C = 150pF; $R = 330\Omega$
ESD Protection – Contact Discharge	VESD_Contact	±30	kV	ISO 10605; contact discharge; C = 330pF; $R = 330\Omega$
	VESD_Contact	±30	kV	1000 contact discharges (IEC 61000-4-2); OPEN Alliance specification
ESD Protection – Air Discharge	VESD_Air	±30	kV	IEC 61000-4-2; Air discharge

Thermal Characteristics

Characteristic	Symbol	Value	Unit
Package Power Dissipation (Note 5)	PD	250	mW
Thermal Resistance, Junction to Ambient (Note 5)	R _θ JA	500	°C/W
Operating Junction Temperature Range	TJ	-55 to +150	°C
Storage Temperature Range	Tstg	-55 to +150	°C

Electrical Characteristics (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Min	Тур	Max	Unit	Test Conditions	
Reverse Working Voltage	VRWM	_	_	24	V	_	
Reverse Leakage Current (Note 6)	IR	_	_	100	nA	V _{RWM} = 24V	
Trigger Voltage (Note 7)	VTR	100	160	_	V	TLP, t _R = 10ns, t _P = 100ns	
Holding Voltage (Note 7)	Vhold	28	_	_	V		
Dynamic Resistance (Note 7)	R _{DYN}	_	0.6	_	Ω	TLP, 40A, $t_R = 10$ ns, $t_P = 100$ ns	
Channel Input Capacitance	Ст	_	1.2	1.8	pF	$V_{IN} = 0V, f = 1MHz$	

Notes:

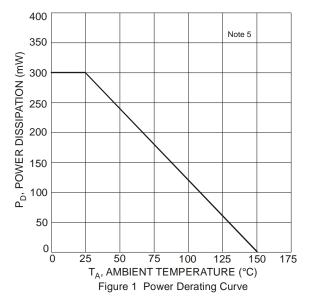
^{5.} Device mounted on FR-4 PCB pad layout (2oz copper) as shown in Diodes Incorporated's package outline PDFs, which can be found on our website at http://www.diodes.com/package-outlines.html.

^{6.} Short duration pulse test used to minimize self-heating effect.

^{7.} Non-repetitive current pulse, Transmission Line Pulse (TLP); square pulse.







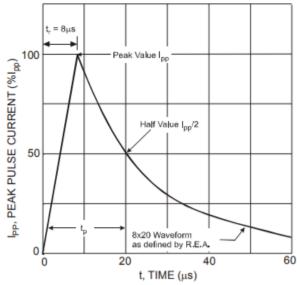


Figure 3 Typical 8 × 20µs Pulse Waveform

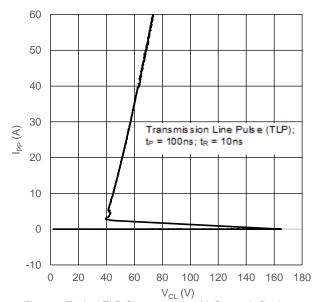
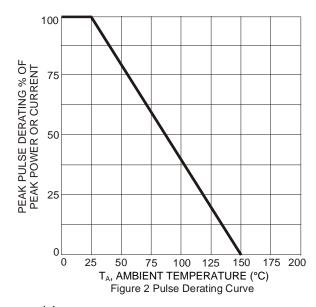


Figure 5 Typical TLP Characteristic with Dynamic Resistance



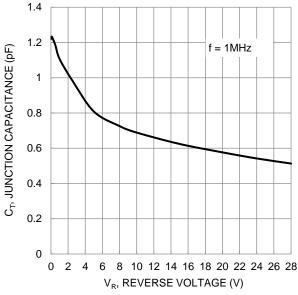
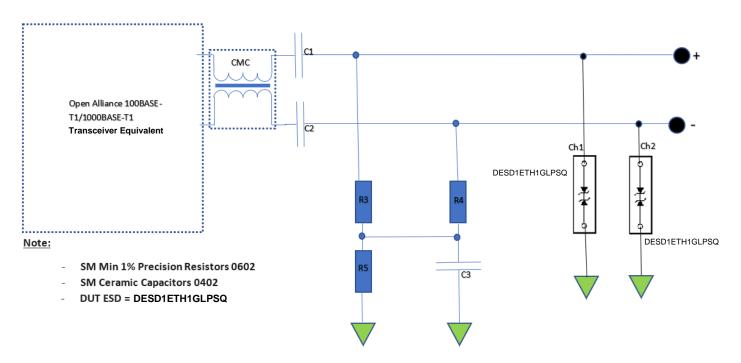


Figure 4 Typical Junction Capacitance



Application Data

In the IEEE 100BASE-T1 and 1000BASE-T1 EMC Test Specification for ESD suppression devices (OPEN Alliance 100/1000BASE-T1 specification), the OPEN Alliance describes four different tests to ensure compliance of ESD suppressor devices and PHYs which are compliant according to the document "Transceiver EMC Test Specification". The return loss and insertion loss are evaluated using the differential S-parameters Sdd11 and Sdd21. These measurements replace the requirement for a certain capacitance value.



To ensure symmetry, the differential to common mode rejection is evaluated using the S-parameter Ssd21. This measurement replaces the requirement for a matching of the capacitances per line. To ensure that the device does not degrade and changes behavior after repetitive ESD events, the S-parameter measurements are repeated after discharging 20 times ± 8 kV ESD on signal lines 1 and 2, with C = 150pF, R = 330Ω according to ISO 10605.

Subsequently, the S-parameters are measured again and compared to the original data. To predict if the ESD suppressor device would protect a PHY of a certain robustness class (Class I (JEDEC-HBM 4kV) and Class II (JEDEC-HBM 2kV)), the ESD discharge current is measured in a reference circuit according to OPEN Alliance 100/1000BASE-T1 specification for ± 4 kV and ± 6 kV according to IEC 61000-4-2 with C = 150pF and R = 330 Ω . Transceiver simulation network is implemented with 2Ω and 50Ω resistors.

The return loss and insertion loss are evaluated using the differential S-parameters Sdd11 and Sdd21. These measurements replace the requirement for a certain capacitance value. To ensure symmetry, the differential to common mode rejection is evaluated using the S-parameter Ssd21. This measurement replaces the requirement for a matching of the capacitances per line. To ensure that the device does not degrade and changes behavior after repetitive ESD events, the S-parameter measurements are repeated after discharging 20 times $\pm 8kV$ ESD on signal lines 1 and 2, with C = 150pF, R = 330 Ω according to ISO 10605. Subsequently, the S-parameters are measured again and compared to the original data.



Application Data (continued)

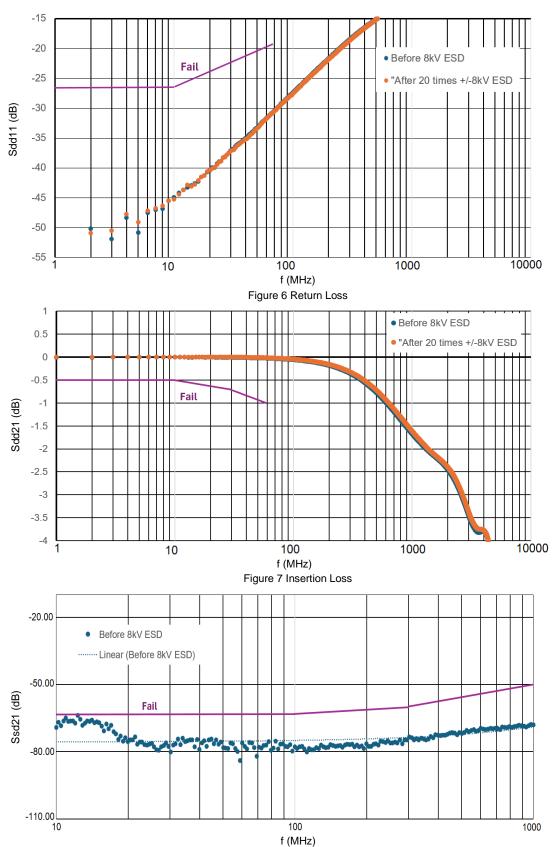


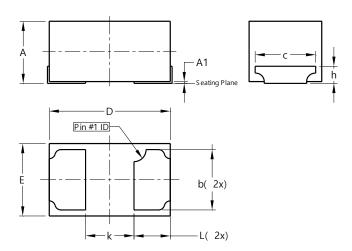
Figure 8. Differential to Common Mode Rejection



Package Outline Dimensions

Please see http://www.diodes.com/package-outlines.html for the latest version.

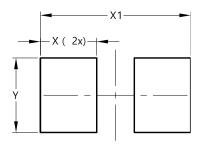
U-DFN1006-2/SWP



U-DFN1006-2/SWP					
Dim	Min	Max	Тур		
Α	0.47	0.53	0.50		
A1	0.0	0.05	0.03		
b	0.45	0.55	0.50		
С	0.55 REF				
D	0.95	1.05	1.00		
E	0.55	0.65	0.60		
h	0.17 REF				
k	0.37 REF				
L	0.25	0.35	0.30		
All Dimensions in mm					

Suggested Pad Layout

U-DFN1006-2/SWP



Dimensions	Value (in mm)
Х	0.45
X1	1.20
Υ	0.60



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