COMPLEMENTARY PAIR ENHANCEMENT MODE MOSFET

Product Summary

Device	BV_{DSS}	$R_{DS(ON)}$ Max	I_D Max T_A = +25°C
Q1	30V	0.4Ω @ V_{GS} = 10V	0.9A
		0.7Ω @ V_{GS} = 4.5V	0.68A
Q2	-30V	0.9Ω @ V_{GS} = -10V	-0.6A
		1.7Ω @ V_{GS} = -4.5V	-0.43A

Features and Benefits

- Low On-Resistance
- Low Input Capacitance
- Fast Switching Speed
- ESD Protected Gate
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**
- **The DMC3350LDWQ is suitable for automotive applications requiring specific change control; this part is AEC-Q101 qualified, PPAP capable, and manufactured in IATF16949 certified facilities.**
  https://www.diodes.com/quality/product-definitions/

Description and Applications

This MOSFET is designed to minimize the on-state resistance ($R_{DS(ON)}$) yet maintain superior switching performance, making it ideal for high-efficiency power-management applications.

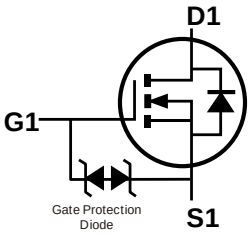
- Motor controls
- Power-management functions
- DC-DC converters

Mechanical Data

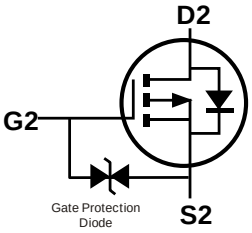
- Package: SOT363
- Package Material: Molded Plastic, "Green" Molding Compound. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminal Connections Indicator: See Diagram
- Terminals: Finish — Matte Tin Annealed over Copper Leadframe. Solderable per MIL-STD-202, Method 208 e3
- Weight: 0.027 grams (Approximate)

SOT363

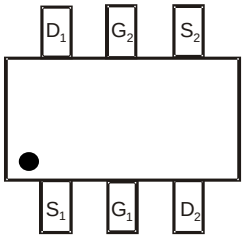
Top View



Q1 N-CHANNEL



Q2 P-CHANNEL



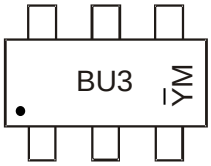
Top View
Pin Out

Ordering Information (Note 4)

Part Number	Package	Packing	
		Qty.	Carrier
DMC3350LDWQ-7	SOT363	3000	Tape & Reel
DMC3350LDWQ-13	SOT363	10000	Tape & Reel

Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
4. For packaging details, go to our website at https://www.diodes.com/design/support/packaging/diodes-packaging/.

Marking Information



BU3 = Product Type Marking Code
YM = Date Code Marking
Y = Year (ex: L = 2024)
M = Month (ex: 9 = September)

Date Code Key

Year	2024	2025	2026	2027	2028	2029	2030	2031	2032	2033	2034	2035
Code	L	M	N	P	R	S	T	U	V	W	X	Y

Month	Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec
Code	1	2	3	4	5	6	7	8	9	O	N	D

Maximum Ratings (@T_A = +25°C, unless otherwise specified.)

Characteristic			Symbol	Value_Q1	Value_Q2	Unit
Drain-Source Voltage			V_{DSS}	30	-30	V
Gate-Source Voltage			V_{GSS}	±20	±20	V
Continuous Drain Current (Note 5) Q1: V_{GS} = 10V Q2: V_{GS} = -10V	Steady State	T_A = +25°C T_A = +70°C	I_D	0.9 0.72	-0.6 -0.48	A
Maximum Continuous Body Diode Forward Current (Note 5)			I_S	0.44	-0.44	A
Pulsed Drain Current (10µs Pulse, Duty Cycle = 1%)			I_{DM}	3.4	-2.5	A

Thermal Characteristics (@T_A = +25°C, unless otherwise specified.)

Characteristic		Symbol	Value	Unit
Total Power Dissipation (Note 6)		P_D	0.35	W
Thermal Resistance, Junction to Ambient (Note 6)	Steady State	$R_{\theta JA}$	353	°C/W
Total Power Dissipation (Note 5)		P_D	0.49	W
Thermal Resistance, Junction to Ambient (Note 5)	Steady State	$R_{\theta JA}$	254	°C/W
Operating and Storage Temperature Range		T_J, T_{STG}	-55 to +150	°C

Notes: 5. Device mounted on FR-4 substrate PC board, 2oz copper, with 1inch square copper plate.
6. Device mounted on FR-4 substrate PC board, 2oz copper, with minimum recommended pad layout.

Electrical Characteristics – N Channel – Q1 (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 7)						
Drain-Source Breakdown Voltage	BV_{DSS}	30	—	—	V	V_{GS} = 0V, I_D = 250μA
Zero Gate Voltage Drain Current	I_{DSS}	—	—	1.0	μA	V_{DS} = 30V, V_{GS} = 0V
Gate-Source Leakage	I_{GSS}	—	—	±10	μA	V_{GS} = ±20V, V_{DS} = 0V
ON CHARACTERISTICS (Note 7)						
Gate Threshold Voltage	$V_{GS(TH)}$	0.8	—	1.6	V	V_{DS} = V_{GS}, I_D = 250μA
Static Drain-Source On-Resistance	$R_{DS(ON)}$	—	0.24	0.4	Ω	V_{GS} = 10V, I_D = 0.59A
		—	0.32	0.7		V_{GS} = 4.5V, I_D = 0.2A
Diode Forward Voltage	V_{SD}	—	0.7	1.2	V	V_{GS} = 0V, I_S = 0.1A
DYNAMIC CHARACTERISTICS (Note 8)						
Input Capacitance	C_{iss}	—	38.4	—	pF	V_{DS} = 15V, V_{GS} = 0V f = 1.0MHz
Output Capacitance	C_{oss}	—	10.5	—	pF	
Reverse Transfer Capacitance	C_{rss}	—	6.4	—	pF	
Total Gate Charge (V_{GS} = 4.5V)	Q_g	—	0.5	—	nC	V_{DS} = 10V, I_D = 250mA
Total Gate Charge (V_{GS} = 10V)	Q_g	—	1.1	—	nC	
Gate-Source Charge	Q_{gs}	—	0.2	—	nC	
Gate-Drain Charge	Q_{gd}	—	0.1	—	nC	
Turn-On Delay Time	$t_{D(ON)}$	—	3.2	—	ns	V_{GS} = 10V, V_{DS} = 30V I_D = 100mA, R_G = 25Ω
Turn-On Rise Time	t_R	—	12	—	ns	
Turn-Off Delay Time	$t_{D(OFF)}$	—	82	—	ns	
Turn-Off Fall Time	t_F	—	51	—	ns	

Electrical Characteristics – P Channel – Q2 (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 7)						
Drain-Source Breakdown Voltage	BV_{DSS}	-30	—	—	V	V_{GS} = 0V, I_D = -250μA
Zero Gate Voltage Drain Current	I_{DSS}	—	—	-1	μA	V_{DS} = -24V, V_{GS} = 0V
Gate-Source Leakage	I_{GSS}	—	—	±10	μA	V_{GS} = ±16V, V_{DS} = 0V
ON CHARACTERISTICS (Note 7)						
Gate Threshold Voltage	$V_{GS(TH)}$	-1	—	-2.6	V	V_{DS} = V_{GS}, I_D = -250μA
Static Drain-Source On-Resistance	$R_{DS(ON)}$	—	0.46	0.9	Ω	V_{GS} = -10V, I_D = -0.42A
		—	0.89	1.7		V_{GS} = -4.5V, I_D = -0.2A
Diode Forward Voltage	V_{SD}	—	-0.8	-1.2	V	V_{GS} = 0V, I_S = -0.23A
DYNAMIC CHARACTERISTICS (Note 8)						
Input Capacitance	C_{iss}	—	19	—	pF	V_{DS} = -15V, V_{GS} = 0V f = 1.0MHz
Output Capacitance	C_{oss}	—	16	—	pF	
Reverse Transfer Capacitance	C_{rss}	—	3	—	pF	
Total Gate Charge (V_{GS} = -4.5V)	Q_g	—	0.36	—	nC	V_{DS} = -10V, I_D = -0.24A
Total Gate Charge (V_{GS} = -10V)	Q_g	—	0.8	—	nC	
Gate-Source Charge	Q_{gs}	—	0.1	—	nC	
Gate-Drain Charge	Q_{gd}	—	0.1	—	nC	
Turn-On Delay Time	$t_{D(ON)}$	—	30	—	ns	V_{GS} = -10V, V_{DD} = -15V I_D = -0.5A, R_G = 1Ω
Turn-On Rise Time	t_R	—	74	—	ns	
Turn-Off Delay Time	$t_{D(OFF)}$	—	28	—	ns	
Turn-Off Fall Time	t_F	—	31	—	ns	

Notes: 7. Short duration pulse test used to minimize self-heating effect.
8. Guaranteed by design. Not subject to product testing.

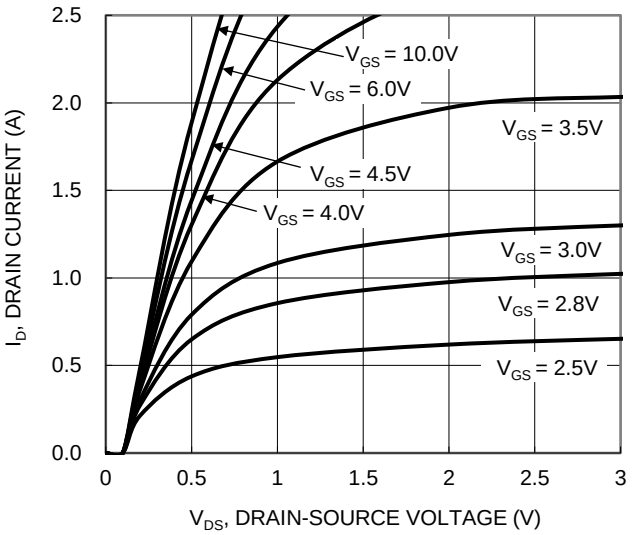


Figure 1. Typical Output Characteristic (Q1)

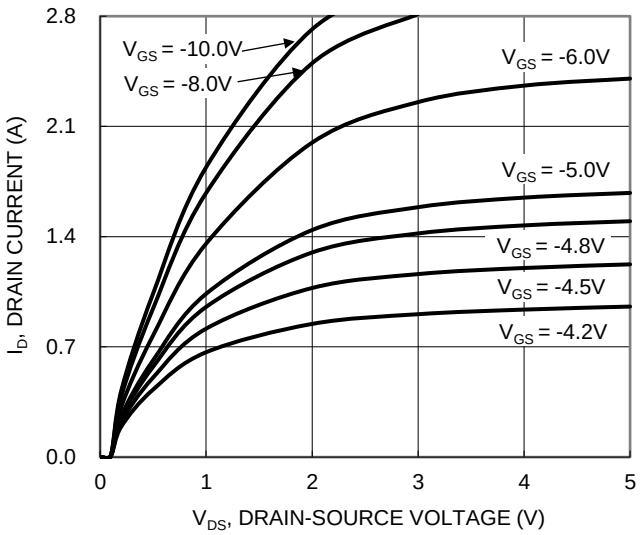


Figure 2. Typical Output Characteristic (Q2)

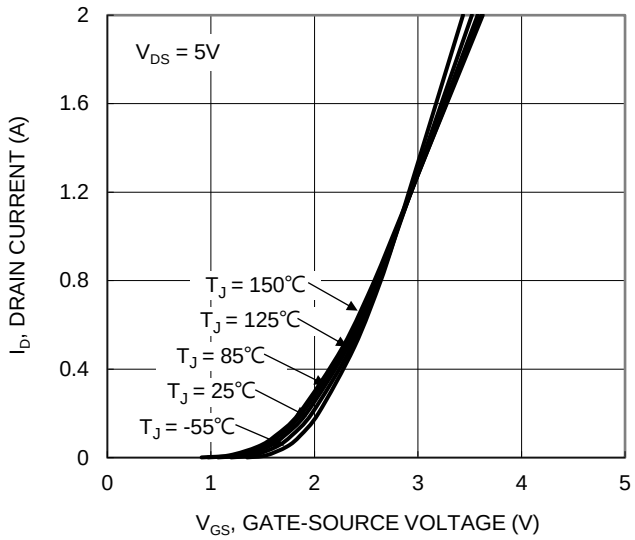


Figure 3. Typical Transfer Characteristic (Q1)

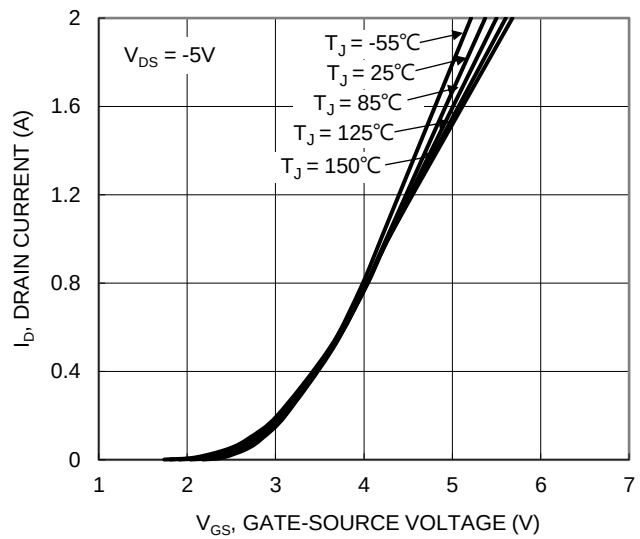


Figure 4. Typical Transfer Characteristic (Q2)

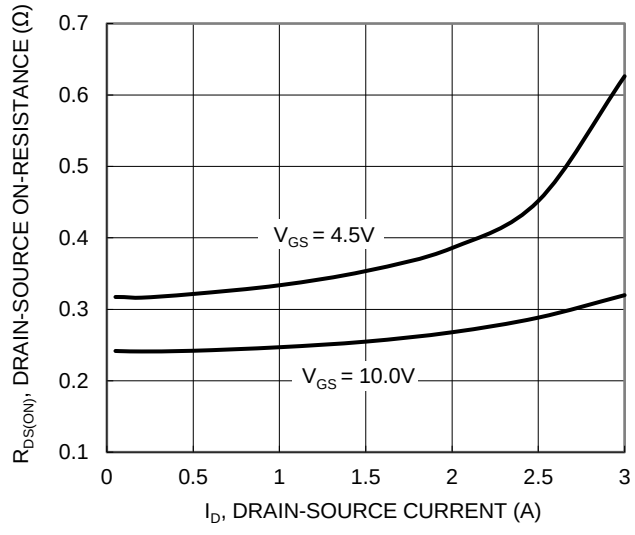


Figure 5. Typical On-Resistance vs. Drain Current and Gate Voltage (Q1)

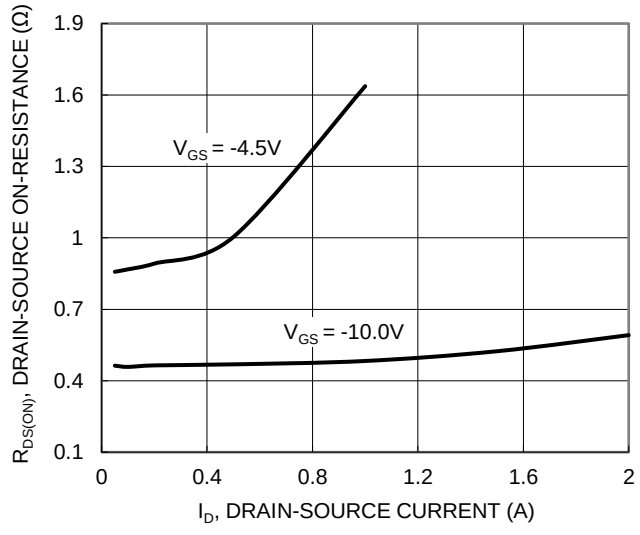


Figure 6. Typical On-Resistance vs. Drain Current and Gate Voltage (Q2)

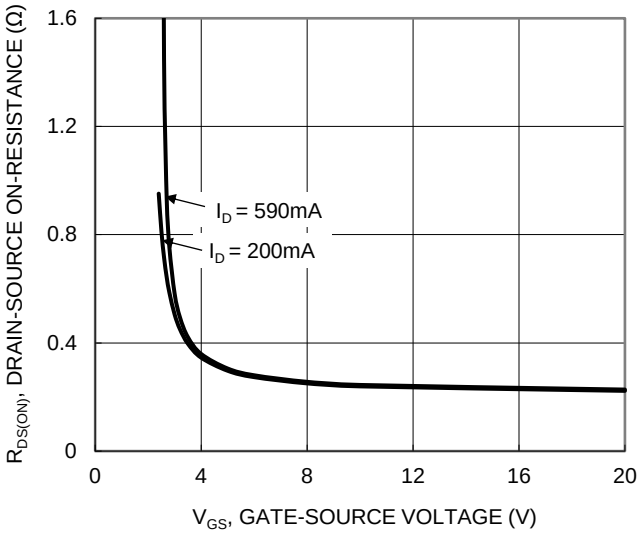


Figure 7. Typical Transfer Characteristic (Q1)

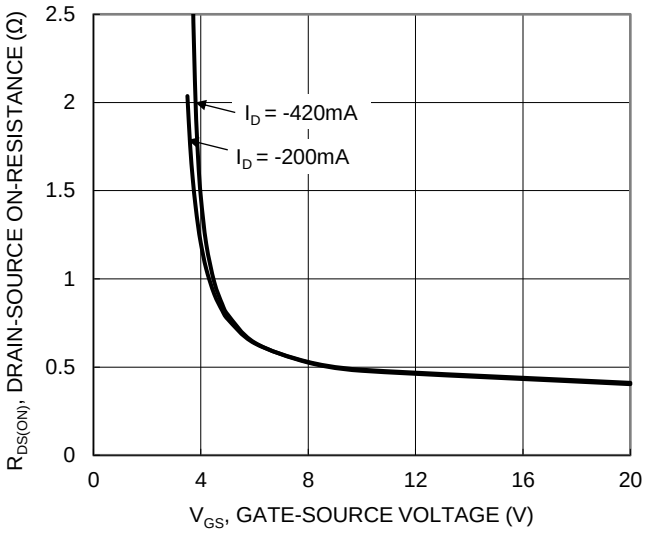


Figure 8. Typical Transfer Characteristic (Q2)

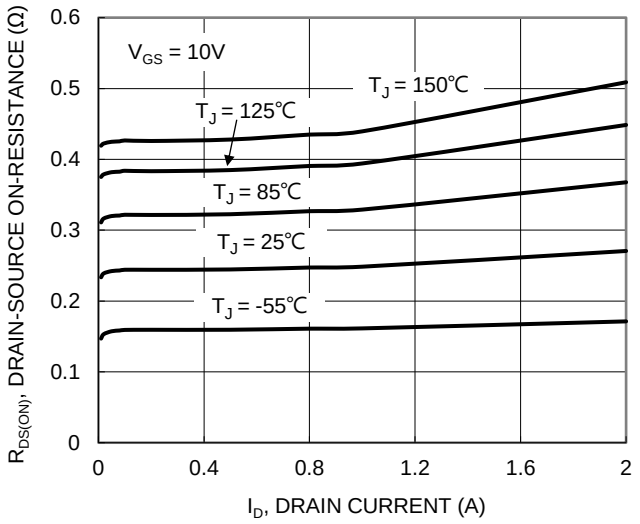


Figure 9. Typical On-Resistance vs. Drain Current and Junction Temperature (Q1)

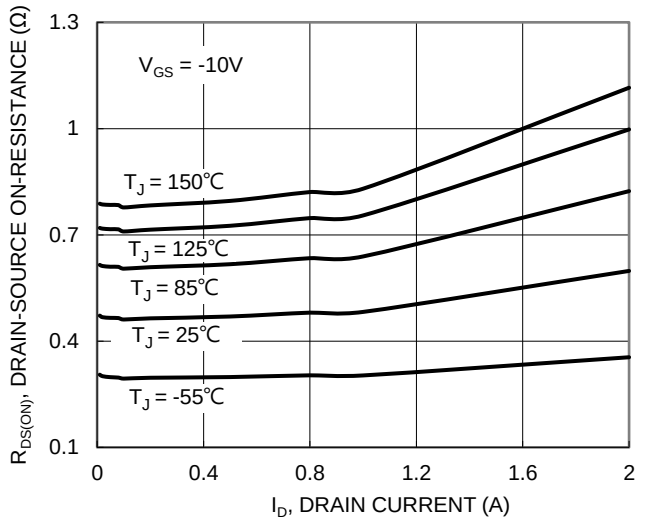


Figure 10. Typical On-Resistance vs. Drain Current and Junction Temperature (Q2)

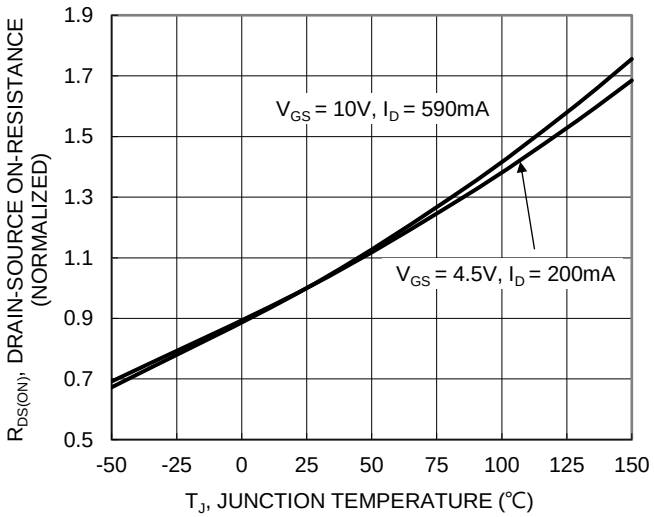


Figure 11. On-Resistance Variation with Junction Temperature (Q1)

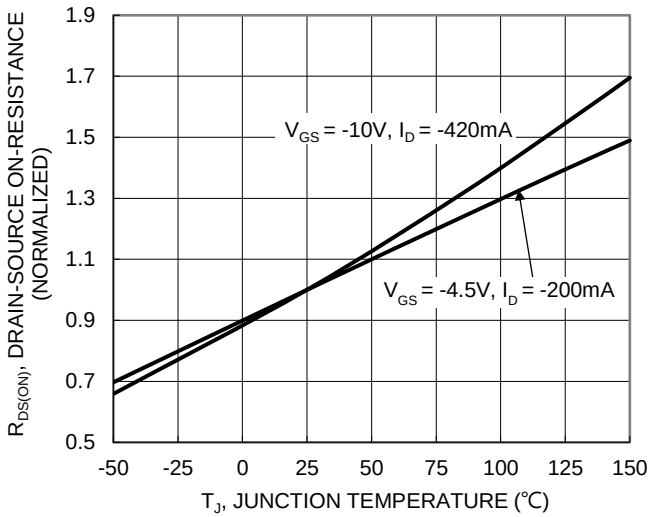


Figure 12. On-Resistance Variation with Junction Temperature (Q2)

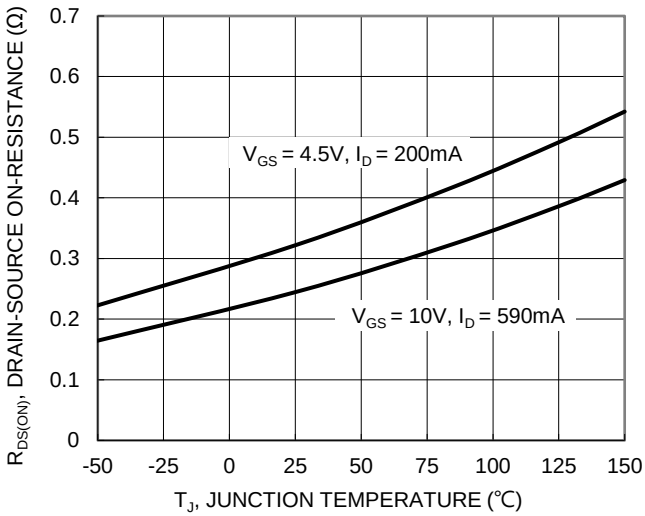


Figure 13. On-Resistance Variation with Junction Temperature (Q1)

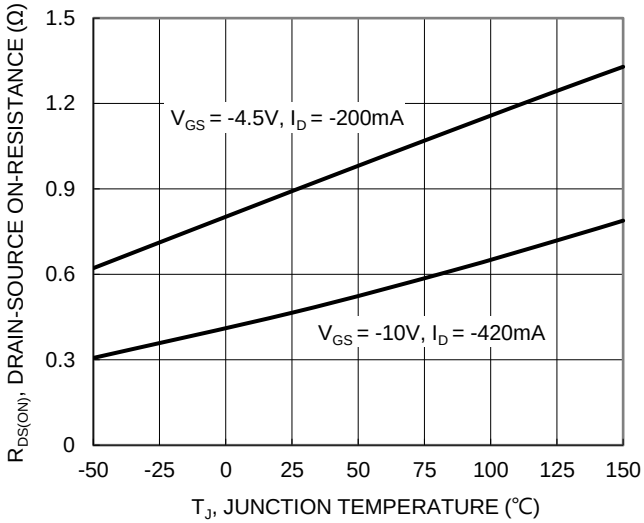


Figure 14. On-Resistance Variation with Junction Temperature (Q2)

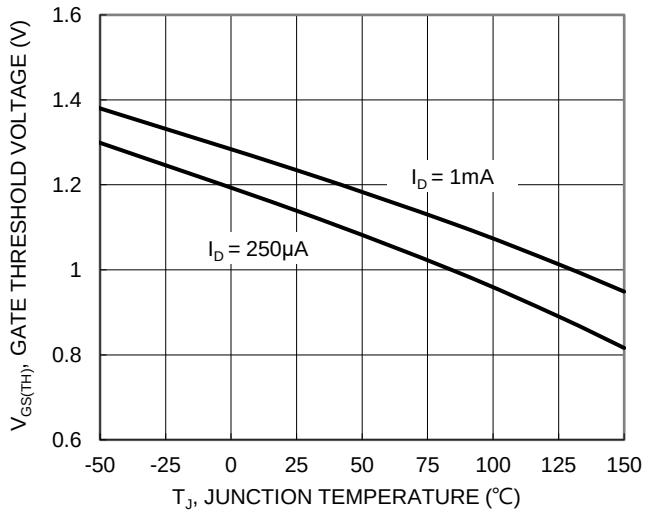


Figure 15. Gate Threshold Variation vs. Junction Temperature (Q1)

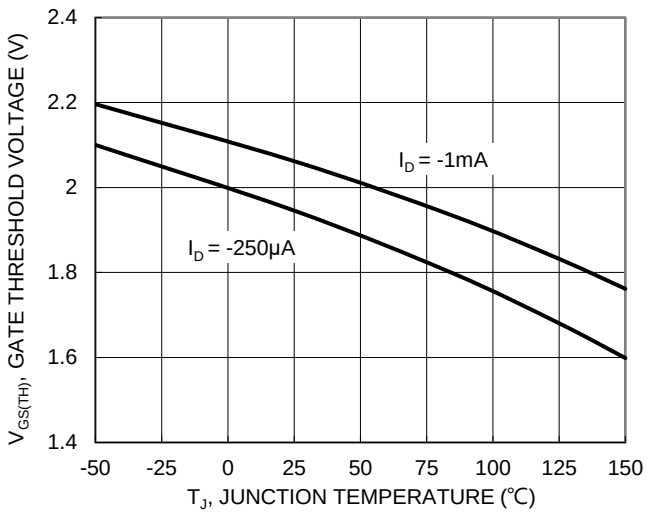


Figure 16. Gate Threshold Variation vs. Junction Temperature (Q2)

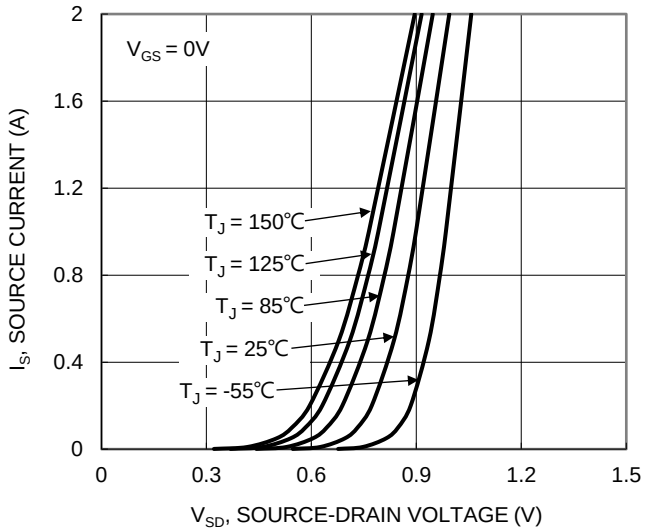


Figure 17. Diode Forward Voltage vs. Current (Q1)

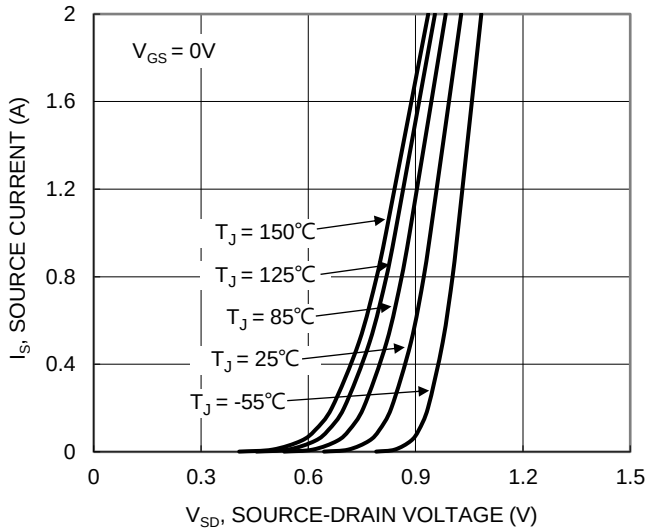


Figure 18. Diode Forward Voltage vs. Current (Q2)

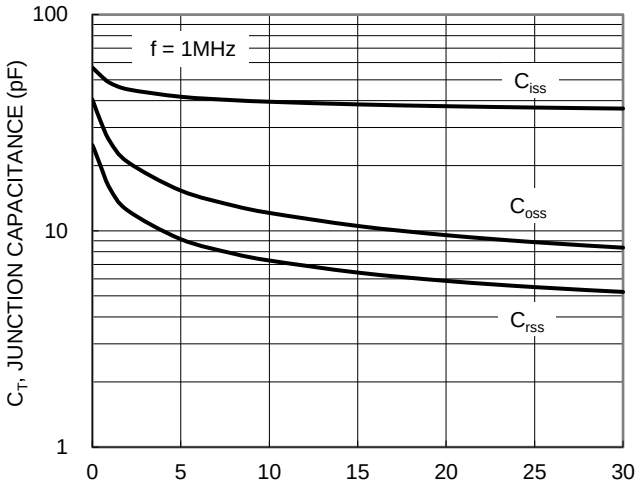


Figure 19. Typical Junction Capacitance (Q1)

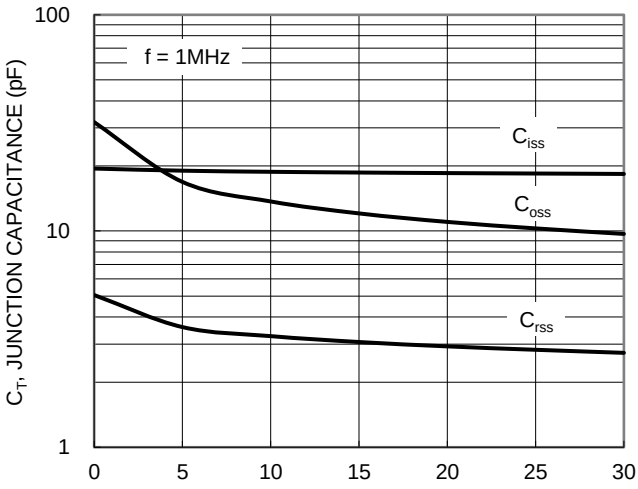


Figure 20. Typical Junction Capacitance (Q2)

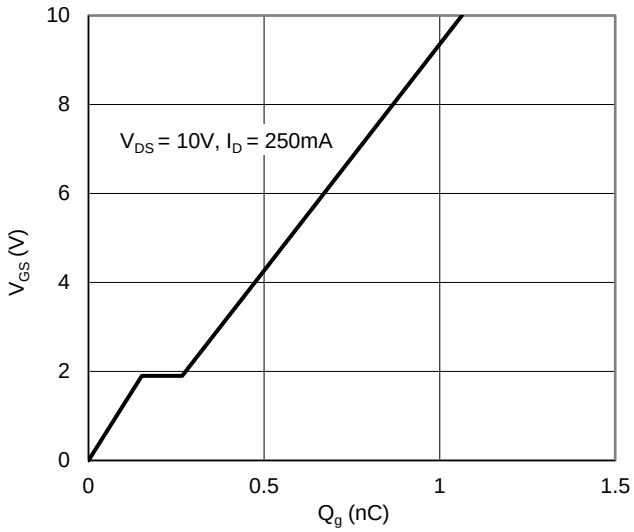


Figure 21. Gate Charge (Q1)

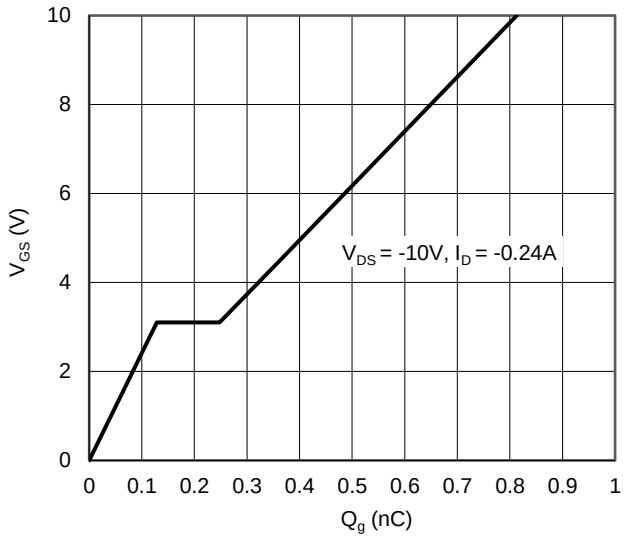


Figure 22. Gate Charge (Q2)

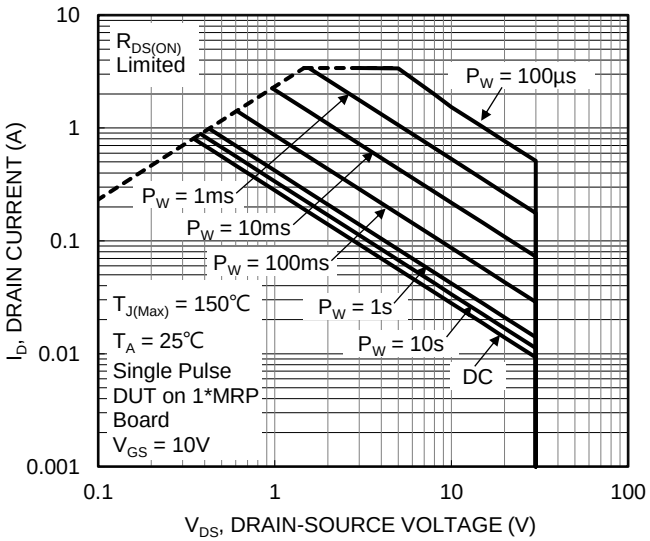


Figure 23. SOA, Safe Operation Area (Q1)

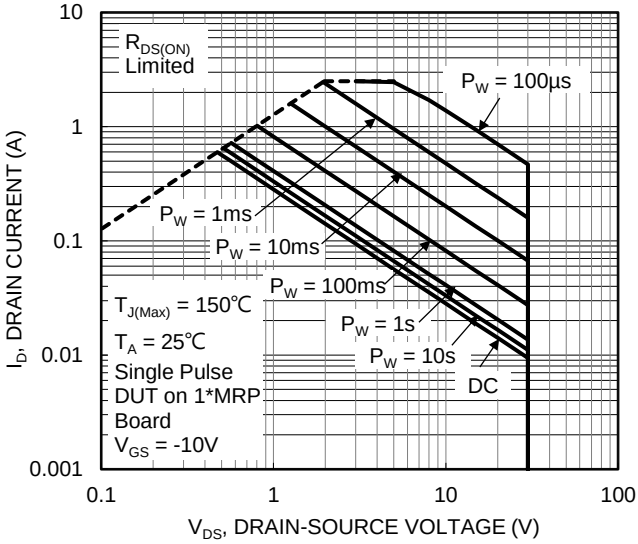


Figure 24. SOA, Safe Operation Area (Q2)

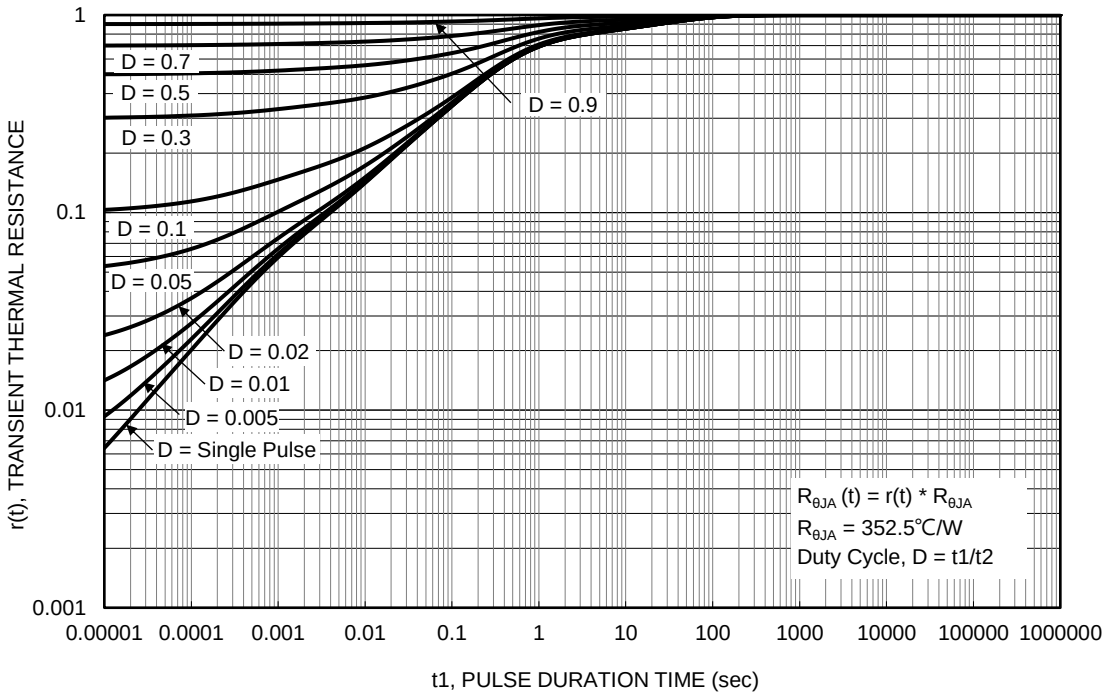
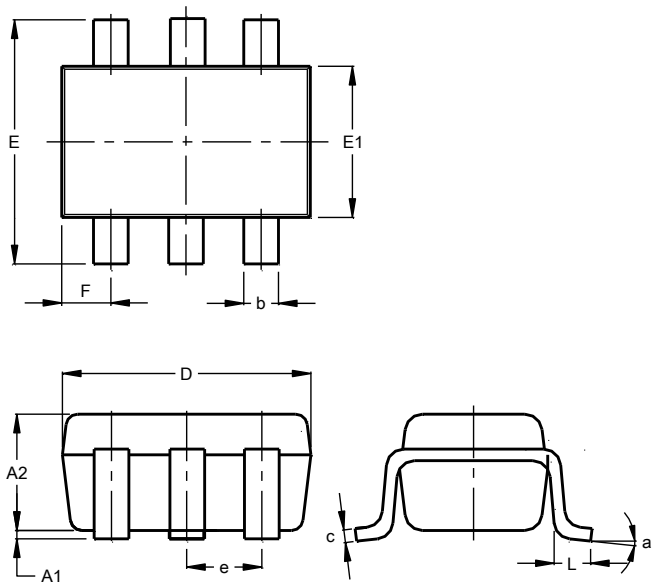


Figure 25. Transient Thermal Resistance (Q1/Q2)

Package Outline Dimensions

Please see http://www.diodes.com/package-outlines.html for the latest version.

SOT363

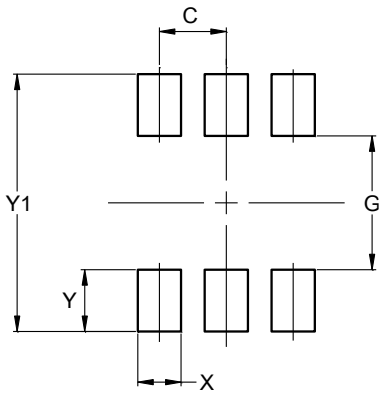


SOT363			
Dim	**Min**	**Max**	**Typ**
A1	0.00	0.10	0.05
A2	0.90	1.00	0.95
b	0.10	0.30	0.25
c	0.10	0.22	0.11
D	1.80	2.20	2.15
E	2.00	2.20	2.10
E1	1.15	1.35	1.30
e	0.650 BSC		
F	0.40	0.45	0.425
L	0.25	0.40	0.30
a	0°	8°	--
All Dimensions in mm			

Suggested Pad Layout

Please see http://www.diodes.com/package-outlines.html for the latest version.

SOT363



Dimensions	Value (in mm)
C	0.650
G	1.300
X	0.420
Y	0.600
Y1	2.500

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